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[Diodes Incorporated](#)  
[DMN2005K-7](#)

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**DMN2005K**

**N-CHANNEL ENHANCEMENT MODE FIELD EFFECT TRANSISTOR**

**Features**

- Low On-Resistance
- Very Low Gate Threshold Voltage, 0.9V Max.
- Fast Switching Speed
- Low Input/Output Leakage
- Ultra-Small Surface Mount Package
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **ESD Protected Gate**

**Mechanical Data**

- Case: SOT23
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish — Matte Tin annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208 (E3)
- Ordering & Date Code Information: See Below
- Weight: 0.008 grams (approximate)

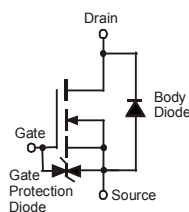


ESD protected

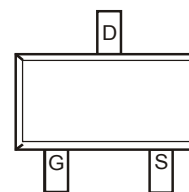


SOT23

TOP VIEW



Equivalent Circuit



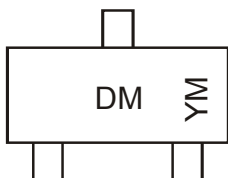
TOP VIEW

**Ordering Information** (Note 4)

Part Number	Case	Packaging
DMN2005K-7	SOT23	3000/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
  2. See [http://www.diodes.com/quality/lead\\_free.html](http://www.diodes.com/quality/lead_free.html) for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

**Marking Information**



DM = Product Type Marking Code  
 YM = Date Code Marking  
 Y = Year ex: T = 2006  
 M = Month ex: 9 = September

Date Code Key

Year	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
Code	T	U	V	W	X	Y	Z	A	B	C	D	E	F	G	H
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec			
Code	1	2	3	4	5	6	7	8	9	O	N	D			

**Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V <sub>DSS</sub>	20	V
Gate-Source Voltage	V <sub>GSS</sub>	±10	V
Drain Current per element (Note 5)	I <sub>D</sub>	300	mA
Continuous Pulsed (Note 6)		600	

**Thermal Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P <sub>D</sub>	350	mW
Thermal Resistance, Junction to Ambient	R <sub>θJA</sub>	357	°C/W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-65 to +150	°C

**Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 7)</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	20	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 100μA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	—	—	10	μA	V <sub>DS</sub> = 17V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	—	—	±5	μA	V <sub>GS</sub> = ±8V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS (Note 7)</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	0.53	—	0.9	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 100μA
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	—	0.55	3.5	Ω	V <sub>GS</sub> = 1.8V, I <sub>D</sub> = 200mA
		—	0.4	1.7		
Forward Transfer Admittance	Y <sub>fs</sub>	40	—	—	mS	V <sub>DS</sub> = 3V, I <sub>D</sub> = 10mA

- Notes: 5. Device mounted on FR-4 PCB.  
 6. Pulse width ≤10μS, Duty Cycle ≤1%.  
 7. Short duration pulse test used to minimize self-heating effect.

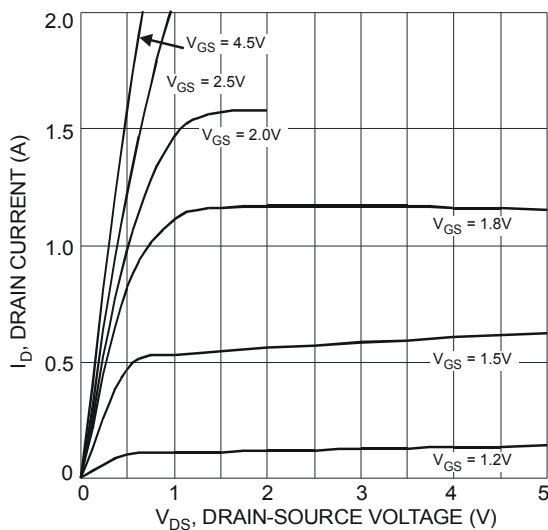


Fig. 1 Typical Output Characteristics

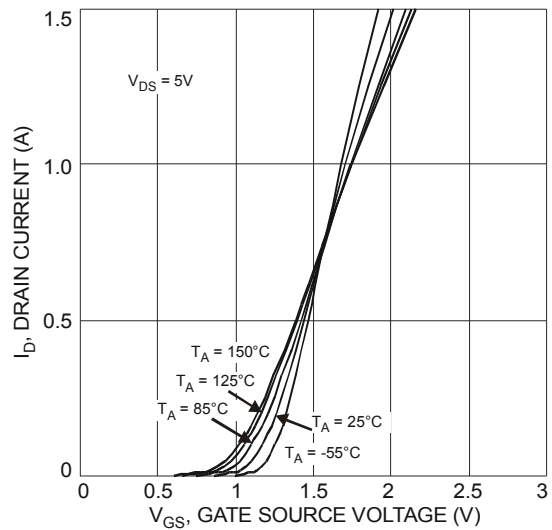


Fig. 2 Typical Transfer Characteristics



**DMN2005K**

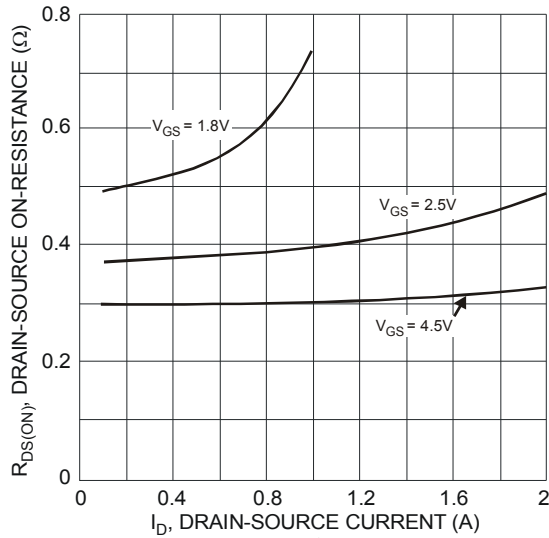


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

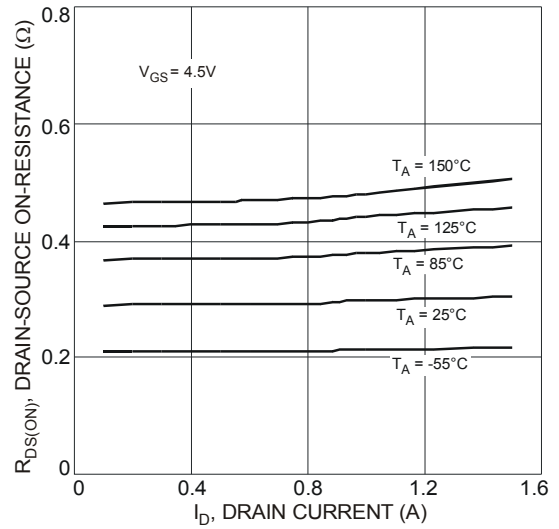


Fig. 4 Typical Drain-Source On-Resistance vs. Drain Current and Temperature

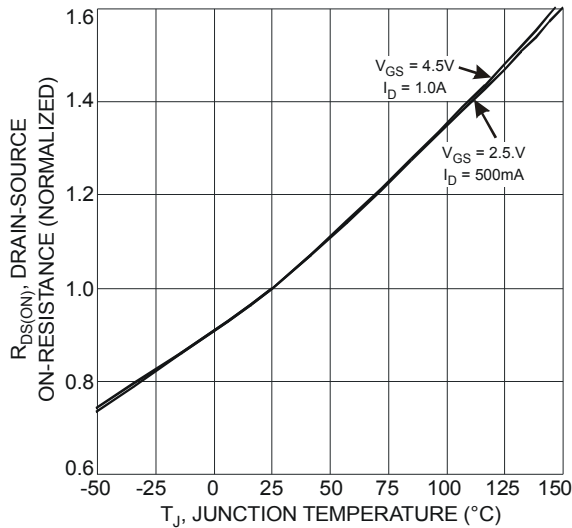


Fig. 5 On-Resistance Variation with Temperature

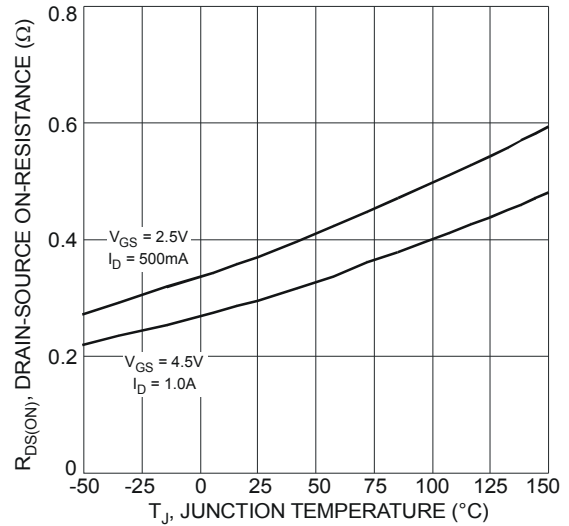


Fig. 6 On-Resistance Variation with Temperature

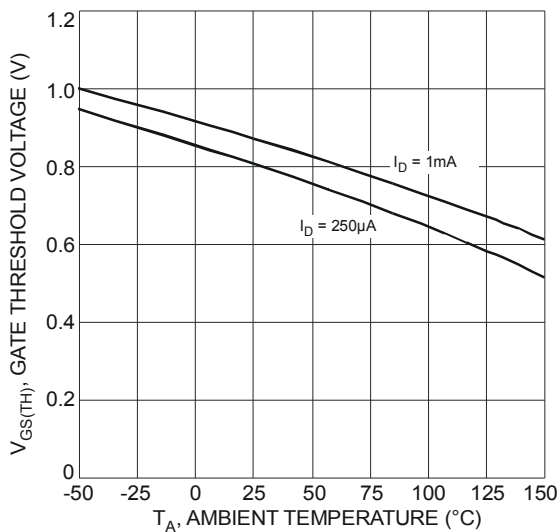


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

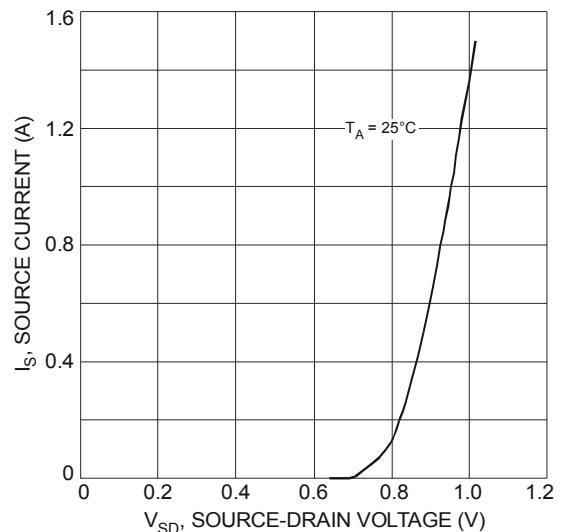
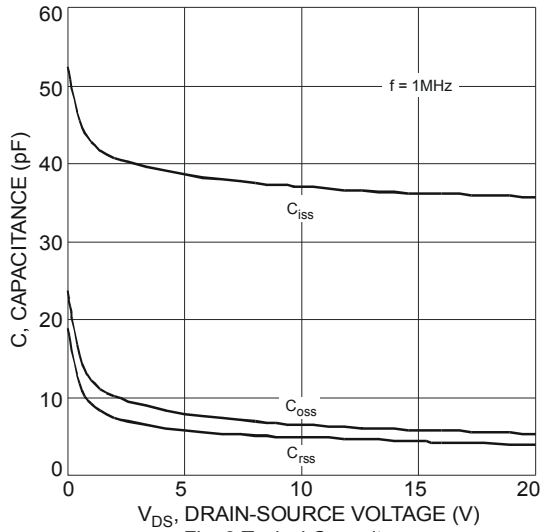


Fig. 8 Diode Forward Voltage vs. Current

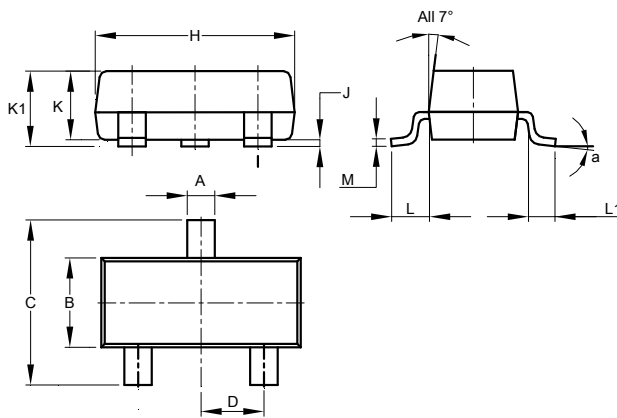


**DMN2005K**



**Package Outline Dimensions**

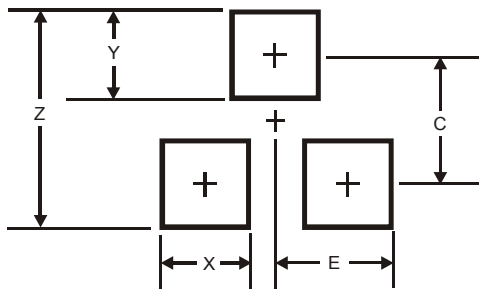
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.



SOT23			
Dim	Min	Max	Typ
A	0.37	0.51	0.40
B	1.20	1.40	1.30
C	2.30	2.50	2.40
D	0.89	1.03	0.915
F	0.45	0.60	0.535
G	1.78	2.05	1.83
H	2.80	3.00	2.90
J	0.013	0.10	0.05
K	0.890	1.00	0.975
K1	0.903	1.10	1.025
L	0.45	0.61	0.55
L1	0.25	0.55	0.40
M	0.085	0.150	0.110
a	8°		
All Dimensions in mm			

**Suggested Pad Layout**

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



Dimensions	Value (in mm)
Z	2.9
X	0.8
Y	0.9
C	2.0
E	1.35

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