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PSMN8R5-100XSQ

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# PSMN8R5-100XS

## N-channel 100V 8.5 mΩ standard level MOSFET in TO220F (SOT186A)

**29 November 2012** **Product data sheet**

## 1. Product profile

### 1.1 General description

Standard level N-channel MOSFET in TO220F (SOT186A) package qualified to 175C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

### 1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Isolated package
- Suitable for standard level gate drive

### 1.3 Applications

- AC-to-DC power supply equipment
- Motor control
- Server power supplies
- Synchronous rectification

### 1.4 Quick reference data

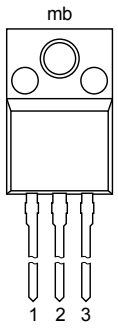
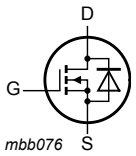
**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | $T_j \geq 25$ °C; $T_j \leq 175$ °C | | - | - | 100 | V |
| $I_D$ | drain current | $T_{mb}$ = 25 °C; $V_{GS}$ = 10 V; Fig. 1 | | - | - | 49 | A |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Fig. 2 | | - | - | 55 | W |
| **Static characteristics** | | | | | | | |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 10 A; $T_j$ = 25 °C; Fig. 12; Fig. 13 | | 4.5 | 6.4 | 8.5 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 10 A; $T_j$ = 100 °C; Fig. 13 | | - | 11.18 | 14.9 | mΩ |
| **Dynamic characteristics** | | | | | | | |
| $Q_{GD}$ | gate-drain charge | $V_{GS}$ = 10 V; $I_D$ = 10 A; $V_{DS}$ = 50 V; Fig. 14; Fig. 15 | | - | 30 | - | nC |
| $Q_{G(tot)}$ | total gate charge | | | - | 100 | - | nC |

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Avalanche ruggedness** | | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; $I_D$ = 49 A; $V_{sup}$ ≤ 100 V; unclamped; $R_{GS}$ = 50 Ω; Fig. 3 | | - | - | 439 | mJ |

## 2. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | G | gate |   TO-220F (SOT186A) |   |
| 2 | D | drain | | |
| 3 | S | source | | |
| mb | | mounting base; isolated | | |

## 3. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PSMN8R5-100XS | TO-220F | plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack" | SOT186A |

## 4. Marking

**Table 4. Marking codes**

| Type number | Marking code |
|---|---|
| PSMN8R5-100XS | PSMN8R5-100XS |

## 5. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | $T_j$ ≥ 25 °C; $T_j$ ≤ 175 °C | | - | 100 | V |

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DGR}$ | drain-gate voltage | $T_j \geq 25$ °C; $T_j \leq 175$ °C; $R_{GS} = 20$ kΩ | | - | 100 | V |
| $V_{GS}$ | gate-source voltage | | | -20 | 20 | V |
| $I_D$ | drain current | $V_{GS} = 10$ V; $T_{mb} = 25$ °C; Fig. 1 | | - | 49 | A |
| | | $V_{GS} = 10$ V; $T_{mb} = 100$ °C; Fig. 1 | | - | 34.6 | A |
| $I_{DM}$ | peak drain current | pulsed; $t_p \leq 10$ µs; $T_{mb} = 25$ °C; Fig. 4 | | - | 196 | A |
| $P_{tot}$ | total power dissipation | $T_{mb} = 25$ °C; Fig. 2 | | - | 55 | W |
| $T_{stg}$ | storage temperature | | | -55 | 175 | °C |
| $T_j$ | junction temperature | | | -55 | 175 | °C |
| $T_{sld(M)}$ | peak soldering temperature | | | - | 260 | °C |
| **Source-drain diode** | | | | | | |
| $I_S$ | source current | $T_{mb} = 25$ °C | | - | 46 | A |
| $I_{SM}$ | peak source current | pulsed; $t_p \leq 10$ µs; $T_{mb} = 25$ °C | | - | 196 | A |
| **Avalanche ruggedness** | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $V_{GS} = 10$ V; $T_{j(init)} = 25$ °C; $I_D = 49$ A; $V_{sup} \leq 100$ V; unclamped; $R_{GS} = 50$ Ω; Fig. 3 | | - | 439 | mJ |

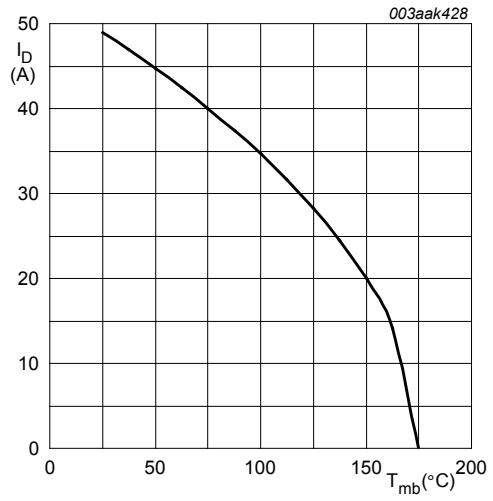



**Fig. 1. Continuous drain current as a function of mounting base temperature**

$V_{GS} \geq 10V$

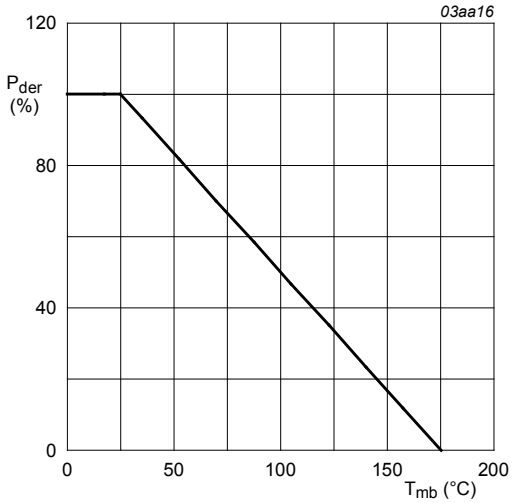



**Fig. 2. Normalized total power dissipation as a function of mounting base temperature**

$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

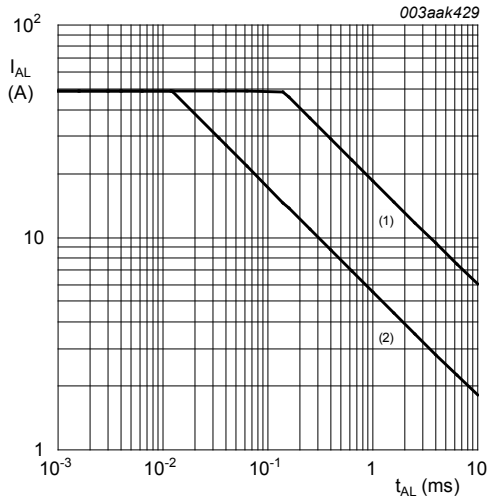



**Fig. 3. Avalanche rating; avalanche current as a function of avalanche time**

(1) $T_{j\ (init)} = 25°C$; (2) $T_{j\ (init)} = 130°C$

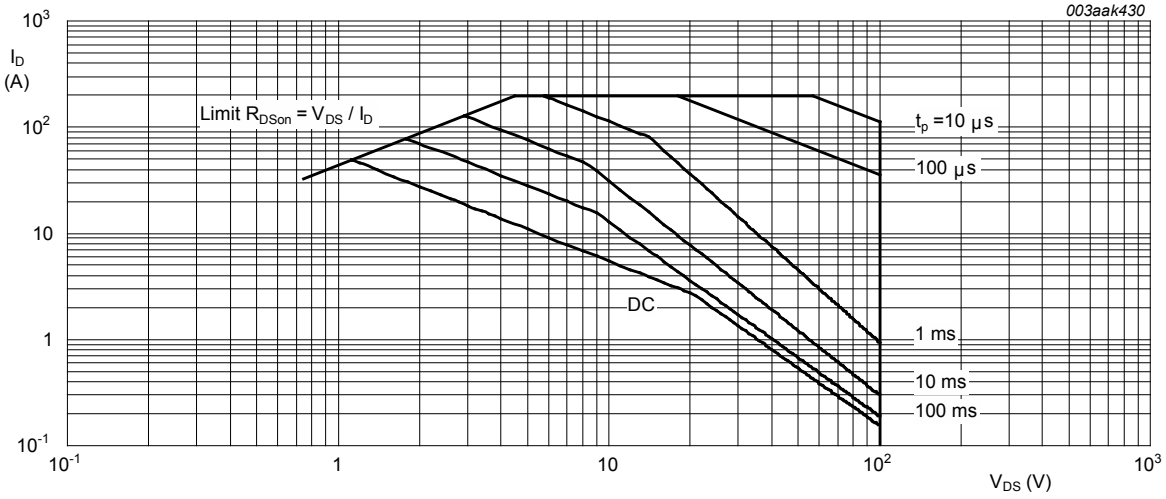



**Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

$T_{mb} = 25°C$; $I_{DM}$ *is a single pulse*

## 6. Thermal characteristics

**Table 6. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{th(j\text{-}mb)}$ | thermal resistance from junction to mounting base | Fig. 5 | | - | 2.5 | 2.73 | K/W |
| $R_{th(j\text{-}a)}$ | thermal resistance from junction to ambient | vertical in free air | | - | 55 | - | K/W |

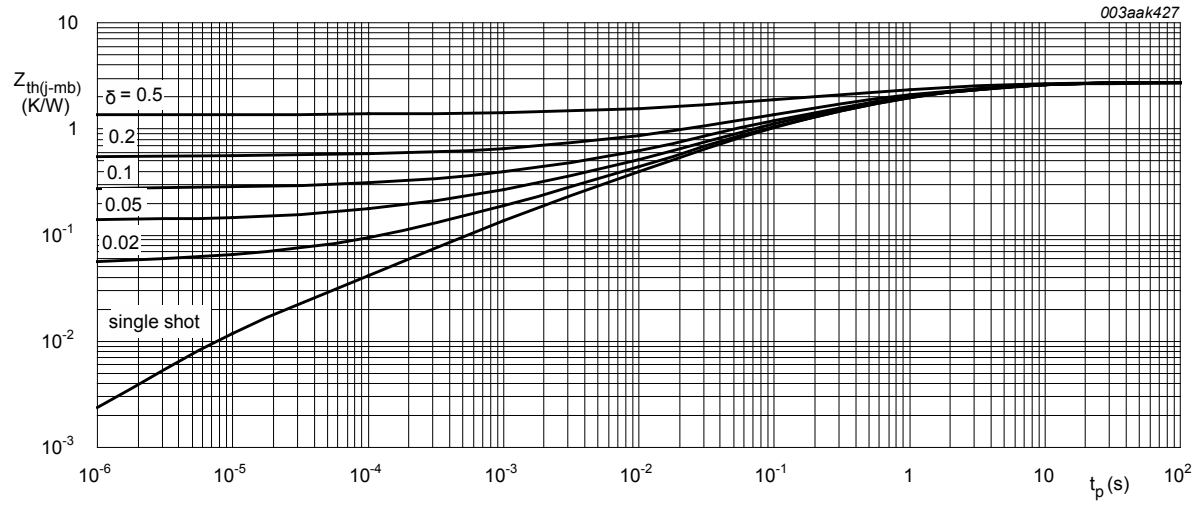



**Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration**

## 7. Isolation characteristics

**Table 7. Isolation characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $C_{isol}$ | isolation capacitance | | [1] | - | 10 | - | pF |
| $V_{isol(RMS)}$ | RMS isolation voltage | 50 Hz ≤ f ≤ 60 Hz; RH ≤ 65 %; sinusoidal waveform; clean and dust free | | - | - | 2500 | V |

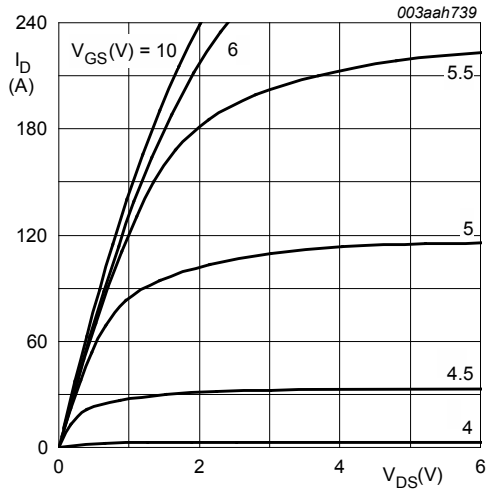
[1] f = 1 MHz

## 8. Characteristics

**Table 8. Characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | 100 | - | - | V |
| | | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = -55 °C | | 90 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = 25 °C; Fig. 10; Fig. 11 | | 2.4 | 3 | 4 | V |
| | | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = 175 °C; Fig. 10 | | 1 | - | - | V |
| | | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = -55 °C; Fig. 10 | | - | - | 4.5 | V |
| $I_{DSS}$ | drain leakage current | $V_{DS}$ = 100 V; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | - | 0.02 | 1 | µA |
| | | $V_{DS}$ = 100 V; $V_{GS}$ = 0 V; $T_j$ = 100 °C | | - | - | 20 | µA |

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{GSS}$ | gate leakage current | $V_{GS}$ = 20 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | | - | 2 | 100 | nA |
| | | $V_{GS}$ = -20 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | | - | 2 | 100 | nA |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 10 A; $T_j$ = 25 °C; Fig. 12; Fig. 13 | | 4.5 | 6.4 | 8.5 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 10 A; $T_j$ = 100 °C; Fig. 13 | | - | 11.18 | 14.9 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 10 A; $T_j$ = 175 °C; Fig. 13 | | - | 16.95 | 22.6 | mΩ |
| $R_G$ | internal gate resistance (AC) | f = 1 MHz | | 0.36 | 0.71 | 1.42 | Ω |
| **Dynamic characteristics** | | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D$ = 10 A; $V_{DS}$ = 50 V; $V_{GS}$ = 10 V; Fig. 14; Fig. 15 | | - | 100 | - | nC |
| $Q_{GS}$ | gate-source charge | | | - | 19 | - | nC |
| $Q_{GS(th)}$ | pre-threshold gate-source charge | | | - | 14 | - | nC |
| $Q_{GS(th-pl)}$ | post-threshold gate-source charge | | | - | 5 | - | nC |
| $Q_{GD}$ | gate-drain charge | | | - | 30 | - | nC |
| $V_{GS(pl)}$ | gate-source plateau voltage | $I_D$ = 10 A; $V_{DS}$ = 50 V; Fig. 14; Fig. 15 | | - | 4 | - | V |
| $C_{iss}$ | input capacitance | $V_{DS}$ = 50 V; $V_{GS}$ = 0 V; f = 1 MHz; $T_j$ = 25 °C; Fig. 16; Fig. 17 | | - | 5512 | - | pF |
| $C_{oss}$ | output capacitance | $V_{DS}$ = 50 V; $V_{GS}$ = 0 V; f = 1 MHz; $T_j$ = 25 °C; Fig. 16 | | - | 380 | - | pF |
| $C_{rss}$ | reverse transfer capacitance | $V_{DS}$ = 50 V; $V_{GS}$ = 0 V; f = 1 MHz; $T_j$ = 25 °C; Fig. 16; Fig. 17 | | - | 256 | - | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS}$ = 50 V; $R_L$ = 5 Ω; $V_{GS}$ = 10 V; $R_{G(ext)}$ = 5 Ω; $T_j$ = 25 °C | | - | 21.5 | - | ns |
| $t_r$ | rise time | | | - | 30 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | | - | 83 | - | ns |
| $t_f$ | fall time | | | - | 40 | - | ns |
| **Source-drain diode** | | | | | | | |
| $V_{SD}$ | source-drain voltage | $I_S$ = 10 A; $V_{GS}$ = 0 V; $T_j$ = 25 °C; Fig. 18 | | - | 0.77 | 1.2 | V |
| $t_{rr}$ | reverse recovery time | $I_S$ = 10 A; $dI_S/dt$ = -100 A/μs; $V_{GS}$ = 0 V; $V_{DS}$ = 50 V | | - | 53 | - | ns |
| $Q_r$ | recovered charge | | | - | 124 | - | nC |




$T_j$ = 25 °C; $t_p$ = 300 µs

**Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values**

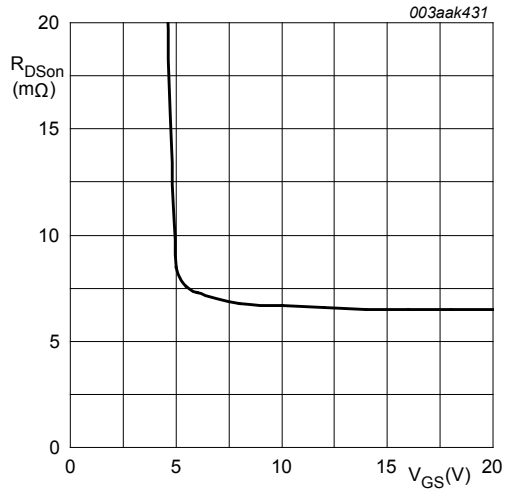



**Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values**

$T_j = 25°C;\ I_D = 10A$

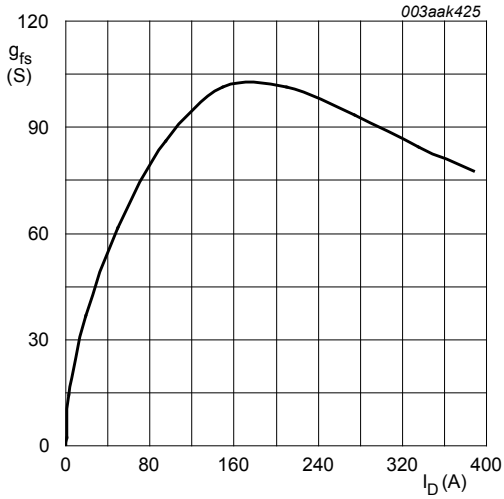



**Fig. 8. Forward transconductance as a function of drain current; typical values**

$T_j = 25°C;\ V_{DS} = 10V$

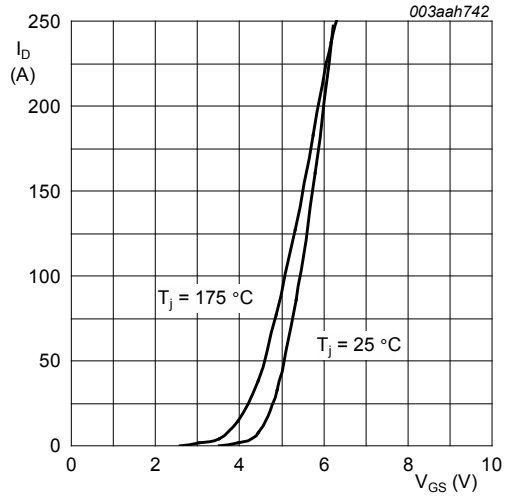



**Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values**

$V_{DS} = 10V$

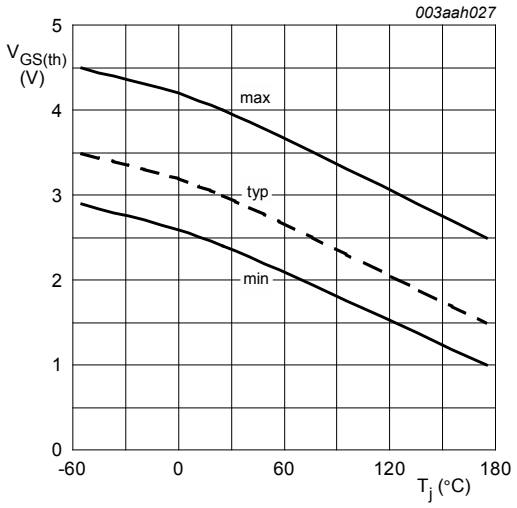



**Fig. 10. Gate-source threshold voltage as a function of junction temperature**

$I_D = 1\ \text{mA};\ V_{DS} = V_{GS}$

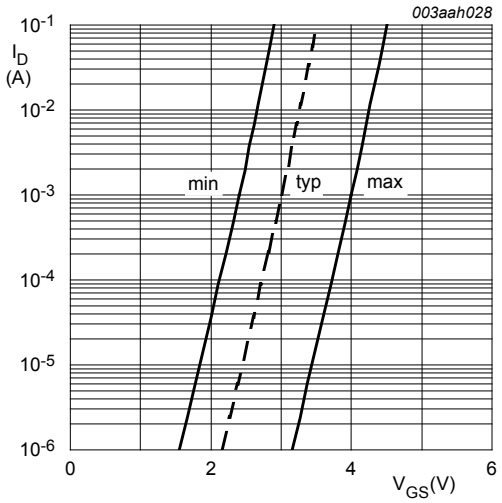



**Fig. 11. Sub-threshold drain current as a function of gate-source voltage**

$T_j = 25°C;\ V_{DS} = 5V$

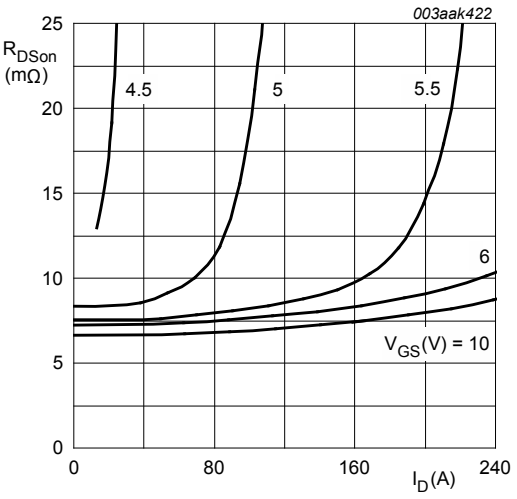



**Fig. 12. Drain-source on-state resistance as a function of drain current; typical values**

$T_j = 25°C$

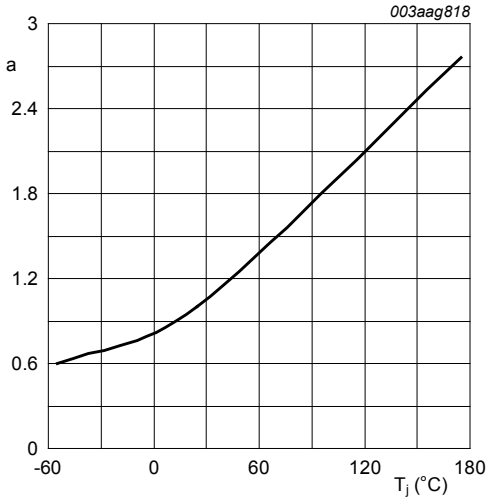



**Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature**

$$a = \frac{R_{DSon}}{R_{DSon(25\,°C)}}$$

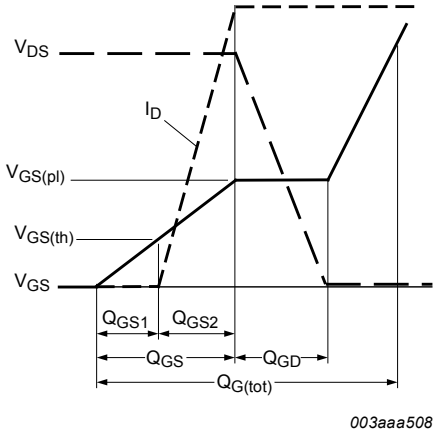



Fig. 14. Gate charge waveform definitions

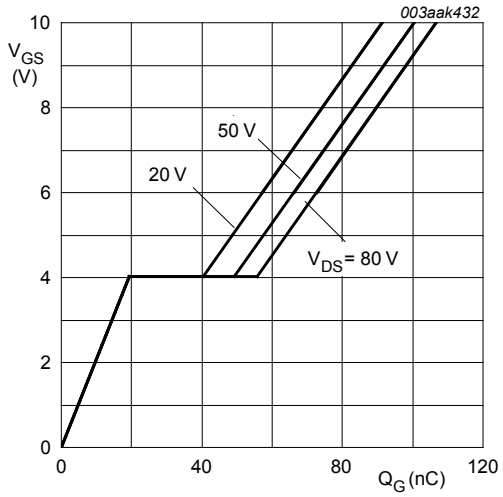



Fig. 15. Gate-source voltage as a function of gate charge; typical values

$T_j = 25°C;\ I_D = 10A$

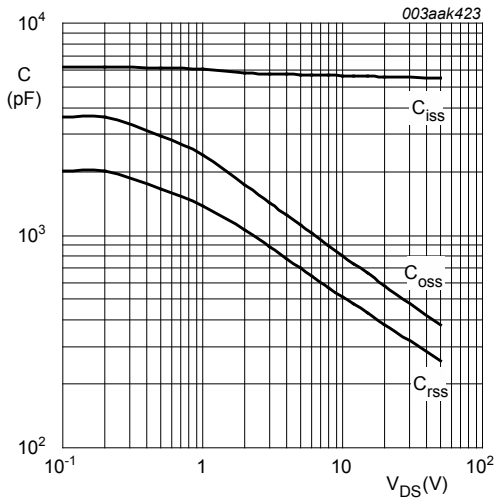



Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0V;\ f = 1MHz$

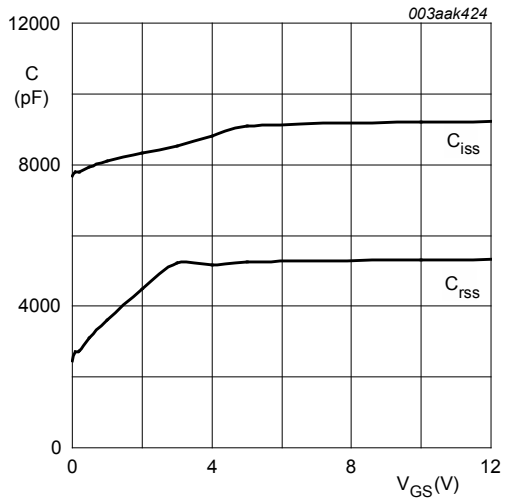



Fig. 17. Input and reverse transfer capacitances as a function of gate-source voltage, typical values

f = 1 MHz; $V_{DS} = 0$ V

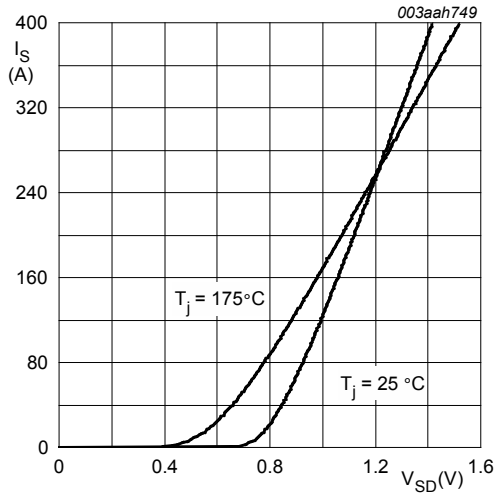


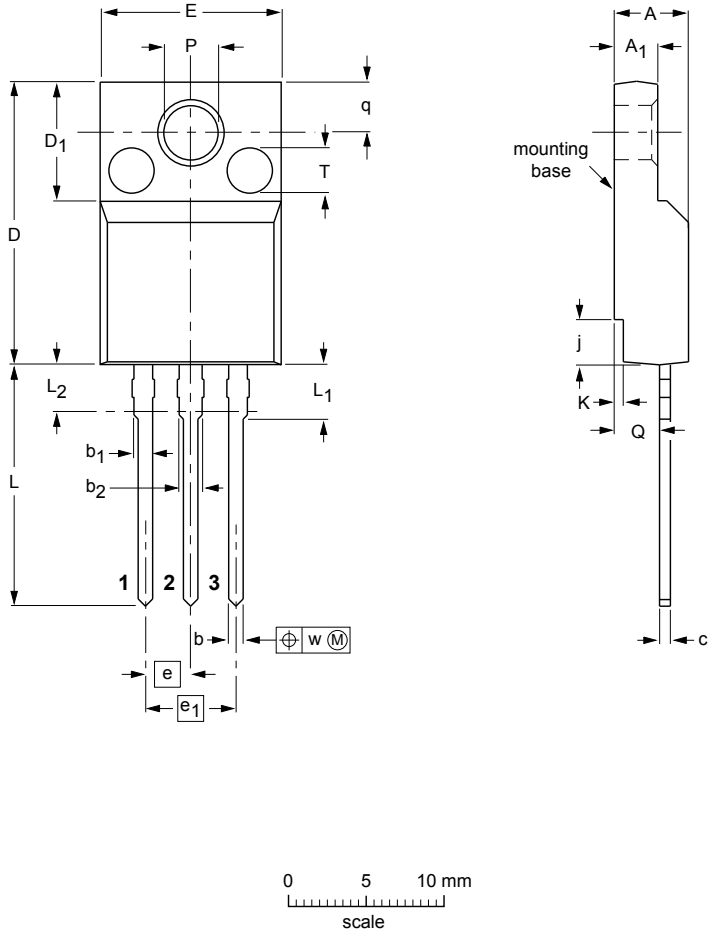

**Fig. 18. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values**

$V_{GS} = 0V$

## 9. Package outline

**Plastic single-ended package; isolated heatsink mounted;**
**1 mounting hole; 3-lead TO-220 'full pack'**

**SOT186A**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ | b | $b_1$ | $b_2$ | c | D | $D_1$ | E | e | $e_1$ | j | K | L | $L_1$ | $L_2$ (1) max. | P | Q | q | T (2) | w |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.6<br>4.0 | 2.9<br>2.5 | 0.9<br>0.7 | 1.1<br>0.9 | 1.4<br>1.0 | 0.7<br>0.4 | 15.8<br>15.2 | 6.5<br>6.3 | 10.3<br>9.7 | 2.54 | 5.08 | 2.7<br>1.7 | 0.6<br>0.4 | 14.4<br>13.5 | 3.30<br>2.79 | 3 | 3.2<br>3.0 | 2.6<br>2.3 | 3.0<br>2.6 | 2.5 | 0.4 |

**Notes**

1. Terminal dimensions within this zone are uncontrolled.
2. Both recesses are # 2.5 × 0.8 max. depth

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT186A | | 3-lead TO-220F | | | | ~~02-04-09~~<br>06-02-14 |

**Fig. 19. Package outline TO-220F (SOT186A)**

# 10. Legal information

## 10.1 Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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