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[TLC59482DBQR](#)

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16-Channel, 16-Bit, PWM LED Driver with 6-Bit Global Brightness Control

Check for Samples: [TLC59482](#)

FEATURES

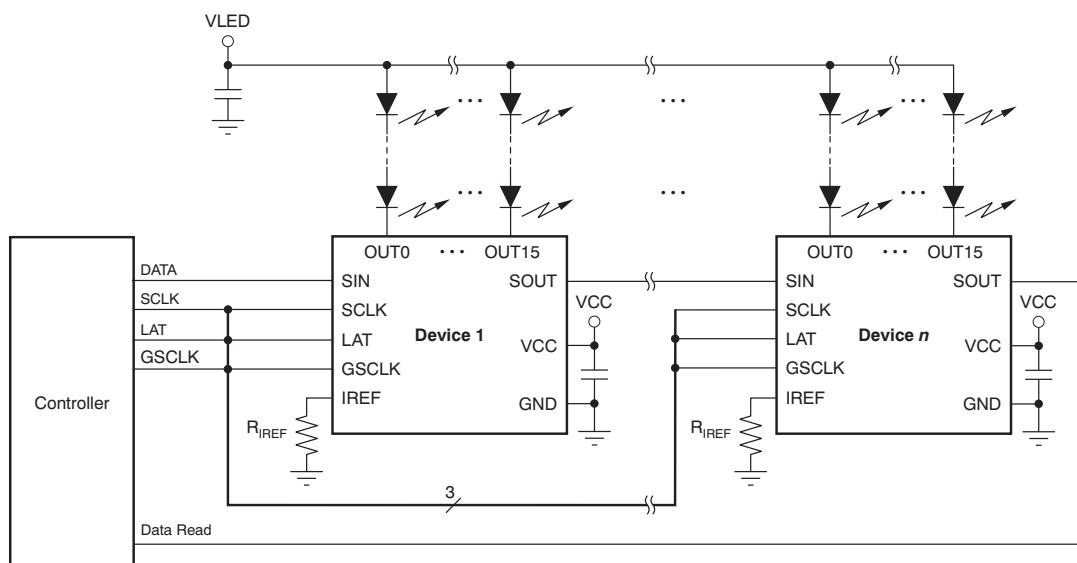
- 16 Constant-Current Sink Output Channels
- Sink Current Capability with Max BC Data:
 - 1 mA to 35 mA ($V_{CC} \leq 3.6$ V)
 - 1 mA to 45 mA ($V_{CC} > 3.6$ V)
- Global Brightness Control (BC):
 - 6-Bit (64 Steps) with 0% to 100% Range (default is 50%)
- LED Power-Supply Voltage: Up to 10 V
- VCC: 3.0 V to 5.5 V
- Constant-Current Accuracy:
 - Channel-to-Channel: $\pm 1\%$ (typ), $\pm 2.5\%$ (max)
 - Device-to-Device: $\pm 2\%$ (typ), $\pm 4\%$ (max)
- Data Transfer Rate: 30 MHz
- Grayscale Control Clock: 33 MHz
- Auto Display Repeat
- Auto Data Refresh
- Display Timing Reset
- Four-Channel Grouped Delay Switching to Prevent Inrush Current
- Operating Temperature: -40°C to $+85^{\circ}\text{C}$

APPLICATIONS

- LED Video Displays
- LED Signboards

DESCRIPTION

The TLC59482 is a 16-channel, constant-current sink driver. Each channel has an individually-adjustable, pulse width modulation (PWM) grayscale (GS) brightness control with 65,536 steps. All channels have a 64-step global brightness control (BC). BC adjusts brightness deviation with other LED drivers. GS and BC data are accessible via a serial interface port.



Typical Application Circuit (Multiple Daisy-Chained TLC59482s)



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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

 ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

| PRODUCT | PACKAGE DESIGNATOR | ORDERING NUMBER | TRANSPORT MEDIA, QUANTITY |
|----------|--------------------|-----------------|---------------------------|
| TLC59482 | DBQ | TLC59482DBQR | Tape and Reel, 2500 |
| | | TLC59482DBQ | Tube, 50 |
| | RGE ⁽²⁾ | TLC59482RGER | Tape and Reel, 3000 |
| | | TLC59482RGET | Tape and Reel, 250 |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

(2) Product preview device.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over operating free-air temperature range, unless otherwise noted.

| | | VALUE | | UNIT |
|---------------------------------------|---------------------------------|-------|----------------|------|
| | | MIN | MAX | |
| Voltage ⁽²⁾ | VCC | -0.3 | +6 | V |
| | SIN, SCLK, LAT, GSCLK, IREF | -0.3 | $V_{CC} + 0.3$ | V |
| | SOUT | -0.3 | $V_{CC} + 0.3$ | V |
| | OUT0 to OUT15 | -0.3 | +11 | V |
| Current | I_{OUT} (dc), OUT0 to OUT15 | | +55 | mA |
| Temperature | Operating junction, T_J (max) | | +150 | °C |
| | Storage, T_{stg} | -55 | +150 | °C |
| Electrostatic discharge (ESD) ratings | Human body model (HBM) | | 3000 | V |
| | Charged device model (CDM) | | 2000 | V |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to device ground terminal.

THERMAL INFORMATION

| THERMAL METRIC ⁽¹⁾ | TLC59482 | | UNITS |
|-------------------------------|--|-----------|-------|
| | DBQ (SSOP, QSOP) | RGE (QFN) | |
| | 24 PINS | 24 PINS | |
| θ_{JA} | Junction-to-ambient thermal resistance | 86.7 | 35.5 |
| θ_{JCtop} | Junction-to-case (top) thermal resistance | 50.4 | 44 |
| θ_{JB} | Junction-to-board thermal resistance | 10.0 | 14.7 |
| Ψ_{JT} | Junction-to-top characterization parameter | 13.0 | 0.4 |
| Ψ_{JB} | Junction-to-board characterization parameter | 39.7 | 14.8 |
| θ_{JCbot} | Junction-to-case (bottom) thermal resistance | N/A | 2.9 |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](http://www.ti.com).

RECOMMENDED OPERATING CONDITIONS

At $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|--------------------------------------|--|---------------------|---------------------|------------------|
| DC CHARACTERISTICS ($V_{CC} = 3\text{ V}$ to 5.5 V) | | | | | |
| V_{CC} | Supply voltage | | 3.0 | 5.5 | V |
| V_O | Voltage applied to output | OUT0 to OUT15 | | 10 | V |
| V_{IH} | High-level input voltage | SIN, SCLK, LAT, GSCLK | $0.7 \times V_{CC}$ | V_{CC} | V |
| V_{IL} | Low-level input voltage | SIN, SCLK, LAT, GSCLK | GND | $0.3 \times V_{CC}$ | V |
| I_{OH} | High-level output current | SOUT | | -2 | mA |
| I_{OL} | Low-level output current | SOUT | | 2 | mA |
| I_{OLC} | Constant output sink current | OUT0 to OUT15, $3\text{ V} \leq V_{CC} \leq 3.6\text{ V}$ | | 35 | mA |
| | | OUT0 to OUT15, $3.6\text{ V} < V_{CC} \leq 5.5\text{ V}$ | | 45 | mA |
| T_A | Operating free-air temperature range | | -40 | +85 | $^\circ\text{C}$ |
| T_J | Operating junction temperature range | | -40 | +125 | $^\circ\text{C}$ |
| AC CHARACTERISTICS ($V_{CC} = 3\text{ V}$ to 5.5 V) | | | | | |
| V_{CC} | Supply voltage | | 3.0 | 5.5 | V |
| f_{CLK} (SCLK) | Data shift clock frequency | SCLK, $3.0\text{ V} \leq V_{CC} \leq 3.6\text{ V}$ | | 25 | MHz |
| | | SCLK, $3.6\text{ V} < V_{CC} \leq 5.5\text{ V}$ | | 30 | MHz |
| f_{CLK} (GSCLK) | Grayscale control clock frequency | GSCLK | | 33 | MHz |
| t_{WH0} | Pulse duration | SCLK | 10 | | ns |
| t_{WL0} | | SCLK | 10 | | ns |
| t_{WH1} | | GSCLK | 10 | | ns |
| t_{WL1} | | GSCLK | 10 | | ns |
| t_{WH2} | | LAT | 10 | | ns |
| t_{SU0} | Setup time | SIN to SCLK \uparrow | 4 | | ns |
| t_{SU1} | | LAT \uparrow to SCLK \uparrow | 2 | | ns |
| t_{SU2} | | LAT \downarrow to SCLK $\uparrow^{(1)}$ | 5 | | ns |
| t_{H0} | Hold time | SCLK \uparrow to SIN | 4 | | ns |
| t_{H1} | | SCLK \uparrow to LAT \uparrow | 7 | | ns |
| t_{H2} | | SCLK \uparrow to LAT \downarrow | 14 | | ns |
| t_{H3} | | LAT \downarrow to GSCLK \uparrow | 30 | | ns |

(1) Refer to the t_{D1} parameter in the [Switching Characteristics](#) table for the FC data read time.

ELECTRICAL CHARACTERISTICS

At $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ and $V_{CC} = 3\text{ V}$ to 5.5 V , unless otherwise noted. Typical values are at $T_A = +25^\circ\text{C}$ and $V_{CC} = 3.3\text{ V}$.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|-------------------|---|--|----------------------------------|-----------|-------------|---------------|
| V_{OH} | High-level output voltage (SOUT) | $I_{OH} = -2\text{ mA}$ | $V_{CC} - 0.4$ | V_{CC} | V | |
| V_{OL} | Low-level output voltage (SOUT) | $I_{OL} = 2\text{ mA}$ | | 0.4 | V | |
| V_{REF} | Reference voltage output | $R_{REF} = 1.5\text{ k}\Omega$ | 1.175 | 1.200 | 1.225 | V |
| I_{IN} | Input current (SIN, SCLK, GSCLK) | $V_{IN} = V_{CC}$ or GND | | -1 | 1 | μA |
| I_{CC0} | Supply current (V_{CC}) | SIN, SCLK, LAT, GSCLK = GND, GS n = 0000h, BC = 3Fh, $V_{OUTn} = 0.8\text{ V}$, R_{REF} = open | | 1.5 | 3 | mA |
| I_{CC1} | | SIN, SCLK, LAT, GSCLK = GND, GS n = 0000h, BC = 3Fh, $V_{OUTn} = 0.8\text{ V}$, $R_{REF} = 3\text{ k}\Omega$ ($I_{OUTn} = 15.9\text{-mA target}$) | | 3 | 5 | mA |
| I_{CC2} | | SIN, SCLK, LAT = GND, GSCLK = 33 MHz, GS n = FFFFh, BC = 3Fh, $V_{OUTn} = 0.8\text{ V}$, $R_{REF} = 3\text{ k}\Omega$ ($I_{OUT} = 15.9\text{-mA target}$) | | 8 | 10 | mA |
| I_{CC3} | | SIN, SCLK, LAT = GND, GSCLK = 33 MHz, GS n = FFFFh, BC = 3Fh, $V_{OUTn} = 0.8\text{ V}$, $R_{REF} = 1.5\text{ k}\Omega$ ($I_{OUT} = 31.8\text{-mA target}$) | | 9 | 13.5 | mA |
| I_{OLC} | Constant output sink current (OUT0 to OUT15) | All OUT n = on, BC = 3Fh, $V_{OUTn} = V_{OUTfix} = 0.8\text{ V}$, $R_{REF} = 1.5\text{ k}\Omega$, $T_A = +25^\circ\text{C}$ ($I_{OLCn} = 31.8\text{-mA target}$) | 29.8 | 31.8 | 33.8 | mA |
| I_{OLKG0} | Output leakage current (OUT0 to OUT15) | All OUT n = off, GS n = 0000h, $V_{OUTn} = V_{OUTfix} = 10\text{ V}$, $R_{REF} = 1.5\text{ k}\Omega$ ($I_{OLCn} = 31.8\text{-mA target}$) | $T_J = +25^\circ\text{C}$ | | 0.1 | μA |
| I_{OLKG1} | | | $T_J = +85^\circ\text{C}^{(1)}$ | | 0.2 | μA |
| I_{OLKG2} | | | $T_J = +125^\circ\text{C}^{(1)}$ | | 0.3 | μA |
| ΔI_{OLC0} | Constant-current error, channel-to-channel (OUT0 to OUT15) ⁽²⁾ | All OUT n = on, BC = 3Fh, $V_{OUTn} = V_{OUTfix} = 0.8\text{ V}$, $R_{REF} = 1.5\text{ k}\Omega$, $T_A = +25^\circ\text{C}$ ($I_{OUTn} = 31.8\text{-mA target}$) | | $\pm 1\%$ | $\pm 2.5\%$ | |
| ΔI_{OLC1} | Constant-current error, device-to-device (OUT0 to OUT15) ⁽³⁾ | All OUT n = on, BC = 3Fh, $V_{OUTn} = V_{OUTfix} = 0.8\text{ V}$, $R_{REF} = 1.5\text{ k}\Omega$, $T_A = +25^\circ\text{C}$ ($I_{OUTn} = 31.8\text{-mA target}$) | | $\pm 2\%$ | $\pm 4\%$ | |
| ΔI_{OLC2} | Line regulation (OUT0 to OUT15) ⁽⁴⁾ | $V_{CC} = 3.0\text{ V}$ to 5.5 V , all OUT n = on, BC = 3Fh, $V_{OUTn} = V_{OUTfix} = 0.8\text{ V}$, $R_{REF} = 1.5\text{ k}\Omega$ ($I_{OUTn} = 31.8\text{-mA target}$) | | ± 1 | ± 3 | %/V |
| ΔI_{OLC3} | Load regulation (OUT0 to OUT15) ⁽⁵⁾ | All OUT n = on, BC = 3Fh, $V_{OUTn} = 0.8\text{ V}$ to 3.0 V , $V_{OUTfix} = 0.8\text{ V}$, $R_{REF} = 1.5\text{ k}\Omega$ ($I_{OUTn} = 31.8\text{-mA target}$) | | ± 1 | ± 3 | %/V |
| R_{PDWN} | Pull-down resistor | LAT | 250 | 500 | 750 | k Ω |

(1) Not tested; specified by design.

(2) The deviation of each output from the average of OUT0 to OUT15 constant-current. Deviation is calculated by the formula:

$$\Delta (\%) = \left\{ \frac{\frac{I_{OLCn}}{16} - 1}{\frac{I_{OLC0} + I_{OLC1} + \dots + I_{OLC14} + I_{OLC15}}{16}} \right\} \times 100$$

where $n = 0$ to 15.

(3) The deviation of the OUT n output current value from the ideal constant-current value. Deviation is calculated by the formula:

$$\Delta (\%) = \left\{ \frac{\frac{(I_{OLC0} + I_{OLC1} + \dots + I_{OLC14} + I_{OLC15})}{16} - \text{Ideal Output Current}}{\text{Ideal Output Current}} \right\} \times 100$$

Ideal current is calculated by the formula:

$$I_{OLCn(\text{IDEAL})} (\text{mA}) = 39.8 \times \left(\frac{1.20}{R_{REF} (\Omega)} \right)$$

where $n = 0$ to 15.

(4) Line regulation is calculated by the formula:

$$\Delta (\%/\text{V}) = \left\{ \frac{(I_{OLCn} \text{ at } V_{CC} = 5.5\text{ V}) - (I_{OLCn} \text{ at } V_{CC} = 3.0\text{ V})}{I_{OLCn} \text{ at } V_{CC} = 3.0\text{ V}} \right\} \times \frac{100}{5.5\text{ V} - 3\text{ V}}$$

where $n = 0$ to 15.

(5) Load regulation is calculated by the equation:

$$\Delta (\%/\text{V}) = \left\{ \frac{(I_{OLCn} \text{ at } V_{OUTn} = 3\text{ V}) - (I_{OLCn} \text{ at } V_{OUTn} = 0.8\text{ V})}{I_{OLCn} \text{ at } V_{OUTn} = 0.8\text{ V}} \right\} \times \frac{100}{3\text{ V} - 0.8\text{ V}}$$

where $n = 0$ to 15.

SWITCHING CHARACTERISTICS

At $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 3\text{ V}$ to 5.5 V , $C_L = 15\text{ pF}$, $R_L = 110\text{ }\Omega$, $R_{REF} = 1.5\text{ k}\Omega$, and $V_{LED} = 5.0\text{ V}$, unless otherwise noted. Typical values are at $T_A = +25^\circ\text{C}$ and $V_{CC} = 3.3\text{ V}$.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------|-------------------------------------|---|-----|-----|-----|------|
| t_{R0} | Rise time | SOUT | | 1.5 | 5 | ns |
| t_{R1} | | OUTn, BC = 7Fh, $T_A = +25^\circ\text{C}$ | | 30 | | ns |
| t_{F0} | Fall time | SOUT | | 1.5 | 5 | ns |
| t_{F1} | | OUTn, BC = 7Fh, $T_A = +25^\circ\text{C}$ | | 30 | | ns |
| t_{D0} | Propagation delay | SCLK \uparrow to SOUT $\uparrow\downarrow$ | | 23 | 35 | ns |
| t_{D1} | | LAT \downarrow to SOUT $\uparrow\downarrow$ | | 27 | 42 | ns |
| t_{D2} | | GSCLK \uparrow to OUT0, OUT7, OUT8, OUT15 on/off with BC = 7Fh, $T_A = +25^\circ\text{C}$ | | 50 | | ns |
| t_{D3} | | GSCLK \uparrow to OUT1, OUT6, OUT9, OUT14 on/off with BC = 7Fh, $T_A = +25^\circ\text{C}$ | | 55 | | ns |
| t_{D4} | | GSCLK \uparrow to OUT2, OUT5, OUT10, OUT13 on/off with BC = 7Fh, $T_A = +25^\circ\text{C}$ | | 60 | | ns |
| t_{D5} | | GSCLK \uparrow to OUT3, OUT4, OUT11, OUT12 on/off with BC = 7Fh, $T_A = +25^\circ\text{C}$ | | 65 | | ns |
| t_{ON_ERR} | Output on-time error ⁽¹⁾ | $t_{OUT_ON} - t_{GSCLK}$, GS $n = 0001\text{h}$, GSCLK = 20 MHz, BC = 3Fh, $V_{CC} = 3.3\text{ V}$, $T_A = +25^\circ\text{C}$ | -35 | | 10 | ns |

- (1) Output on-time error (t_{ON_ERR}) is calculated by the formula: $t_{ON_ERR} = t_{OUT_ON} - t_{GSCLK}$. t_{OUT_ON} is the actual on-time of the constant-current driver. t_{GSCLK} is the GSCLK period.

PARAMETER MEASUREMENT INFORMATION

PIN-EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

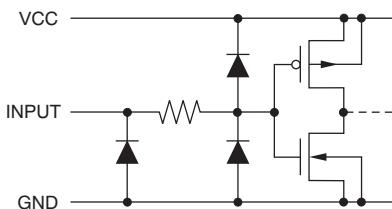


Figure 1. SIN, SCLK, and GSCLK

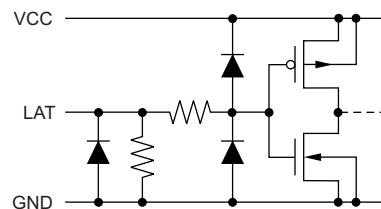


Figure 2. LAT

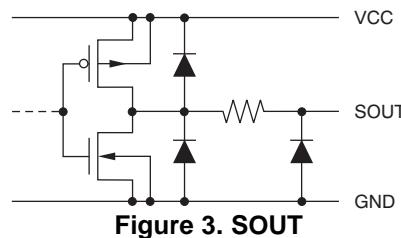


Figure 3. SOUT

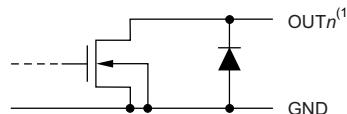
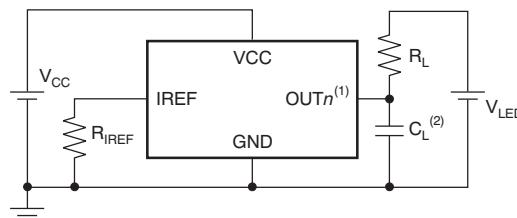


Figure 4. OUT0 Through OUT15

(1) $n = 0$ to 15.

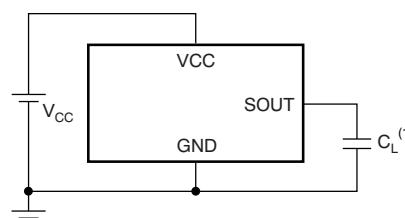
TEST CIRCUITS



(1) $n = 0$ to 15.

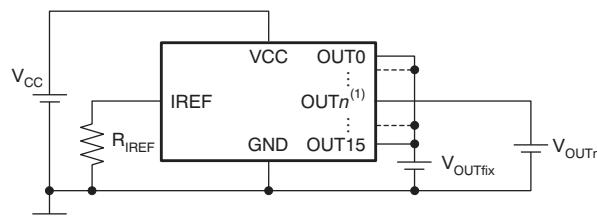
(2) C_L includes measurement probe and jig capacitance.

Figure 5. Rise Time and Fall Time Test Circuit for OUTn



(1) C_L includes measurement probe and jig capacitance.

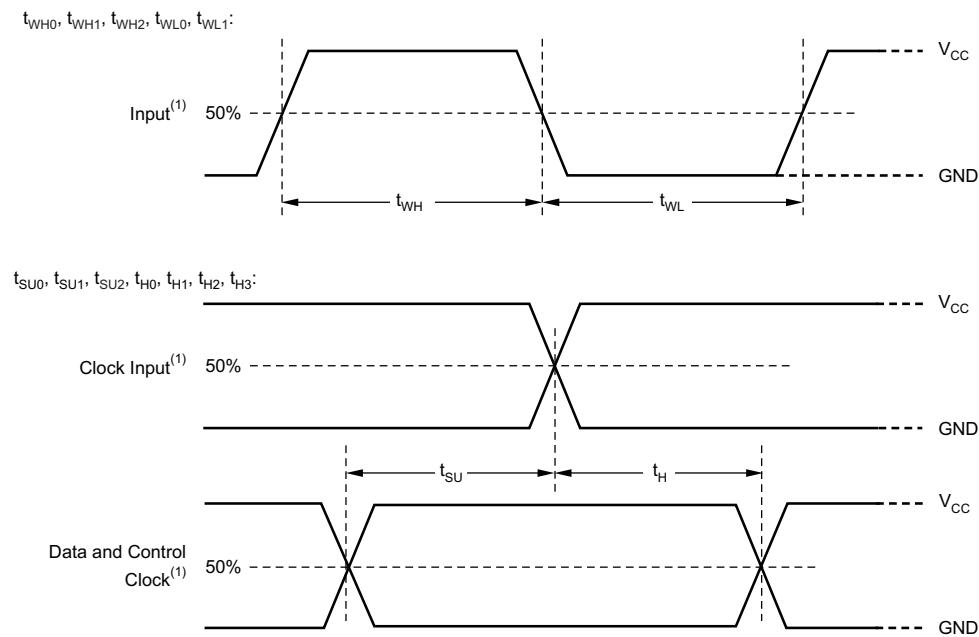
Figure 6. Rise Time and Fall Time Test Circuit for SOUT



(1) $n = 0$ to 15.

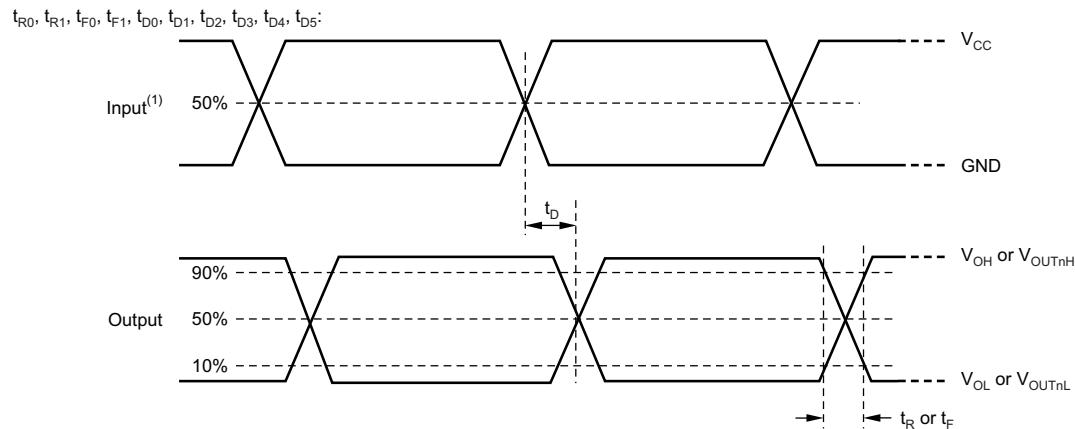
Figure 7. Constant-Current Test Circuit for OUTn

TIMING DIAGRAMS



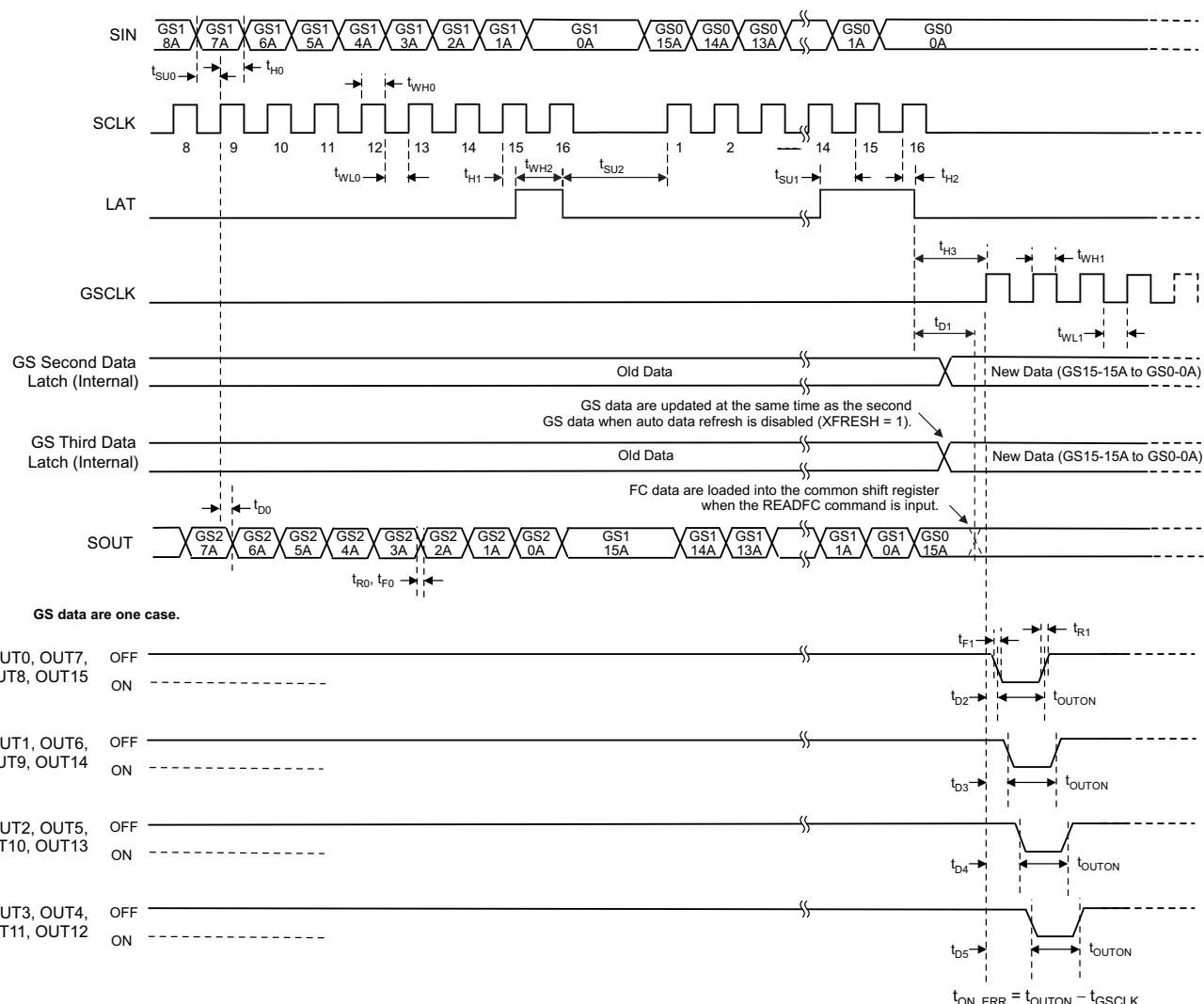
(1) Input pulse rise and fall time is 1 ns to 3 ns.

Figure 8. Input Timing



(1) Input pulse rise and fall time is 1 ns to 3 ns.

Figure 9. Output Timing

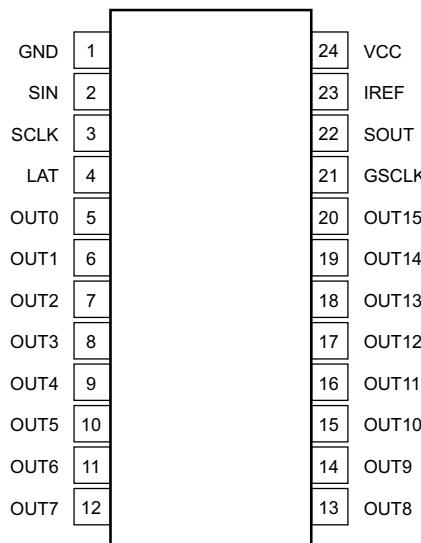


(1) NV = Not valid; these data are not used for any function.

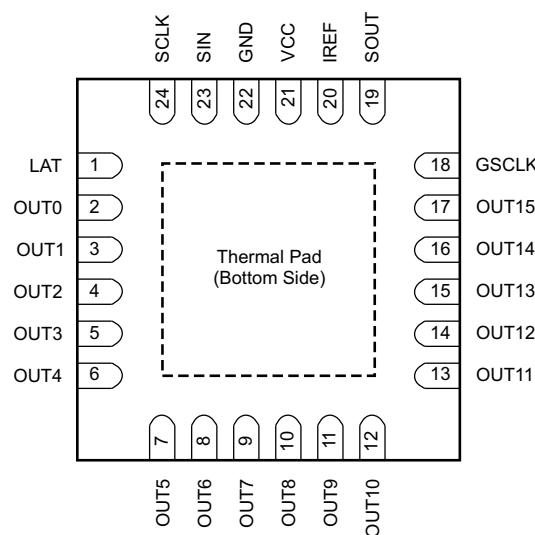
Figure 10. Timing Diagram

PIN CONFIGURATIONS

DBQ PACKAGE
SSOP-24, QSOP-24
(Top View)



RGE PACKAGE
QFN-24
(Top View)

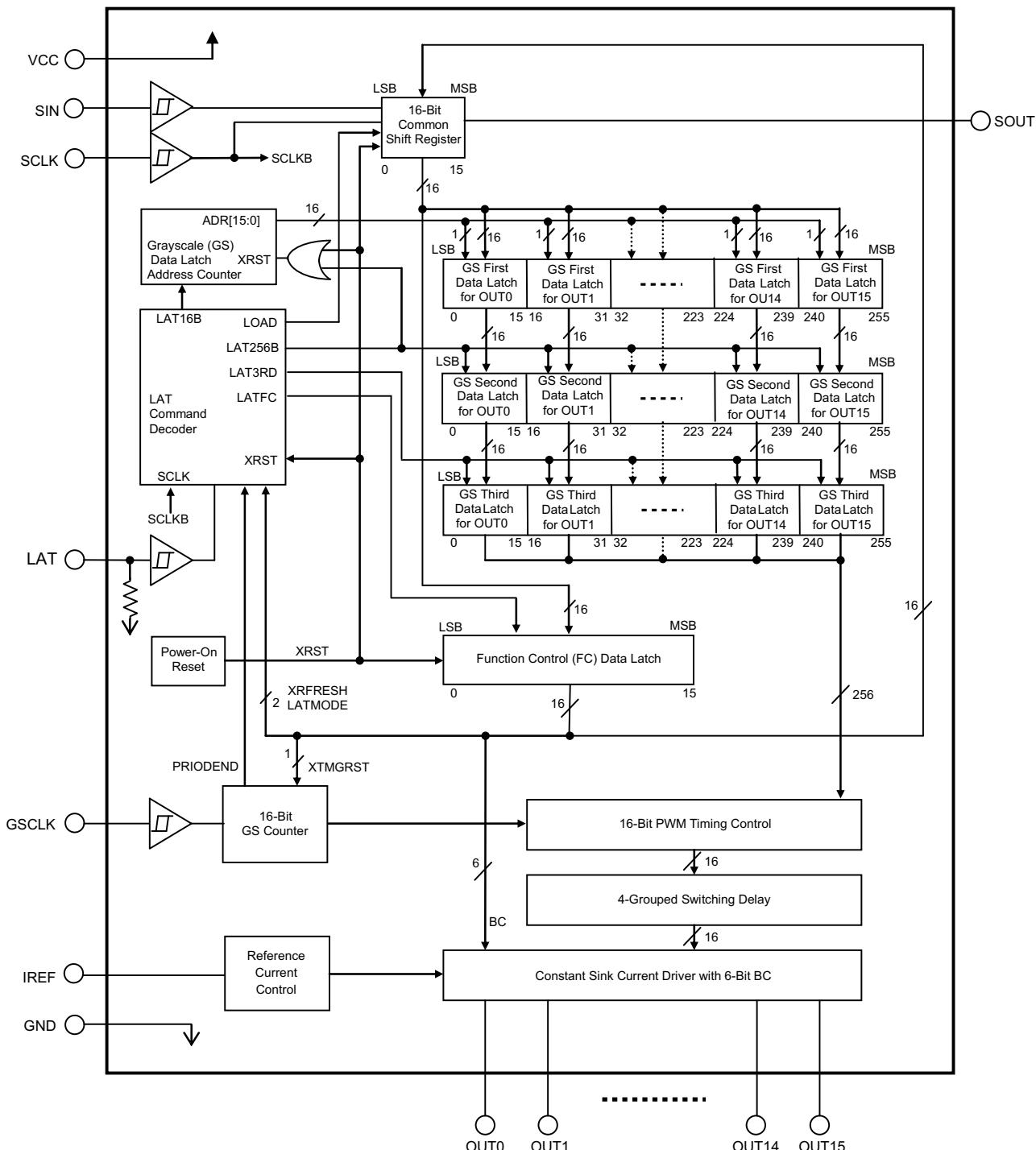


NOTE: The thermal pad is not internally connected to GND. The thermal pad must be connected to GND via the printed board circuit (PCB) pattern.

PIN DESCRIPTIONS

| PIN | | | I/O | DESCRIPTION |
|-------|-----|-----|-----|--|
| NAME | NO. | DBQ | | |
| GND | 1 | 22 | — | Power ground |
| GSCLK | 21 | 18 | I | Grayscale (GS) pulse width modulation (PWM) reference clock control for OUT n . Each GSCLK rising edge increments the GS counter for PWM control. When the TMGRST command is input with the TMRSTEN bit (equal to '1') in the function control data latch, all constant-current outputs (OUT0 to OUT15) are forced off and the GS counter is reset to '0'. Furthermore, all constant-current outputs are forced off and the GS counter is reset to '0' when the LATGS command is input with the XRFRESH bit (equal to '1') in the function control data latch. |
| IREF | 23 | 20 | I/O | Reference current terminal. A resistor connected between IREF to GND sets the maximum current for all constant-current outputs. |
| LAT | 4 | 1 | I | The LAT falling edge latches the data from the 16-bit common shift register into the first GS data latch for the OUT n that are selected by either the GS data address down counter, global brightness control (BC) data latch, or function control (FC) data latch. The data latch is selected by the number of input SCLK rising edges while LAT is high. This pin is internally pulled down to GND with a 500-k Ω (typ) resistor. |
| OUT0 | 5 | 2 | O | Constant-current outputs. Multiple outputs can be configured in parallel to increase the constant-current capability. Different voltages can be applied to each output. |
| OUT1 | 6 | 3 | O | |
| OUT2 | 7 | 4 | O | |
| OUT3 | 8 | 5 | O | |
| OUT4 | 9 | 6 | O | |
| OUT5 | 10 | 7 | O | |
| OUT6 | 11 | 8 | O | |
| OUT7 | 12 | 9 | O | |
| OUT8 | 13 | 10 | O | |
| OUT9 | 14 | 11 | O | |
| OUT10 | 15 | 12 | O | |
| OUT11 | 16 | 13 | O | |
| OUT12 | 17 | 14 | O | |
| OUT13 | 18 | 15 | O | |
| OUT14 | 19 | 16 | O | |
| OUT15 | 20 | 17 | O | |
| SCLK | 3 | 24 | I | Serial data shift clock. Data present on SIN are shifted to the LSB of the 16-bit common shift register with the SCLK rising edge. Data in the shift register are shifted towards the MSB at each SCLK rising edge. The MSB of the common shift register appears on SOUT. |
| SIN | 2 | 23 | I | Serial data input for the 16-bit common shift register |
| SOUT | 22 | 19 | O | Serial data output of the 16-bit common shift register. SOUT is connected to the 16-bit common shift register MSB. Data are clocked out at the SCLK rising edge. Data in the function data latch can be read from SOUT during the READFC command. |
| VCC | 24 | 21 | — | Power-supply voltage |

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, unless otherwise noted.

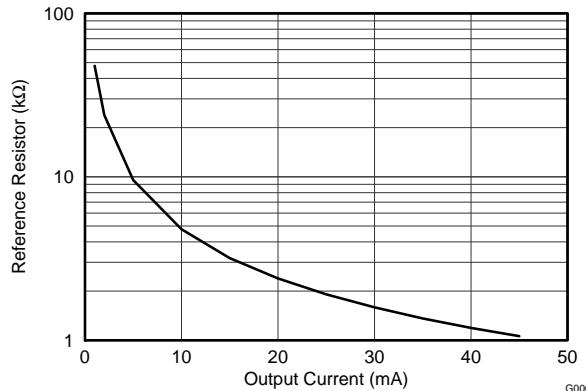


Figure 11. REFERENCE RESISTOR
vs OUTPUT CURRENT

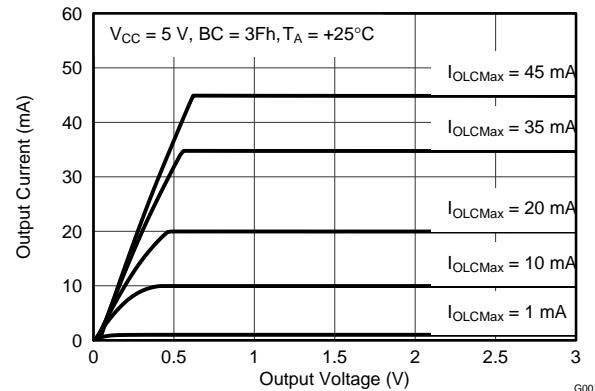


Figure 12. OUTPUT CURRENT
vs OUTPUT VOLTAGE

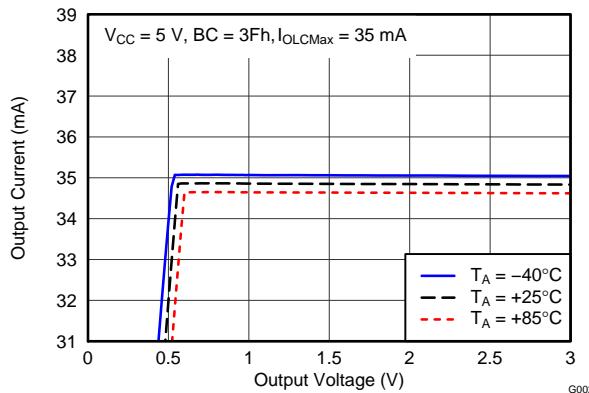


Figure 13. OUTPUT CURRENT
vs OUTPUT VOLTAGE

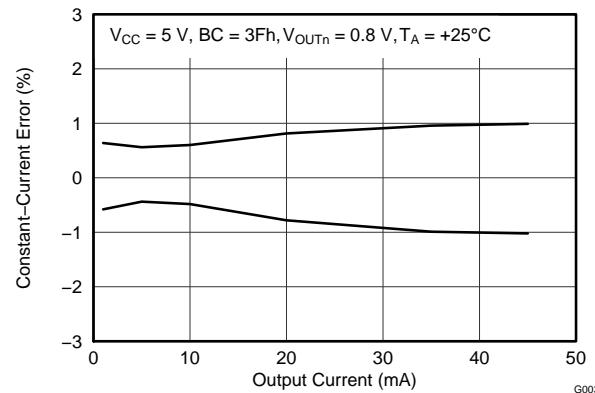


Figure 14. CONSTANT-CURRENT ERROR VS
OUTPUT CURRENT SET BY EXTERNAL RESISTOR

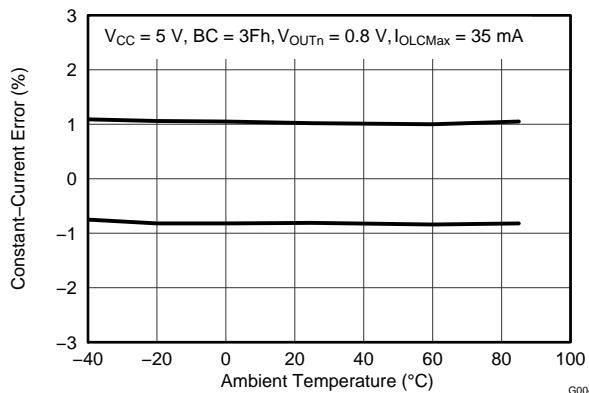


Figure 15. CONSTANT-CURRENT ERROR
vs AMBIENT TEMPERATURE

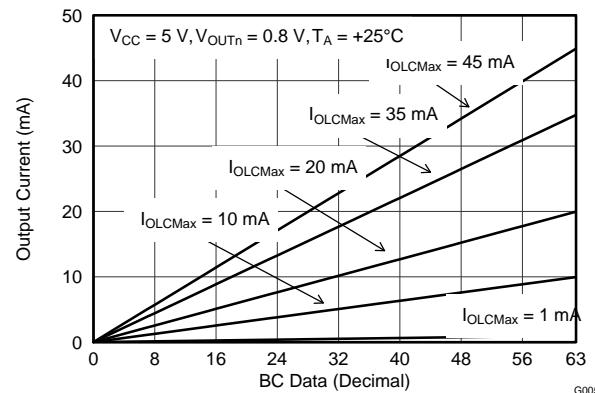
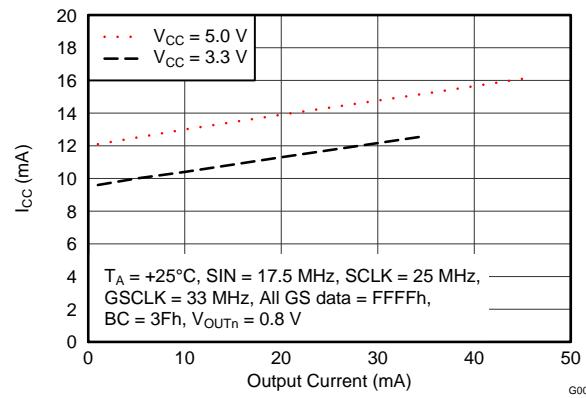


Figure 16. GLOBAL BRIGHTNESS
CONTROL LINEARITY

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, unless otherwise noted.



**Figure 17. SUPPLY CURRENT
vs OUTPUT CURRENT**

DETAILED DESCRIPTION

MAXIMUM CONSTANT SINK CURRENT VALUE

The maximum output current value of each channel (I_{OLCMax}) is programmed by a single resistor (R_{IREF}) that is placed between the IREF and GND pins. The current value can be calculated by [Equation 1](#):

$$R_{IREF} (\text{k}\Omega) = \frac{V_{IREF} (\text{V})}{I_{OLCMax} (\text{mA})} \times 39.8$$

Where:

V_{IREF} = the internal reference voltage on IREF (typically 1.20 V when the global BC data are at maximum)

I_{OLCMax} = 1 mA to 35 mA ($3 \text{ V} \leq V_{CC} \leq 3.6 \text{ V}$) or 1 mA to 45 mA ($3.6 \text{ V} < V_{CC} \leq 5.5 \text{ V}$) at OUTn and BC = 63 (1)

I_{OLCMax} is the highest current for each output. Each output sinks I_{OLCMax} current when it is turned on and the global brightness control (BC) data are set to the maximum value of 3Fh (64). Each output sink current can be reduced by lowering the BC value.

R_{IREF} must be between 1.06 k Ω and 47.8 k Ω in order to hold I_{OLCMax} between 45 mA (typ) and 1 mA (typ). Otherwise, the output may be unstable. Output currents lower than 1 mA can be achieved by setting I_{OLCMax} to 1 mA or higher and then using global BC to lower the output current.

[Table 1](#) shows the characteristics of the constant-current sink versus the external resistor, R_{IREF} .

Table 1. Maximum Constant-Current Output versus External Resistor Value

| I_{OLCMax} (mA) | I_{OLC} FOLLOWING POWER-UP (mA, BC = 32) | R_{IREF} (k Ω , typ) |
|-------------------------------------|--|-------------------------------|
| 45 ($V_{CC} > 3.6 \text{ V}$ only) | 22.5 | 1.06 |
| 40 ($V_{CC} > 3.6 \text{ V}$ only) | 20 | 1.19 |
| 35 | 17.5 | 1.37 |
| 30 | 15 | 1.59 |
| 25 | 12.5 | 1.91 |
| 20 | 10 | 2.39 |
| 15 | 7.5 | 3.18 |
| 10 | 5 | 4.78 |
| 5 | 2.5 | 9.55 |
| 1 | 0.5 | 47.8 |

GLOBAL BRIGHTNESS CONTROL (BC) FUNCTION

The TLC59482 can simultaneously adjust the output current of all constant-current outputs. This function is called *global brightness control* (BC). The global BC for all outputs (OUT0 to OUT15) is programmed with a 6-bit word. The global BC adjusts all output currents in 64 steps from 0% to 100%, where 100% corresponds to the maximum output current set by R_{IREF} . [Equation 2](#) calculates the actual output current as a function of R_{IREF} and global BC value. BC data can be set via the serial interface. When the device is powered on, the BC data in the function control (FC) data latch is set to 32 as the initial value.

The output current value controlled by BC can be calculated by [Equation 2](#).

$$I_{OUTn} (\text{mA}) = I_{OLCMax} (\text{mA}) \times \frac{BCn}{63}$$

Where:

I_{OLCMax} = the maximum constant-current value for each output determined by R_{IREF}

BC = the global brightness control value in the brightness control data latch (0 to 63) (2)

Table 2 summarizes the BC data versus the set current value.

Table 2. BC Data versus Constant-Current Ratio and Set Current Value

| BC DATA | | | RATIO OF OUTPUT CURRENT TO $I_{OLCMax}(\%)$ | I_{OUT} (mA) ($I_{OLCMax} = 45$ mA, typ) | I_{OUT} (mA) ($I_{OLCMax} = 1$ mA, typ) |
|-------------------|--------------|--------------|---|---|--|
| BINARY | DECIMAL | HEX | | | |
| 00 0000 | 0 | 00 | 0 | 0 | 0 |
| 00 0001 | 1 | 01 | 1.6 | 0.71 | 0.02 |
| 00 0010 | 2 | 02 | 3.2 | 1.43 | 0.03 |
| — | — | — | — | — | — |
| 01 1111 | 31 | 1F | 49.2 | 22.14 | 0.49 |
| 10 0000 (default) | 32 (default) | 20 (default) | 50.8 | 22.86 | 0.51 |
| 10 0001 | 33 | 21 | 52.4 | 23.57 | 0.52 |
| — | — | — | — | — | — |
| 11 1101 | 61 | 3D | 96.8 | 43.57 | 0.97 |
| 11 1110 | 62 | 3E | 98.4 | 44.29 | 0.98 |
| 11 1111 | 63 | 3F | 100.0 | 45.00 | 1.00 |

GRAYSCALE (GS) FUNCTION (PWM CONTROL)

The TLC59482 can adjust the brightness of each output channel using a pulse width modulation (PWM) control scheme. The architecture of 16 bits per channel results in 65,536 brightness steps, from 0% up to 100% brightness.

The PWM operation is controlled by the grayscale (GS) counter based on the GS data in the third GS data latch. The GS counter increments on each rising edge of the grayscale reference clock (GSCLK). When the TMGRST command is input with the TMRSTEN bit (equal to '1') of the function control data latch, or when the LATGS command is input with the XRFRESH bit (equal to '1') of the function control data latch, all constant-current outputs (OUT0 to OUT15) are forced off, the GS counter is reset to '0', and the GS PWM timing controller is initialized.

The on-time (t_{OUT_ON}) of each output (OUT n) can be calculated by [Equation 3](#).

$$t_{OUT_ON} (\text{ns}) = t_{GSCLK} \times GS_n$$

where:

t_{GSCLK} is on GS clock period

GS_n is the programmed GS value for OUT n (0 to 65535)

(3)

Table 3 summarizes the GS data values versus the output on-time duty cycle in a 16-bit length PWM. When the device powers up, all outputs are forced off and do not turn on until the 256-bit GS data are written to the third data latch even if GSCLK is input.

Table 3. Output Duty Cycle and On-Time versus GS Data (16-Bit PWM Bit Length)

| GS DATA | | ON-TIME RATE vs MAX GS (%) | GS DATA | | ON-TIME RATE vs MAX GS (%) |
|---------|------|-------------------------------|---------|------|-------------------------------|
| DECIMAL | HEX | | DECIMAL | HEX | |
| 0 | 0 | 0 | 32768 | 8000 | 50.001 |
| 1 | 1 | 0.002 | 32769 | 8001 | 50.002 |
| 2 | 2 | 0.003 | 32770 | 8002 | 50.004 |
| 3 | 3 | 0.005 | 32771 | 8003 | 50.005 |
| — | — | — | — | — | — |
| 8191 | 1FFF | 12.499 | 40959 | 9FFF | 62.499 |
| 8192 | 2000 | 12.500 | 40960 | A000 | 62.501 |
| 8193 | 2001 | 12.502 | 40961 | A001 | 62.502 |
| — | — | — | — | — | — |
| 16383 | 3FFF | 24.999 | 49151 | BFFF | 75.000 |
| 16384 | 4000 | 25.000 | 49152 | C000 | 75.001 |
| 16385 | 4001 | 25.002 | 49153 | C001 | 75.003 |
| — | — | — | — | — | — |
| 24575 | 5FFF | 37.499 | 57343 | DFFF | 87.500 |
| 24576 | 6000 | 37.501 | 57344 | E000 | 87.501 |
| 24577 | 6001 | 37.502 | 57345 | E001 | 87.503 |
| — | — | — | — | — | — |
| 32765 | 7FFD | 49.996 | 65533 | FFFD | 99.997 |
| 32766 | 7FFE | 49.998 | 65534 | FFFE | 99.998 |
| 32767 | 7FFF | 49.999 | 65535 | FFFF | 100.000 |

Enhanced Spectrum (ES) PWM Control

In this PWM control, the entire display period is divided into 128 display segments. The total display period is the time from the first grayscale clock (GSCLK) to the 65,536th GS clock input for the 16-bit length PWM. Each display segment has a maximum of 512 grayscale clocks (maximum). The OUT_n on-time changes, depending on the 16-bit grayscale data. Refer to **Table 4** for the sequence of information and to **Figure 18** for the timing information.

Table 4. ES PWM Drive Turn On-Time Length

| GS DATA | | OUT _n DRIVER OPERATION |
|---------|-------|---|
| DECIMAL | HEX | |
| 0 | 0000h | Does not turn on |
| 1 | 0001h | Turns on for one GSCLK period in the first display segment |
| 2 | 0002h | Turns on for one GSCLK period in the first and 65th display segments |
| 3 | 0003h | Turns on for one GSCLK period in the first, 65th, and 33th display segments |
| 4 | 0004h | Turns on for one GSCLK period in the first, 65th, 33th, and 97th display segments |
| 5 | 0005h | Turns on for one GSCLK period in the first, 65th, 33th, 97th, and 17th display segments |
| 6 | 0006h | Turns on for one GSCLK period in the first, 65th, 33th, 97th, 17th, and 81th display segments |
| — | — | The number of display segments where OUT _n is turned on for one GSCLK is incremented by increasing the GS data in the following order: 1 > 65 > 33 > 97 > 17 > 81 > 49 > 113 > 9 > 73 > 41 > 105 > 25 > 89 > 57 > 121 > 5 > 69 > 37 > 101 > 21 > 85 > 53 > 117 > 13 > 77 > 45 > 109 > 29 > 93 > 61 > 125 > 3 > 67 > 35 > 99 > 19 > 83 > 51 > 115 > 11 > 75 > 43 > 107 > 27 > 91 > 59 > 123 > 7 > 71 > 39 > 103 > 23 > 87 > 55 > 119 > 15 > 79 > 47 > 111 > 31 > 95 > 63 > 127 > 2 > 66 > 34 > 98 > 18 > 82 > 50 > 114 > 10 > 74 > 42 > 106 > 26 > 90 > 58 > 122 > 6 > 70 > 38 > 102 > 22 > 86 > 54 > 118 > 14 > 78 > 46 > 110 > 30 > 94 > 62 > 126 > 4 > 68 > 36 > 100 > 20 > 84 > 52 > 116 > 12 > 76 > 44 > 108 > 28 > 92 > 60 > 124 > 8 > 72 > 40 > 104 > 24 > 88 > 56 > 120 > 16 > 80 > 48 > 112 > 32 > 96 > 64 > 128. |
| 127 | 007Fh | Turns on for one GSCLK period in the first to 127th display segments, but does not turn on in the 128th display segment |
| 128 | 0080h | Turns on for one GSCLK period in all display segments (first to 128th) |
| 129 | 0081h | Turns on for two GSCLK periods in the first display period and for one GSCLK period in all other display periods |
| — | — | The number of display segments where OUT _n is turned on for one GSCLK is incremented by increasing the GS data in the following order: 1 > 65 > 33 > 97 > 17 > 81 > 49 > 113 > 9 > 73 > 41 > 105 > 25 > 89 > 57 > 121 > 5 > 69 > 37 > 101 > 21 > 85 > 53 > 117 > 13 > 77 > 45 > 109 > 29 > 93 > 61 > 125 > 3 > 67 > 35 > 99 > 19 > 83 > 51 > 115 > 11 > 75 > 43 > 107 > 27 > 91 > 59 > 123 > 7 > 71 > 39 > 103 > 23 > 87 > 55 > 119 > 15 > 79 > 47 > 111 > 31 > 95 > 63 > 127 > 2 > 66 > 34 > 98 > 18 > 82 > 50 > 114 > 10 > 74 > 42 > 106 > 26 > 90 > 58 > 122 > 6 > 70 > 38 > 102 > 22 > 86 > 54 > 118 > 14 > 78 > 46 > 110 > 30 > 94 > 62 > 126 > 4 > 68 > 36 > 100 > 20 > 84 > 52 > 116 > 12 > 76 > 44 > 108 > 28 > 92 > 60 > 124 > 8 > 72 > 40 > 104 > 24 > 88 > 56 > 120 > 16 > 80 > 48 > 112 > 32 > 96 > 64 > 128. |
| 255 | 00FFh | Turns on for two GSCLK periods in the first to 127th display segments and turns on one GSCLK period in the 128th display segment |
| 256 | 0100h | Turns on for two GSCLK periods in all display segments (first to 128th) |
| 257 | 0101h | Turns on for three GSCLK periods in the first display segments and for two GSCLK periods in all other display segments |
| — | — | The number of display segments where OUT _n is turned on for one GSCLK is incremented by increasing the GS data in the following order: 1 > 65 > 33 > 97 > 17 > 81 > 49 > 113 > 9 > 73 > 41 > 105 > 25 > 89 > 57 > 121 > 5 > 69 > 37 > 101 > 21 > 85 > 53 > 117 > 13 > 77 > 45 > 109 > 29 > 93 > 61 > 125 > 3 > 67 > 35 > 99 > 19 > 83 > 51 > 115 > 11 > 75 > 43 > 107 > 27 > 91 > 59 > 123 > 7 > 71 > 39 > 103 > 23 > 87 > 55 > 119 > 15 > 79 > 47 > 111 > 31 > 95 > 63 > 127 > 2 > 66 > 34 > 98 > 18 > 82 > 50 > 114 > 10 > 74 > 42 > 106 > 26 > 90 > 58 > 122 > 6 > 70 > 38 > 102 > 22 > 86 > 54 > 118 > 14 > 78 > 46 > 110 > 30 > 94 > 62 > 126 > 4 > 68 > 36 > 100 > 20 > 84 > 52 > 116 > 12 > 76 > 44 > 108 > 28 > 92 > 60 > 124 > 8 > 72 > 40 > 104 > 24 > 88 > 56 > 120 > 16 > 80 > 48 > 112 > 32 > 96 > 64 > 128. |
| 65407 | FF7Fh | Turns on for 511 GSCLK periods in the first to 127th display segments, but only turns on 510 GSCLK periods in the 128th display segment |
| 65408 | FF80h | Turns on for 511 GSCLK periods in all display segments (first to 128th) |
| 65409 | FF81h | Turns on for 512 GSCLK periods in the first display period and for 511 GSCLK periods in the second to 128th display segments |
| — | — | — |
| 65534 | FFFEh | Turns on for 512 GSCLK periods in the first to 63th and 65th to 127th display segments; also turns on 511 GSCLK periods in 64th and 128th display segments |
| 65535 | FFFFh | Turns on for 512 GSCLK periods in the first to 127th display segments but only turns on 511 GSCLK periods in the 128th display segment |

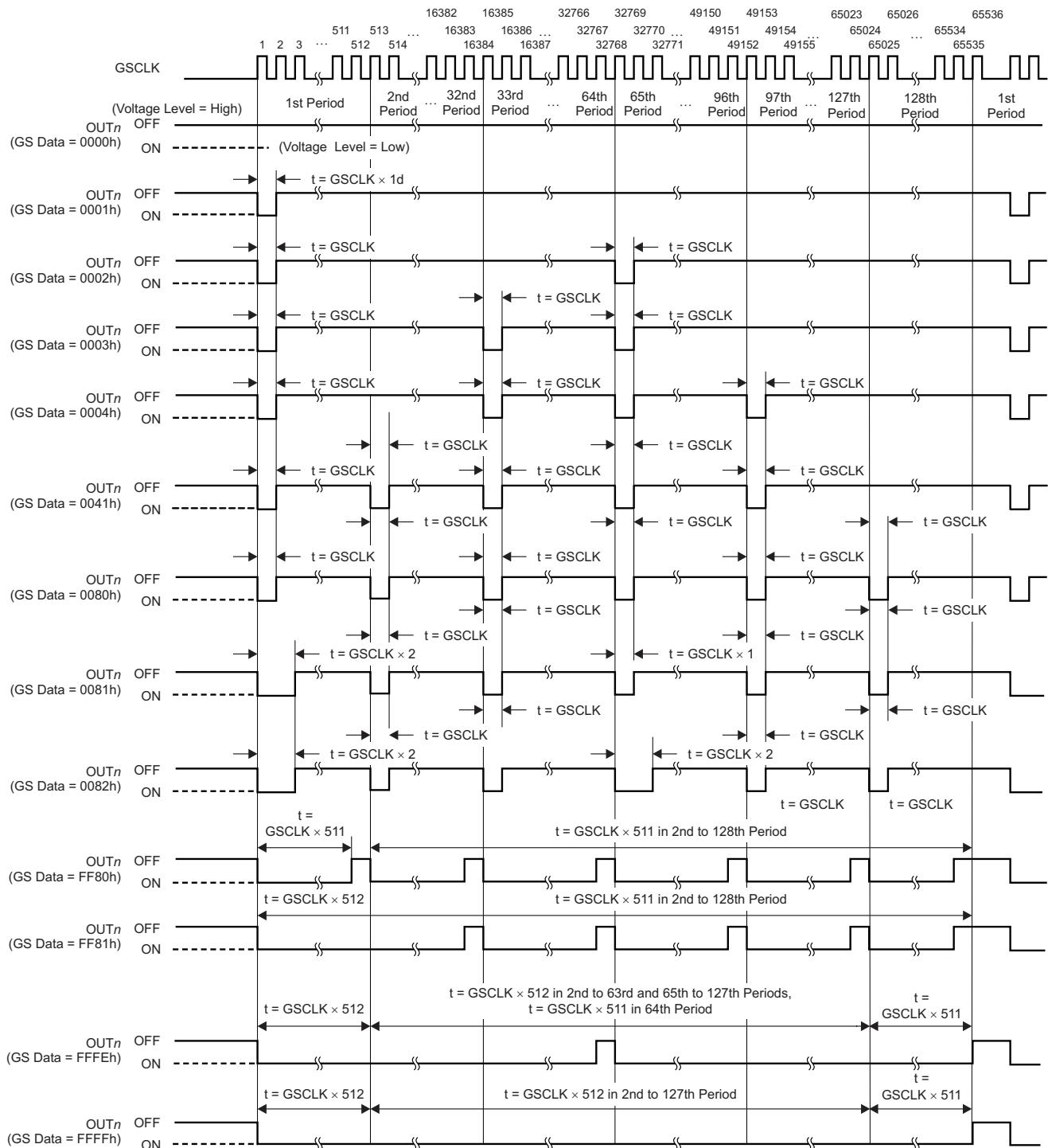


Figure 18. ES PWM Operation

Auto Display Repeat Function

This function can repeat the total display period as long as GSCLK is present, as shown in [Figure 19](#). This function is always enabled. OUTn turn on at the 513th GSCLK after the first LATGS command is input.

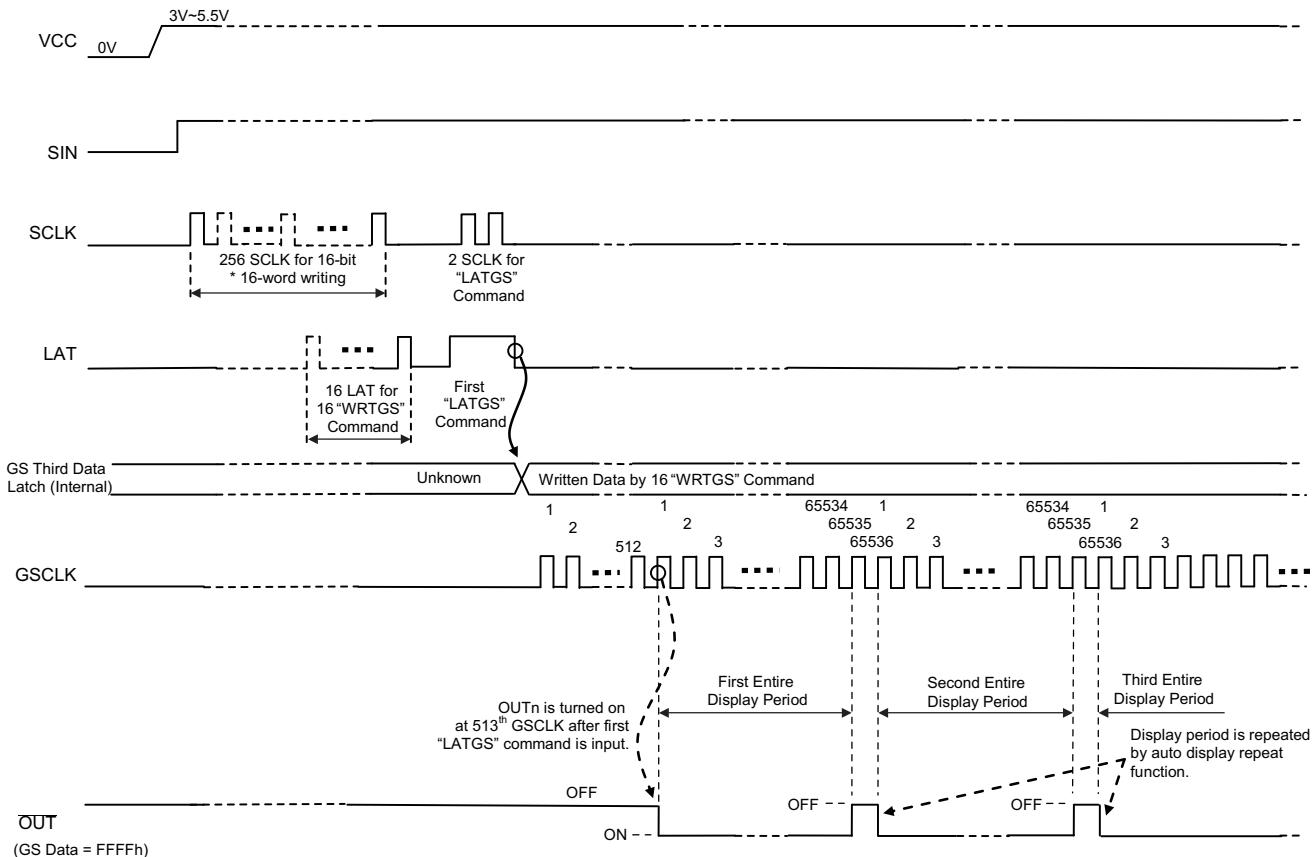


Figure 19. Auto Display Repeat Function

Auto Data Refresh Function

This function allows users to input grayscale (GS) data at any time without synchronizing the input to the display timing. When the LATGS command is input with the auto data refresh function enabled (XRFRESH bit = 0), the 256-bit data in the first GS data latch are copied only to the second GS data latch. The data in the second GS data latch are copied to the third data latch when the 65,536th GSCLK occurs. The third latch data are used for constant-current output (OUT0-OUT15) for the next display period.

When the LATGS command is input with the auto data refresh function disabled (XRFRESH bit = 1), the 256-bit data in the first GS data latch are copied to the second and third GS data latches at the same time and the GS data in the third data latch are used for OUT0-OUT15 on/off control from the next input GSCLK rising edge. Furthermore, the GS counter is set to '0' and all constant-current outputs (OUTn) are forced off. Refer to [Figure 20](#) for a timing diagram of the auto data refresh function.

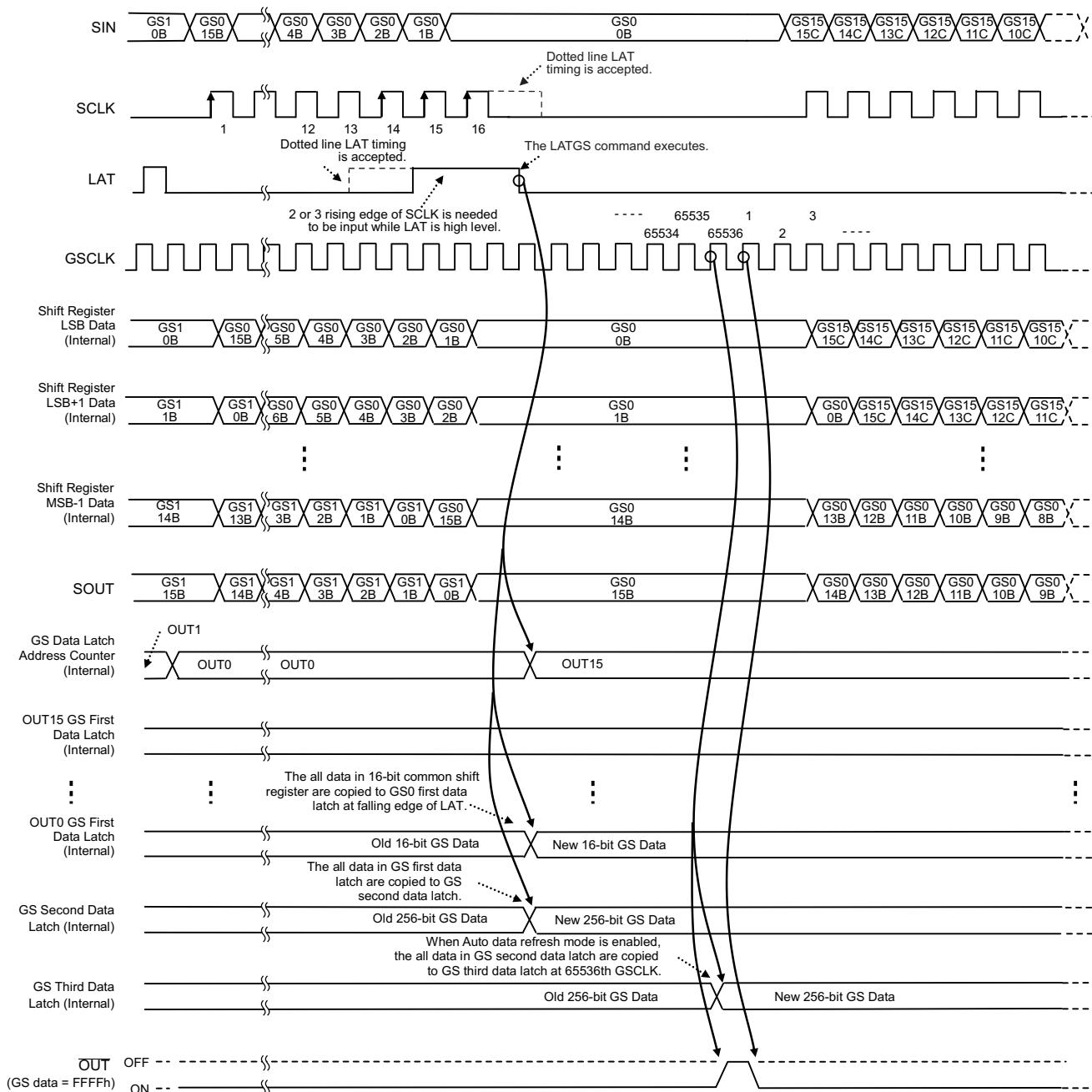


Figure 20. Auto Data Refresh Function (XRFRESH = 0, LATMODE = 0)

REGISTER AND DATA LATCH CONFIGURATION

The TLC59482 has one common shift register, one function control (FC) data latch, and a set of three data latches: the first, second, and third grayscale (GS) data latches. The common shift register and FC data latch are 16 bits long and the GS data latches are 256 bits long. [Figure 21](#) shows the common shift register and the data latches configuration.

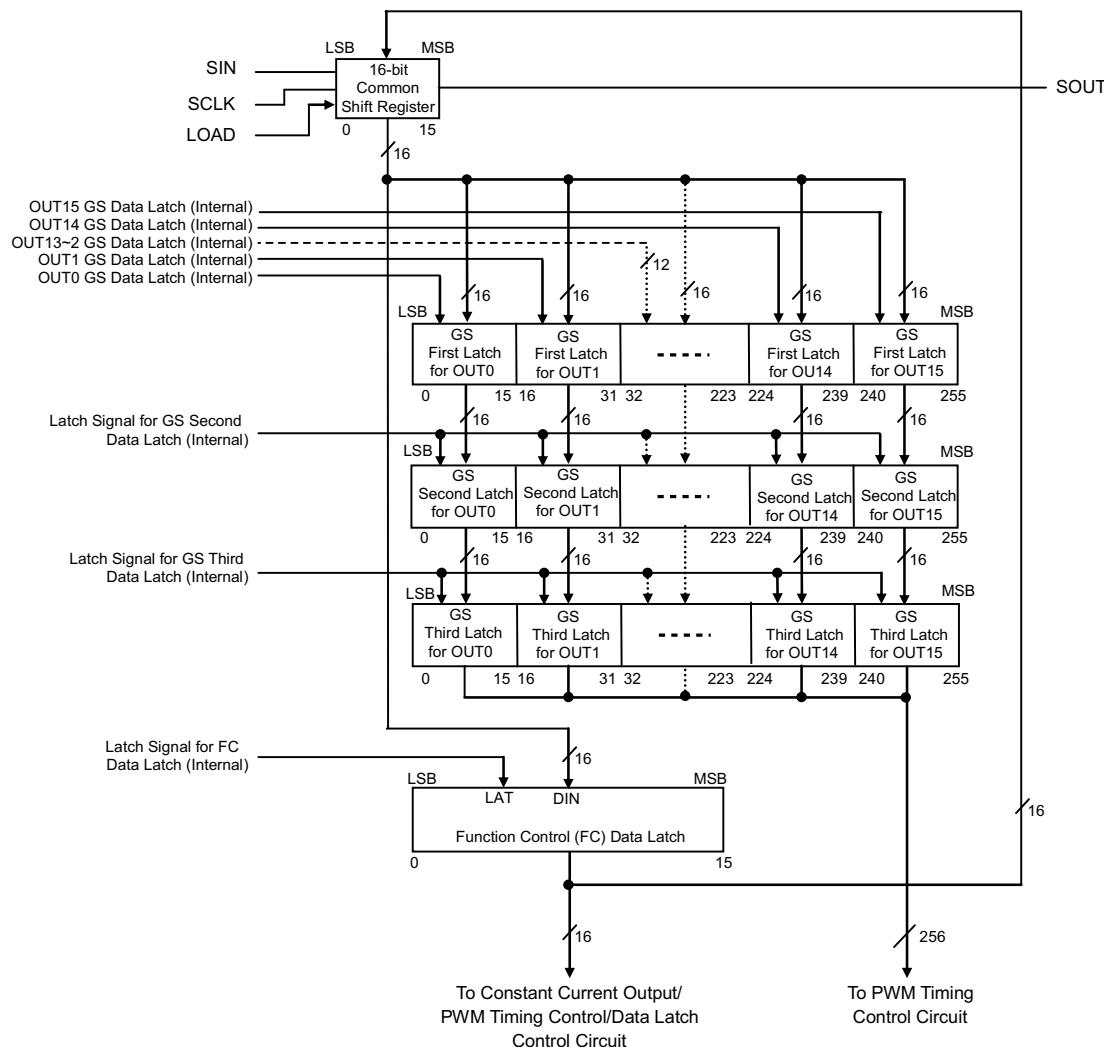


Figure 21. Shift Register and Data Latch Configuration

16-Bit Common Shift Register

The 16-bit common shift register is used to shift data from the SIN pin into the TLC59482. The data shifted into the register are used for GS and FC data. The LSB of the common shift register is connected to SIN and the MSB is connected to SOUT. On each SCLK rising edge, the data on SIN are shifted into the LSB and all 16 bits are shifted towards the MSB. The register MSB is always connected to SOUT. When the device is powered up, the data in the 16-bit common shift register are set to '0'.

First, Second, and Third Grayscale Data Latch

The first, second, and third grayscale (GS) data latches are each 256 bits long, and set the PWM timing for each constant-current output. The on-time of all constant-current outputs is controlled by the data in the third GS data latch. The 16-bit data are copied to the first GS data latch indicated by the GS data latch address counter when the WRTGS command is input. The 256-bit GS data for OUTn in the first data latch are copied to the second GS data latch when the LATGS command is input. The 256-bit data in the second data latch are copied to the third GS data latch when the 65,536th GSCLK occurs with the XRFRESH bit in the FC data latch set to '0'. When the XRFRESH bit is '1', the 256-bit data in the first data latch are copied to the second and third data latch at the same time. When the device powers up, all constant-current outputs are forced off until GS data are written to the third data latch. The GS data write sequence is shown in [Figure 22](#) and [Figure 23](#).

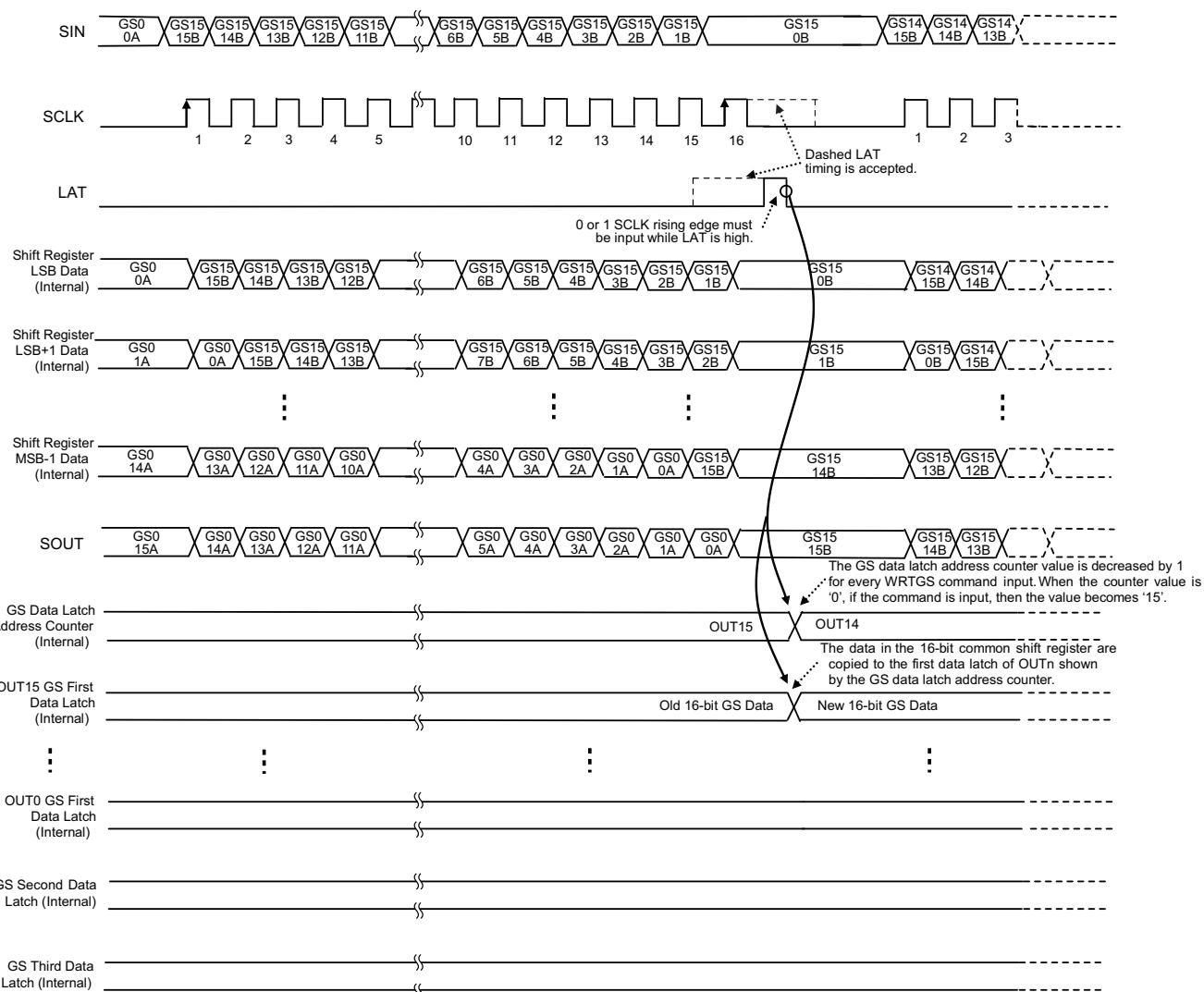


Figure 22. 16-Bit GS Data Write (WRTGS) Command

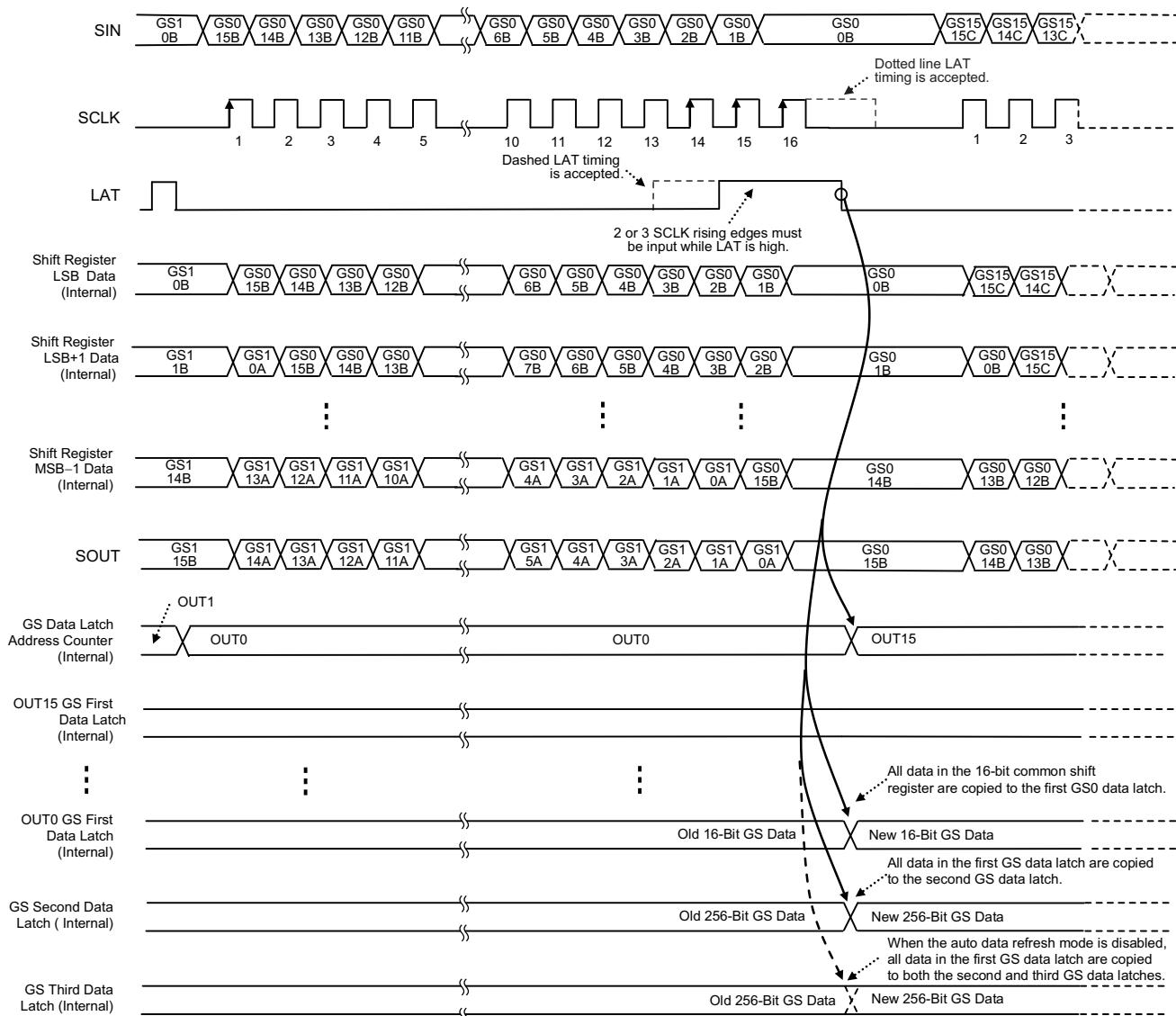


Figure 23. 256-Bit GS Data Latch (LATGS) Command (LATMODE = 0)

Function Control (FC) Data Latch

The function control (FC) data latch is 16 bits long. This latch sets the brightness control (BC) data, auto data refresh, enables or disables the display timing reset, and selects the data latch mode. When the device is powered on, the data in the FC data latch are set to the default values, as shown in [Table 5](#).

Table 5. Function Control Data Latch Bit Description

| BIT NUMBER | BIT NAME | DEFAULT VALUE (Binary) | DESCRIPTION |
|--------------|----------|------------------------|--|
| 0 (LSB) to 3 | N/A | 0000 | No applicable bit |
| 4-9 | BC | 100000 | Global brightness (BC) control bit (000000-111111). This 6-bit data controls all output current with 64 steps between 0% and 100% of the maximum current determined by a external resistor. When all bits are '0', all outputs are off. When the device is powered on, all output current are set to approximately 50%. |
| 10 | XRFRESH | 0 | Auto data refresh mode bit (0 = enabled, 1 = disabled). If the LATGS command is input while this bit is '1', all data in the first grayscale (GS) data latch are copied to both the second and third GS data latches. All OUT _n are forced off and the GS counter is also reset to '0'. If the LATGS command is input while this bit is '0', all data in the first GS data latch are only copied to the second GS data latch. All data in the second GS data latch are copied to the third GS data latch when the GS counter reaches the maximum count value of 65,535. No OUT _n are forced off and the GS counter continues counting. |
| 11 | TMRSTEN | 0 | Display timing reset enable bit (0 = disabled, 1 = enabled). If the TMGRST command is input while this bit is '1', the GS counter is reset to '0'. When this occurs, all OUT _n are forced off. When this bit is '0', even if the TMGRST command is input, the GS counter is not reset to '0'. |
| 12-14 | N/A | 000 | No applicable bit |
| 15 (MSB) | LATMODE | 0 | Latch mode select bit (0 = 15 WRTGS + 1 LATGS mode, 1 = 16 WRTGS + 1 LATGS mode). When this bit is '1', The commands for all GS data writes are (16 × WRTGS + 1 LATGS). The 16th WRTGS command is required to latch the last GS input 16-bit data to the first GS data latch. When this bit is '0', the commands for all GS data writes are (15 × WRTGS + 1 LATGS). The 16th WRTGS command is not required to latch the last GS input 16-bit data to the first GS data latch. |

Display Timing Reset Function

This function allows users to reset the GS counter using the TMGRST command described in [Table 6](#). This function is enabled when the TMRSTEN bit in the FC control data latch is '1'. The grayscale counter is reset to '0' when the TMGRST command is input. All OUT n are forced off. Refer to [Figure 26](#) for a display timing reset functional timing diagram

Table 6. Function Commands Description

| COMMAND NAME | SCLK RISING EDGES WHILE LAT IS HIGH | DESCRIPTION |
|----------------------------------|-------------------------------------|--|
| WRTGS (16-bit GS data write) | 0 or 1 | The 16-bit data in the 16-bit common shift register are copied to the 16-bit GS latch in the first latch selected by the GS data latch address counter. Refer to Figure 22 for a timing diagram of this command operation. |
| LATGS (256-bit GS data latch) | 2 or 3 | All data in the first GS data latch are only copied to the second GS data latch when the XRFRESH bit in the FC data latch is '0'. All data in the first GS data latch are copied to both the second and third GS data latches when the XRFRESH bit in the FC data latch is '1'. The GS data latch address counter is initialized to OUT15 at the same timing. Refer to Figure 23 for a timing diagram of this command operation. |
| READFC (FC data read) | 4 or 5 | The 16-bit data in the FC data latch are copied to the 16-bit shift register. The loaded data can be read from SOUT synchronized with the SCLK rising edge. Refer to Figure 24 for a timing diagram of this command operation. |
| WRTFC (FC data write) | 10 or 11 | The 16-bit data in the 16-bit common shift register are copied to the FC data latch. Refer to Figure 25 for a timing diagram of this command operation. |
| TMGRST (display timing reset) | 12 or 13 | The GS counter is reset to '0' and all constant-current outputs (OUT n) are forced off when the TMRSTEN bit in the FC data latch is '1'. However, the GS data in the third data latch are not updated. Refer to Figure 26 for a timing diagram of this command operation. |
| FCWRTEN (FC write enable) | 14 or 15 | FC writes are enabled by this command. This command must always be input before the FC data write occurs. Refer to Figure 25 for a timing diagram of this command operation. |

Function Commands

The TLC59482 has six commands that can be input with SCLK and LAT signals: WRTGS, LATGS, READFC, WRTFC, TMGRST, and FCWRTEN. Refer to [Figure 21](#) to [Figure 26](#) for detailed command input timing diagrams for each command. Each command function is described in [Table 6](#).

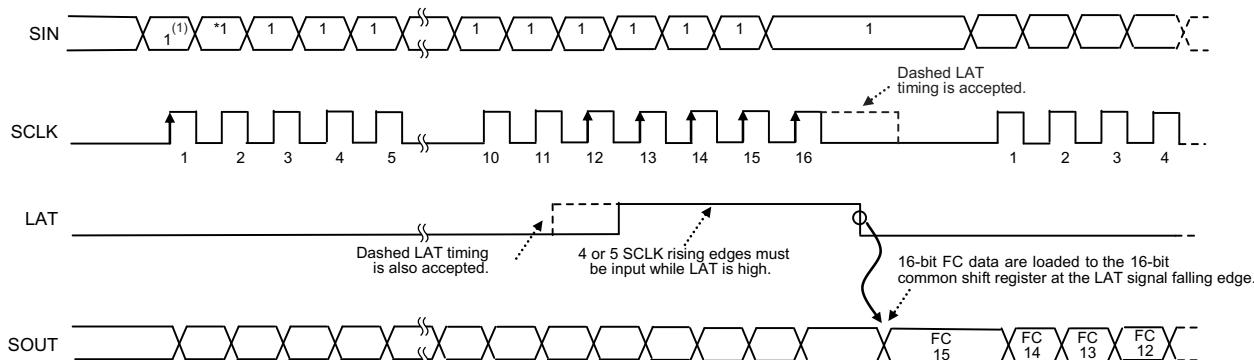


Figure 24. FC Data Read (READFC) Command Timing Diagram

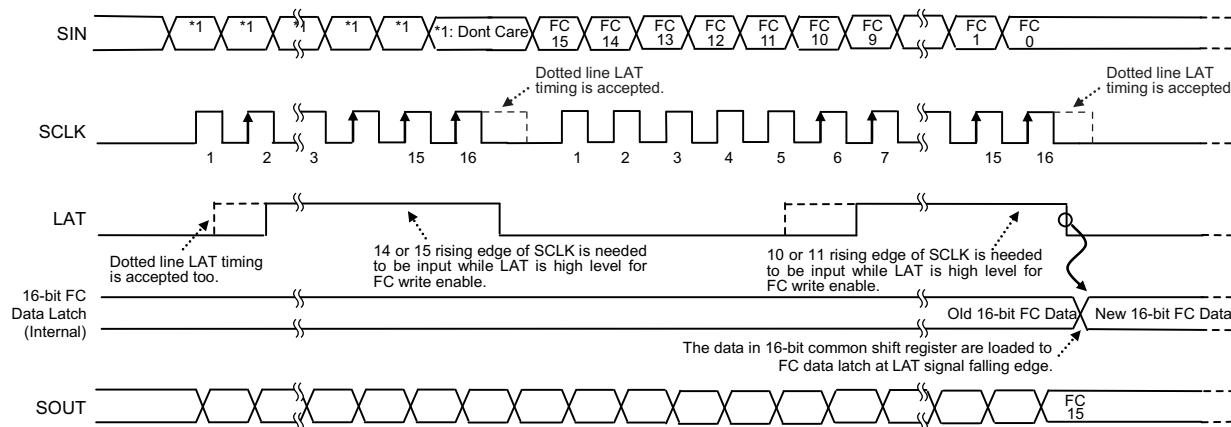


Figure 25. FC Data Write Enable (FCWRTEN) and FC Data Write (WRTFC) Command Timing Diagram

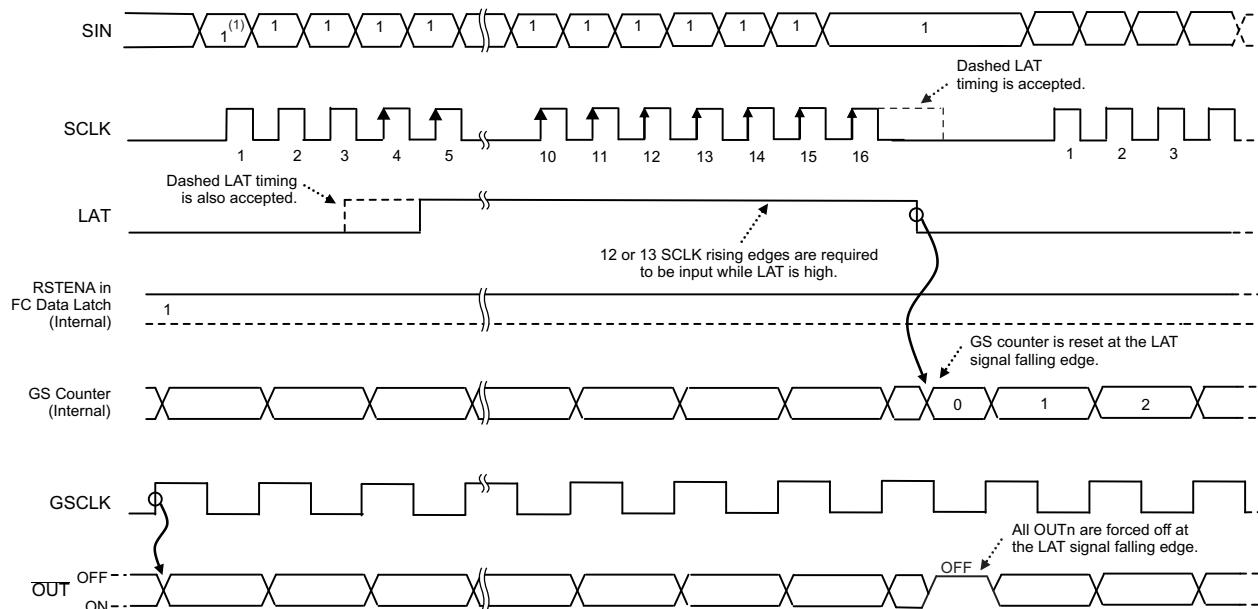
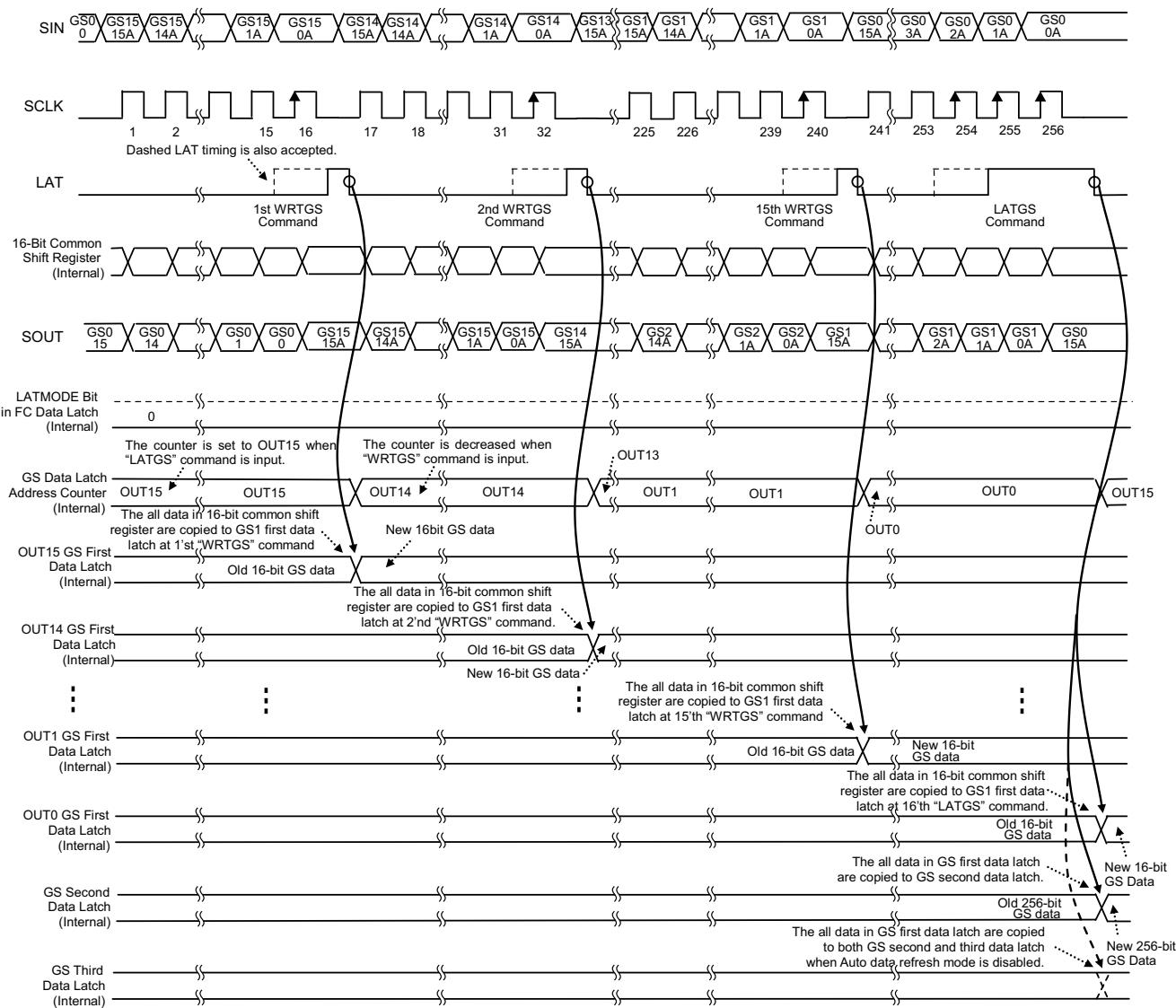
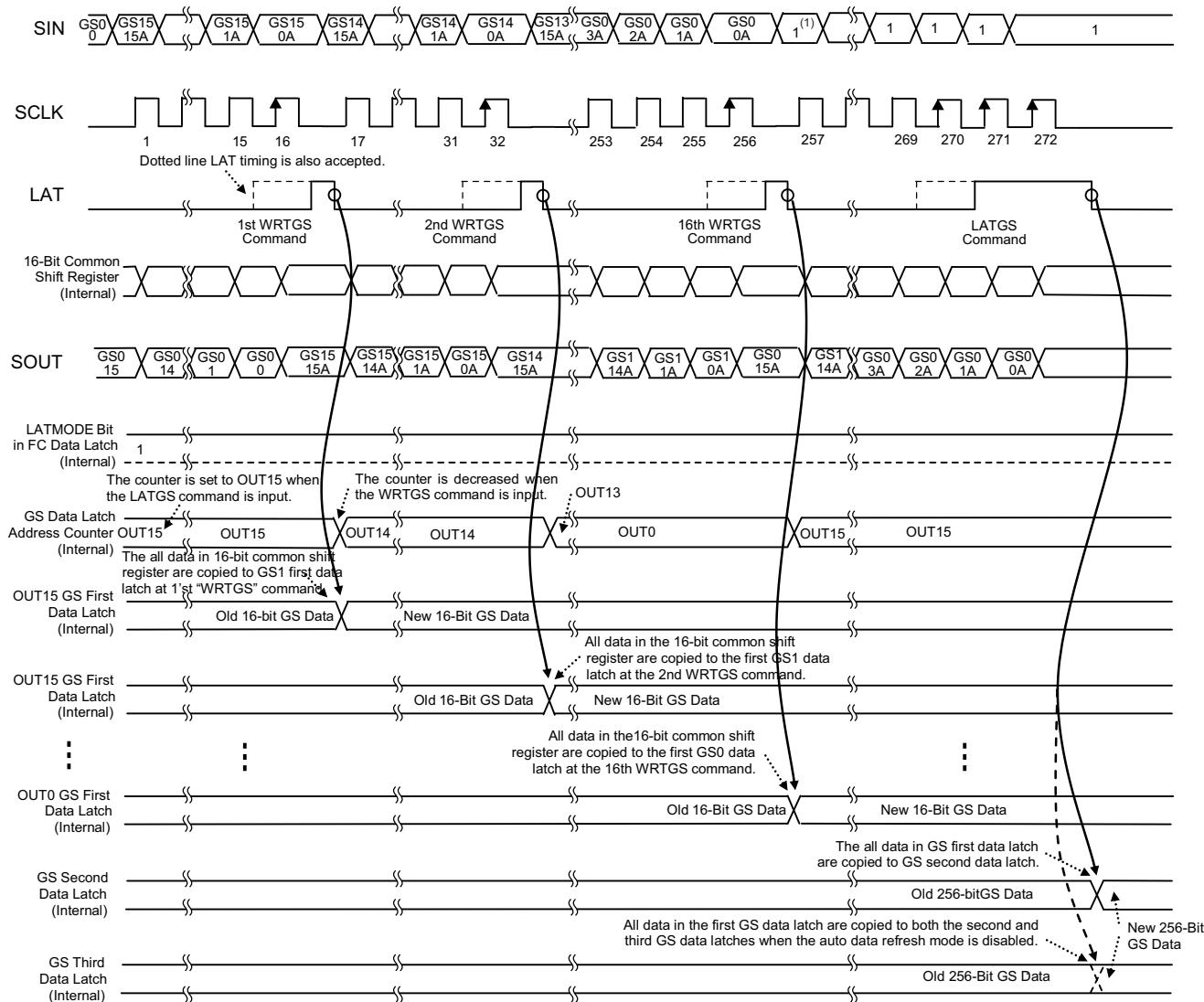


Figure 26. Display Timing Reset (TMGRST) Command Timing Diagram



**Figure 27. 256-Bit GS Data Write Sequence Timing Diagram
(15 × WRTGS + 1 LATGS, LATMODE = 0)**



**Figure 28. 256-Bit GS Data Write Sequence Timing Diagram
(16 × WRTGS + 1 LATGS, LATMODE = 1)**

NOISE REDUCTION

Large surge currents may flow through the device and the board on which the device is mounted if all 16 outputs turn on or off simultaneously. These large current surges can introduce detrimental noise and electromagnetic interference (EMI) into other circuits.

The TLC59482 turns the outputs on with a series delay for each group independently to provide a soft-start feature. The output current sinks are grouped into four groups. The first output group that is turned on/off are OUT0, OUT7, OUT8, and OUT15; the second output group is OUT1, OUT6, OUT9, and OUT14; the third output group is OUT2, OUT5, OUT10, and OUT13; and the fourth output group is OUT3, OUT4, OUT11, and OUT12. Each output group is turned on and off sequentially with a 5-ns (typical) delay between the groups. However, each output on/off is controlled by the GS clock.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|-------------------------|------------------|----------------------|--------------|--------------------------|----------------|
| TLC59482DBQ | ACTIVE | SSOP | DBQ | 24 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TLC59482 | Samples |
| TLC59482DBQR | ACTIVE | SSOP | DBQ | 24 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TLC59482 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

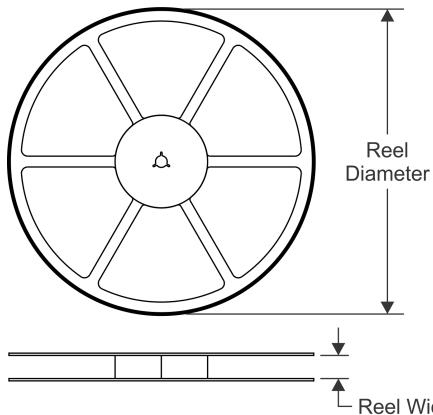
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "—" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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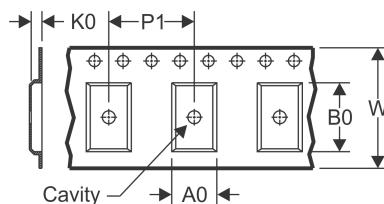
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

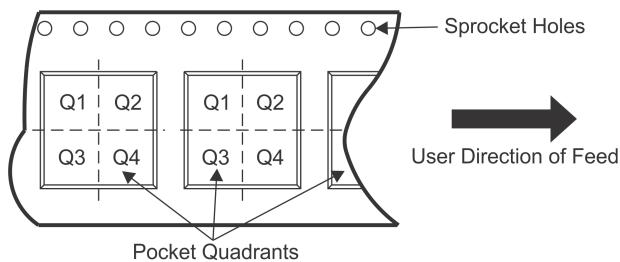


TAPE DIMENSIONS



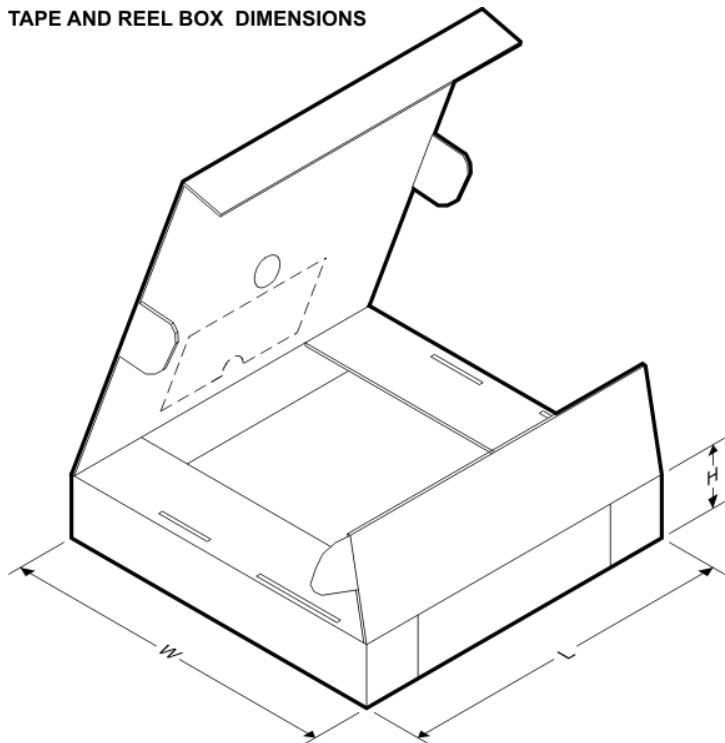
| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLC59482DBQR | SSOP | DBQ | 24 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

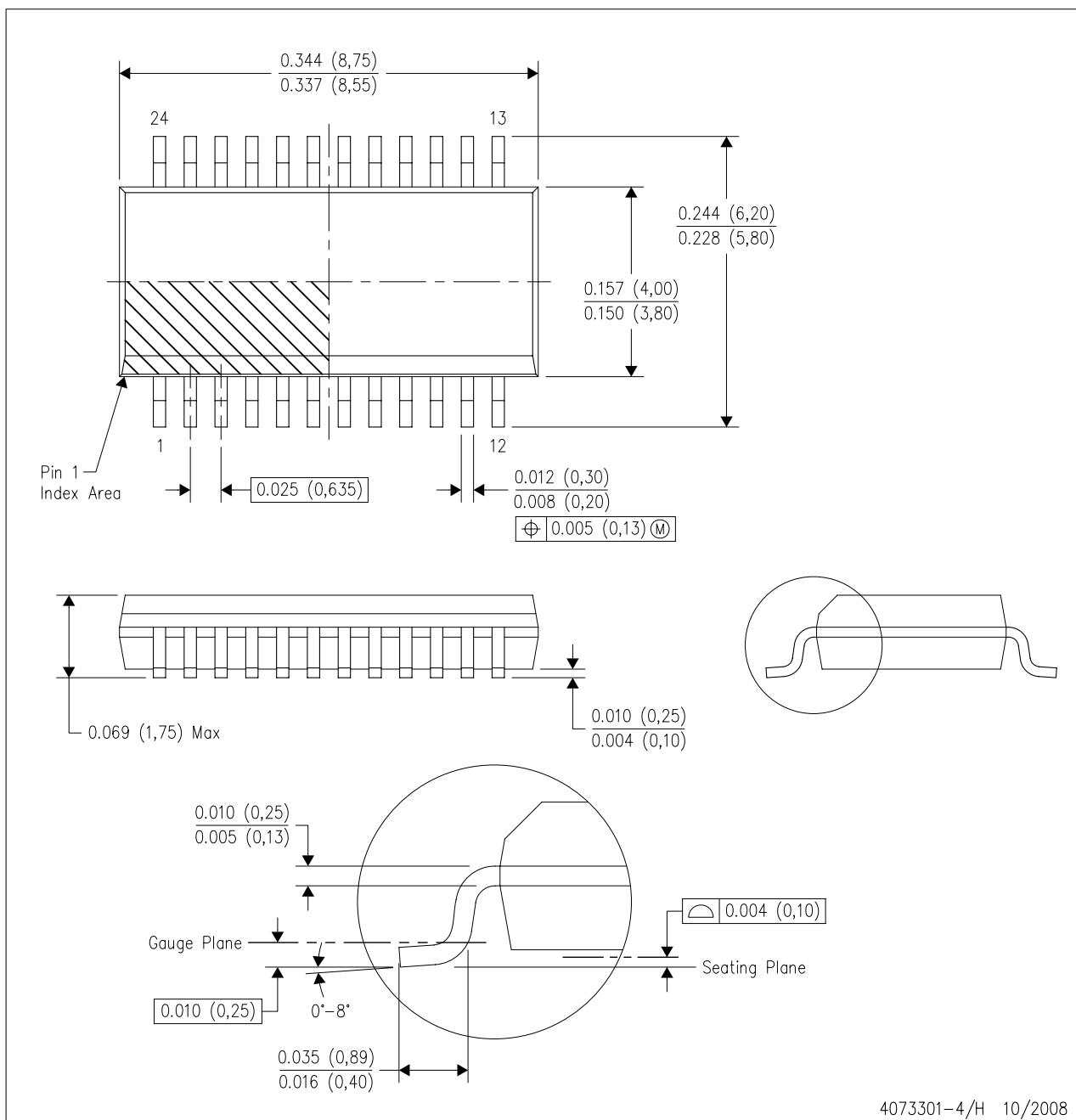
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLC59482DBQR | SSOP | DBQ | 24 | 2500 | 367.0 | 367.0 | 38.0 |

MECHANICAL DATA

DBQ (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
 - Falls within JEDEC MO-137 variation AE.

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