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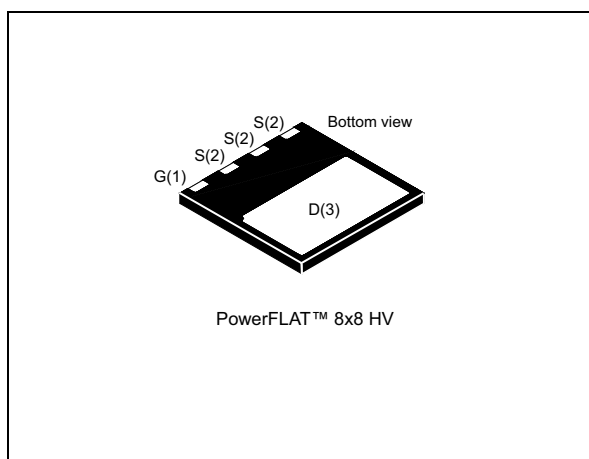
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# STL36N55M5

N-channel 550 V, 0.066  $\Omega$  typ., 22.5 A MDmesh™ M5  
 Power MOSFET in a PowerFLAT™ 8x8 HV package

Datasheet — production data



## Features

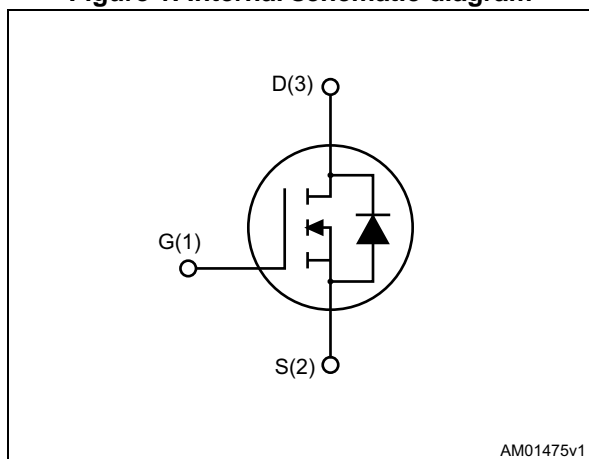
Order code	$V_{DS} @ T_{Jmax}$	$R_{DS(on) max}$	$I_D$
STL36N55M5	600 V	0.090 $\Omega$	22.5 A

- Extremely low  $R_{DS(on)}$
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested

## Applications

- Switching applications

Figure 1. Internal schematic diagram



## Description

This device is an N-channel Power MOSFET based on MDmesh™ M5 innovative vertical process technology combined with the well-known PowerMESH™ horizontal layout. The resulting product offers extremely low on-resistance, making it particularly suitable for applications requiring high power and superior efficiency.

Table 1. Device summary

Order code	Marking	Package	Packaging
STL36N55M5	36N55M5	PowerFLAT™ 8x8 HV	Tape and reel

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## Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	550	V
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	22.5	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	17	A
$I_{DM}^{(1),(2)}$	Drain current (pulsed)	90	A
$I_D^{(3)}$	Drain current (continuous) at $T_{amb} = 25\text{ }^\circ\text{C}$	3.7	A
$I_D^{(3)}$	Drain current (continuous) at $T_{amb} = 100\text{ }^\circ\text{C}$	2.2	A
$P_{TOT}^{(3)}$	Total dissipation at $T_{amb} = 25\text{ }^\circ\text{C}$	2.8	W
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	150	W
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_{j\text{max}}$ )	7	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	510	mJ
$dv/dt^{(4)}$	Peak diode recovery voltage slope	15	V/ns
$T_{stg}$	Storage temperature	- 55 to 150	$^\circ\text{C}$
$T_j$	Max. operating junction temperature	150	$^\circ\text{C}$

1. The value is rated according to  $R_{thj\text{-case}}$  and limited by package.
2. Pulse width limited by safe operating area.
3. When mounted on FR-4 board of inch<sup>2</sup>, 2 oz Cu.
4.  $I_{SD} \leq 22.5\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{Peak} < V_{(BR)DSS}$ ,  $V_{DD} = 340\text{ V}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj\text{-case}}$	Thermal resistance junction-case max	0.83	$^\circ\text{C}/\text{W}$
$R_{thj\text{-amb}}^{(1)}$	Thermal resistance junction-ambient max	45	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of inch<sup>2</sup>, 2 oz Cu.

Electrical characteristics

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## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0$	550			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 550\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 550\text{ V}$ , $T_C = 125\text{ °C}$			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 25\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 16.5\text{ A}$		0.066	0.090	$\Omega$

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	2670	-	pF
$C_{oss}$	Output capacitance		-	75	-	pF
$C_{riss}$	Reverse transfer capacitance		-	6.6	-	pF
$C_{o(er)}^{(1)}$	Equivalent output capacitance energy related	$V_{GS} = 0$ , $V_{DS} = 0\text{ to }440\text{ V}$	-	71	-	pF
$C_{o(tr)}^{(2)}$	Equivalent output capacitance time related		-	192	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	1.85	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 440\text{ V}$ , $I_D = 16.5\text{ A}$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 16</a> )	-	62	-	nC
$Q_{gs}$	Gate-source charge		-	15	-	nC
$Q_{gd}$	Gate-drain charge		-	27	-	nC

- $C_{o(er)}$  is a constant capacitance value that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$
- $C_{o(tr)}$  is a constant capacitance value that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$

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Electrical characteristics

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(V)}$	Voltage delay time	$V_{DD} = 400\text{ V}$ , $I_D = 22\text{ A}$ , $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 20</a> )	-	56	-	ns
$t_{r(V)}$	Voltage rise time		-	13	-	ns
$t_{f(i)}$	Current fall time		-	13	-	ns
$t_{c(off)}$	Crossing time		-	17	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		22.5	A
$I_{SDM}^{(1),(2)}$	Source-drain current (pulsed)		-		90	A
$V_{SD}^{(3)}$	Forward on voltage	$I_{SD} = 22.5\text{ A}$ , $V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 22.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ (see <a href="#">Figure 17</a> )	-	292		ns
$Q_{rr}$	Reverse recovery charge		-	4.2		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	29		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 22.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 17</a> )	-	364		ns
$Q_{rr}$	Reverse recovery charge		-	6		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	33		A

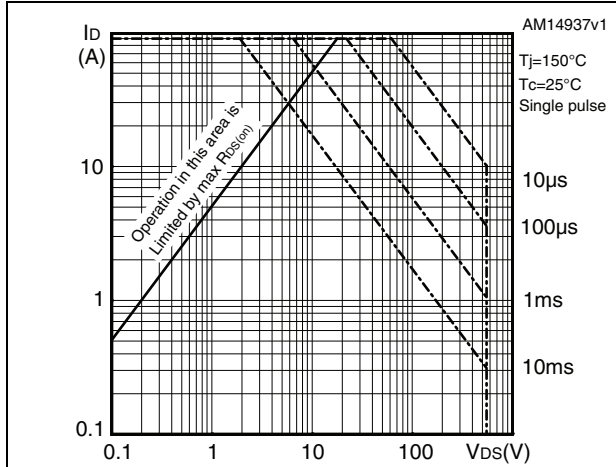
1. The value is rated according to  $R_{thj-case}$  and limited by package.
2. Pulse width limited by safe operating area
3. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

**Electrical characteristics**

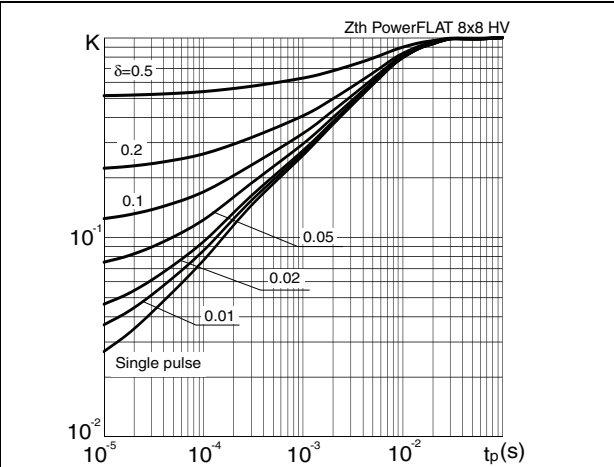
**STL36N55M5**

**2.1 Electrical characteristics (curves)**

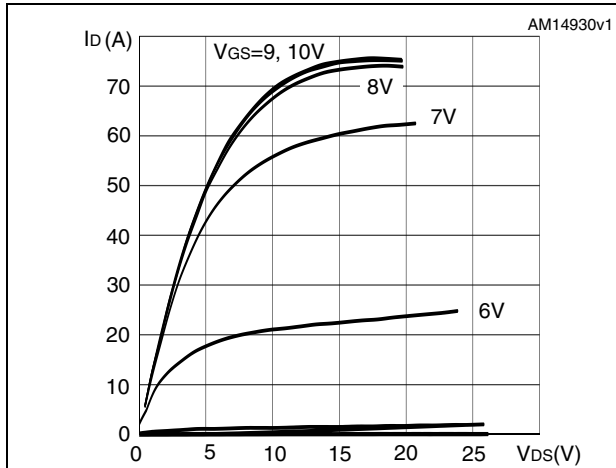
**Figure 2. Safe operating area**



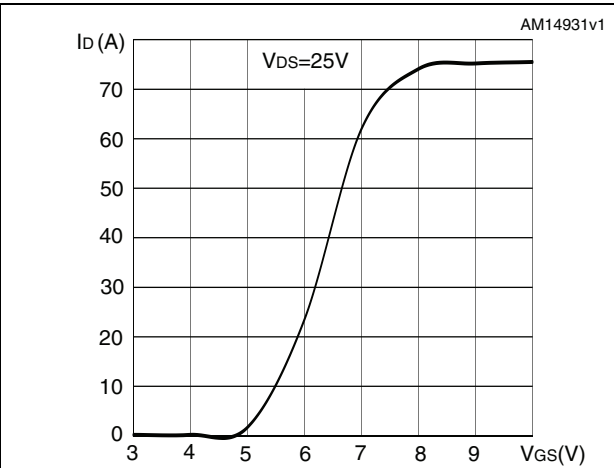
**Figure 3. Thermal impedance**



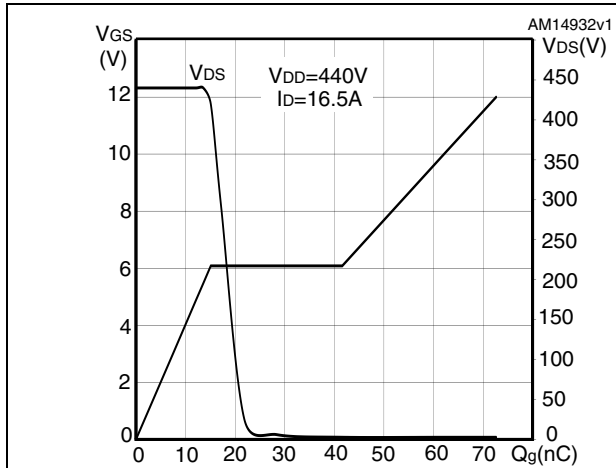
**Figure 4. Output characteristics**



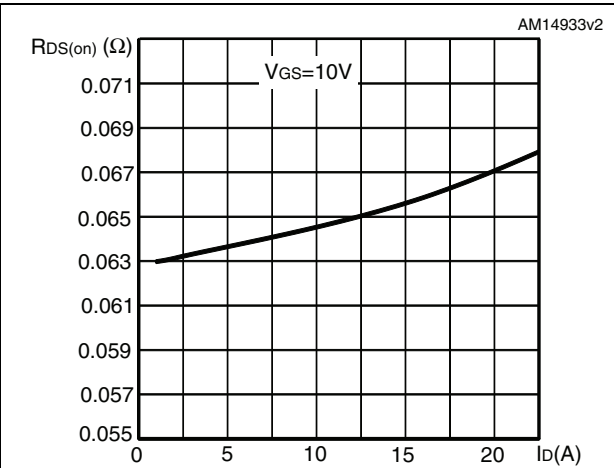
**Figure 5. Transfer characteristics**



**Figure 6. Gate charge vs gate-source voltage**



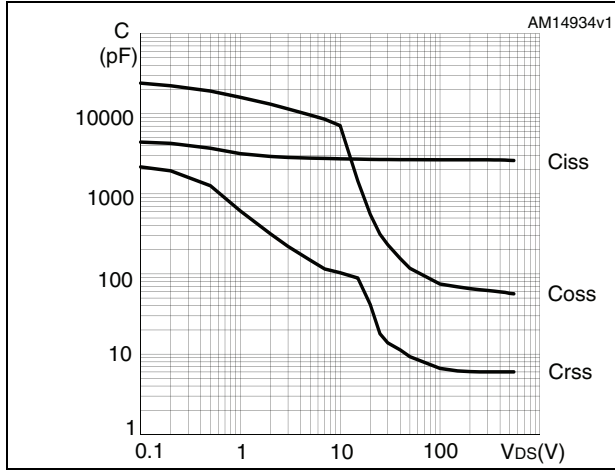
**Figure 7. Static drain-source on-resistance**



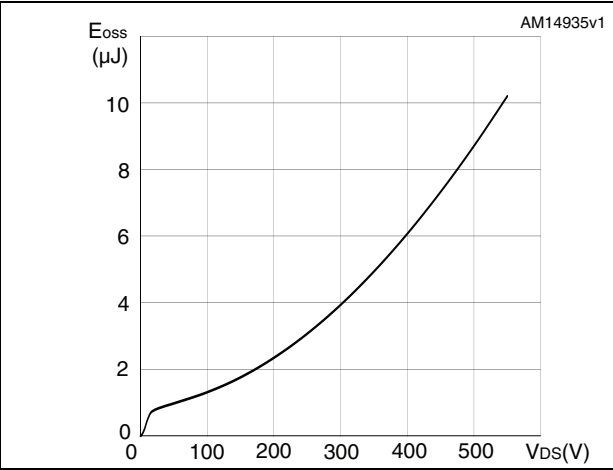
**STL36N55M5**

**Electrical characteristics**

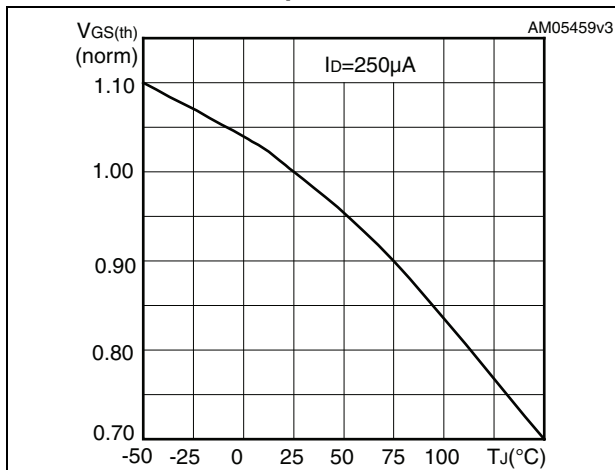
**Figure 8. Capacitance variations**



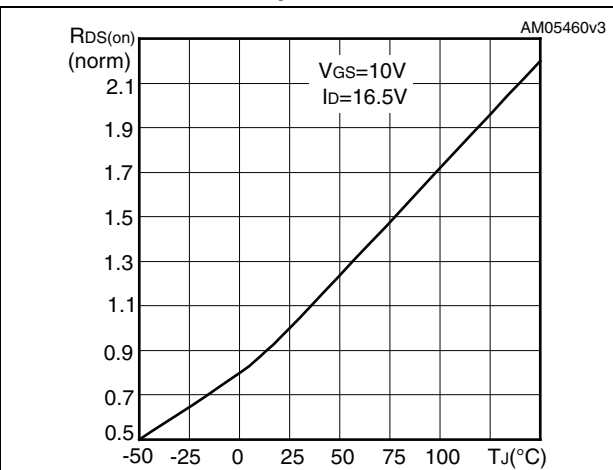
**Figure 9. Output capacitance stored energy**



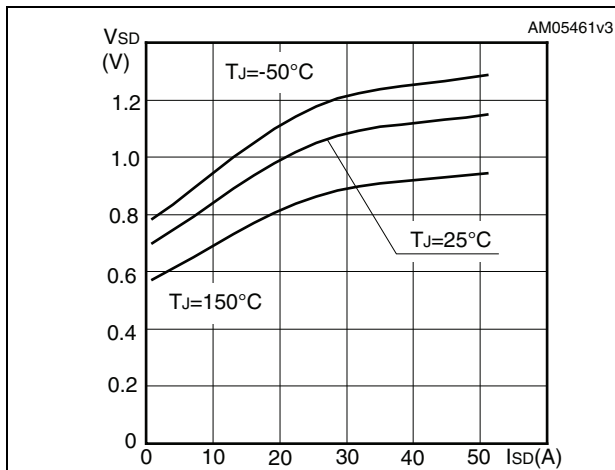
**Figure 10. Normalized gate threshold voltage vs temperature**



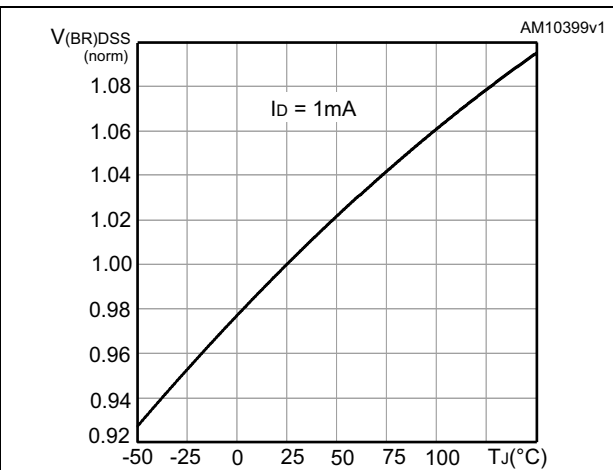
**Figure 11. Normalized on-resistance vs temperature**



**Figure 12. Source-drain diode forward characteristics**



**Figure 13. Normalized V(BR)DSS vs temperature**

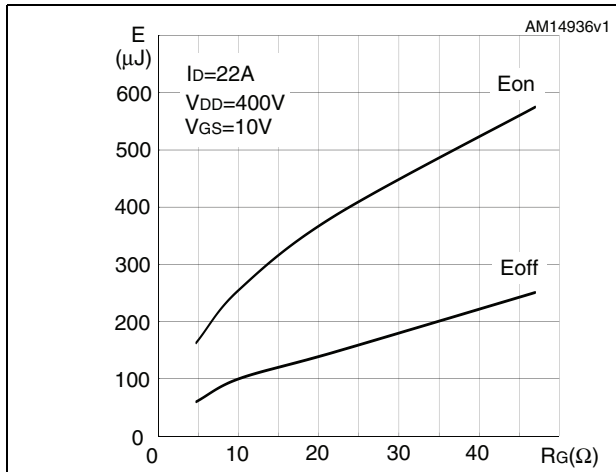




**Electrical characteristics**

**STL36N55M5**

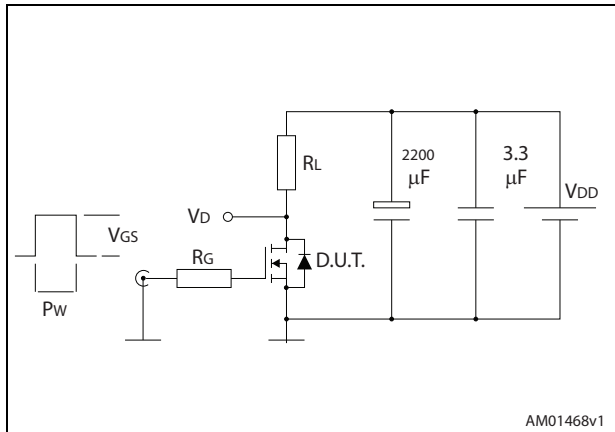
**Figure 14. Switching losses vs gate resistance**  
 (1)



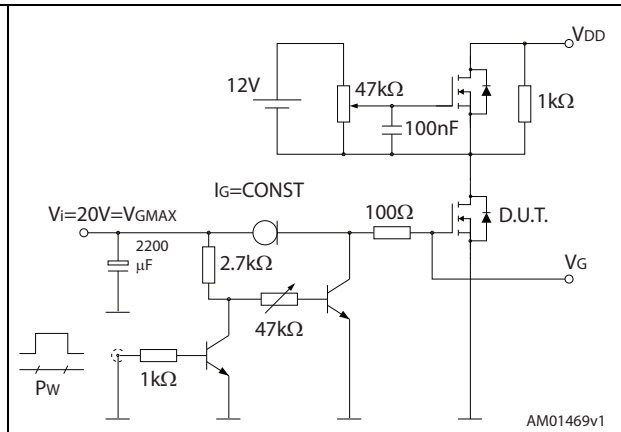
1.  $E_{on}$  including reverse recovery of a SiC diode.

### 3 Test circuits

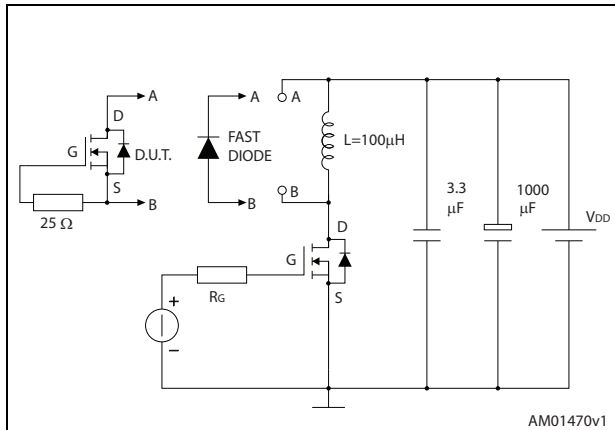
**Figure 15. Switching times test circuit for resistive load**



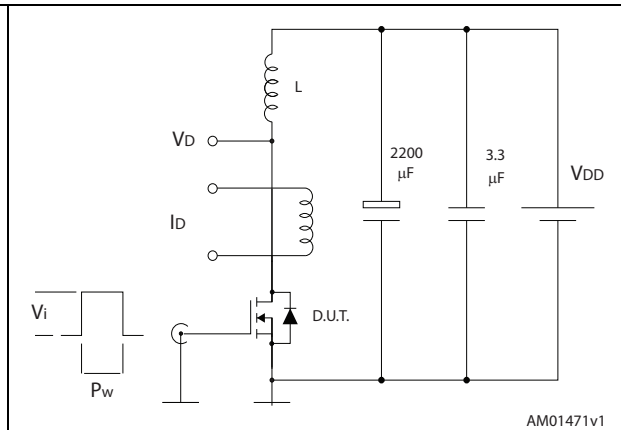
**Figure 16. Gate charge test circuit**



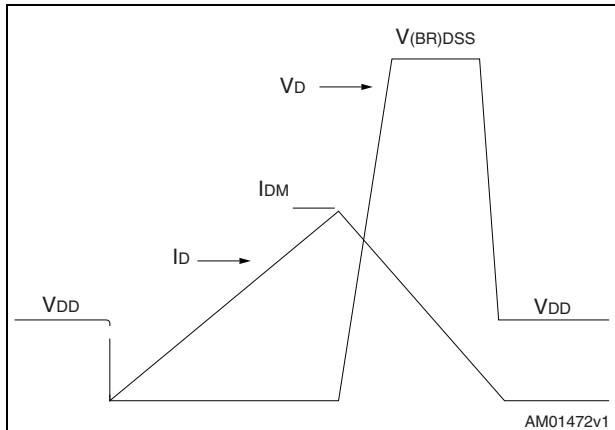
**Figure 17. Test circuit for inductive load switching and diode recovery times**



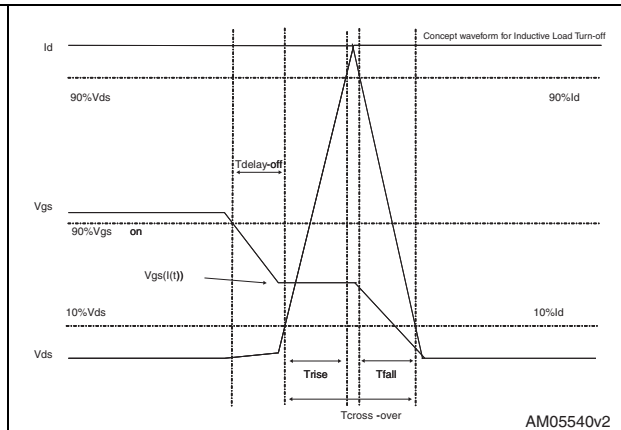
**Figure 18. Unclamped inductive load test circuit**



**Figure 19. Unclamped inductive waveform**



**Figure 20. Switching time waveform**



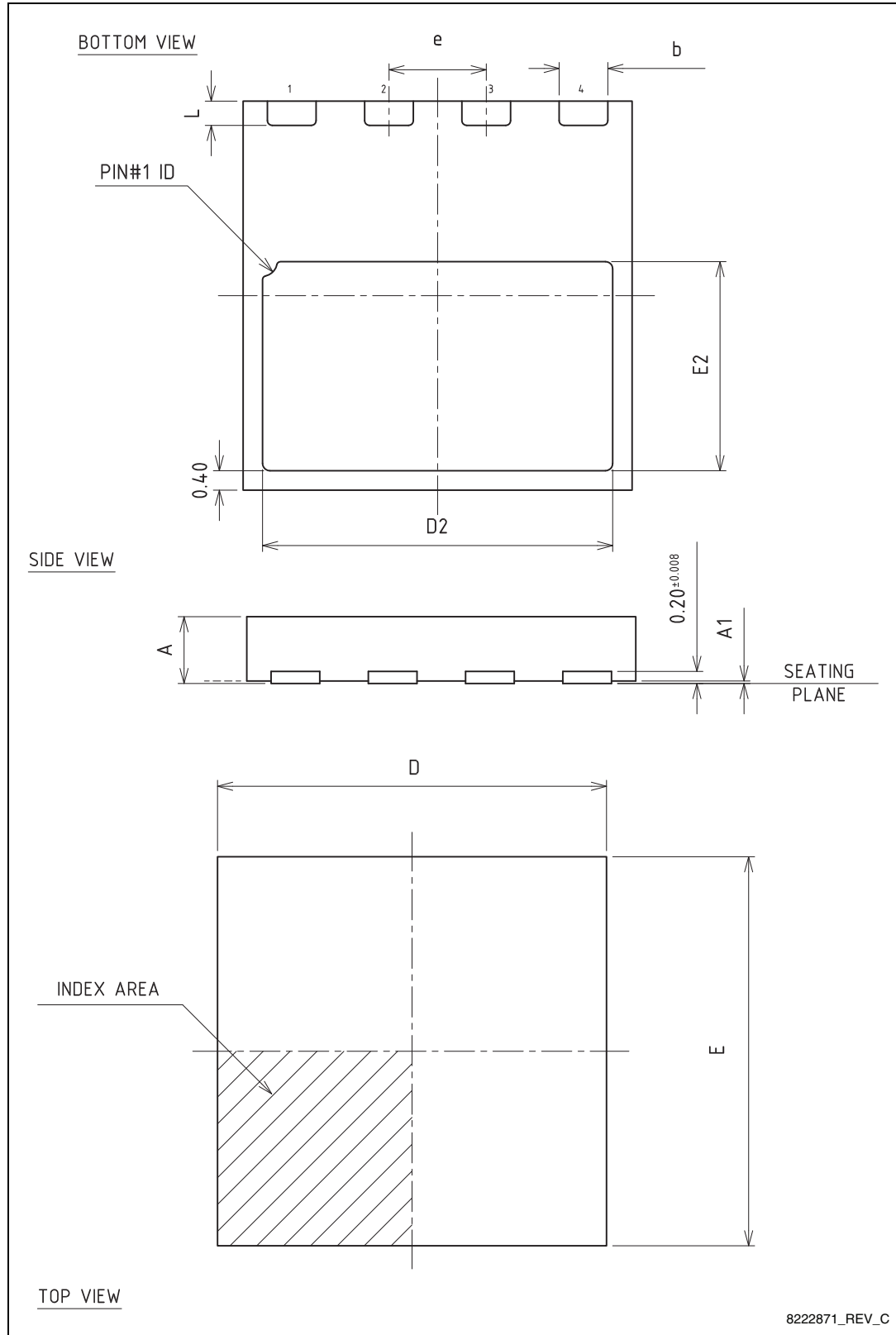
## **4 Package mechanical data**

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

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**Package mechanical data**

**Figure 21. PowerFLAT™ 8x8 HV drawing mechanical data**



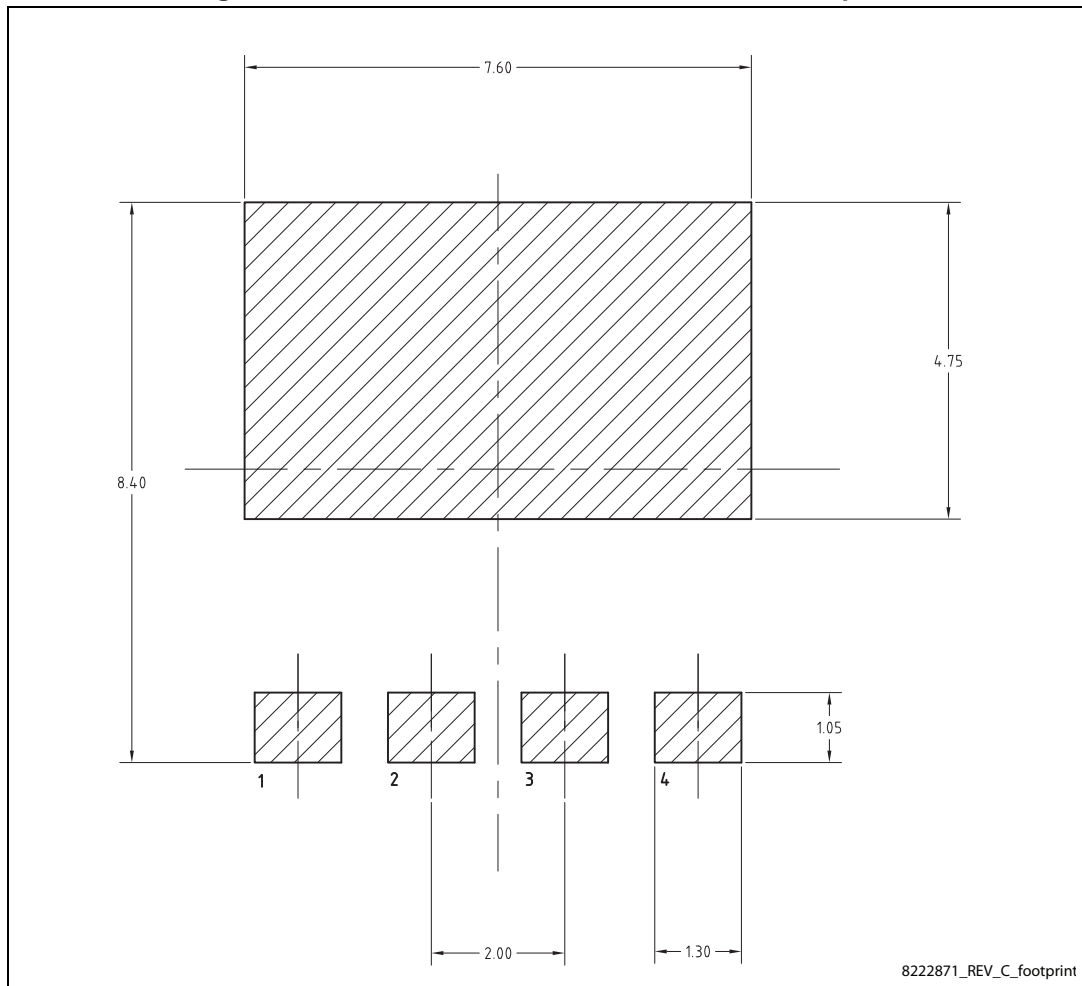
**Package mechanical data**

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**Table 8. PowerFLAT™ 8x8 HV mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.95	1.00	1.05
D		8.00	
E		8.00	
D2	7.05	7.20	7.30
E2	4.15	4.30	4.40
e		2.00	
L	0.40	0.50	0.60

**Figure 22. PowerFLAT™ 8x8 HV recommended footprint**



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Packaging mechanical data

## 5 Packaging mechanical data

Figure 23. PowerFLAT™ 8x8 HV tape

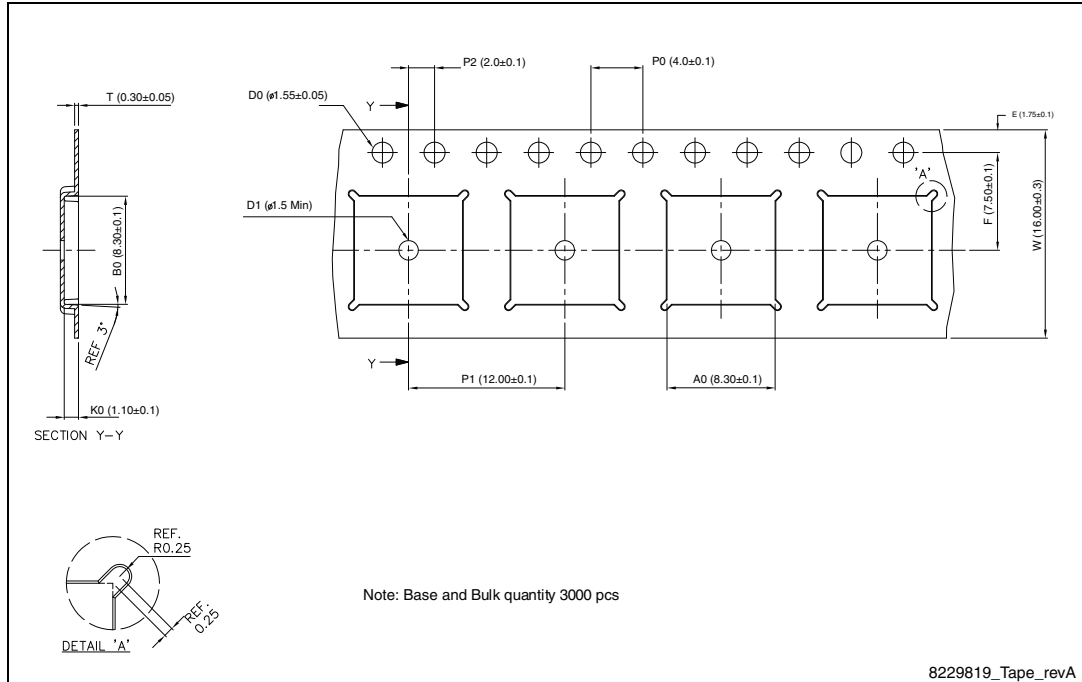
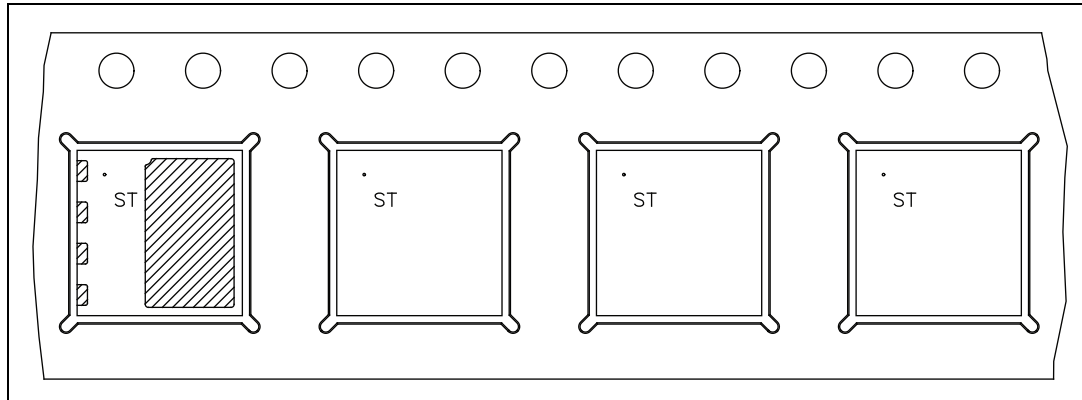


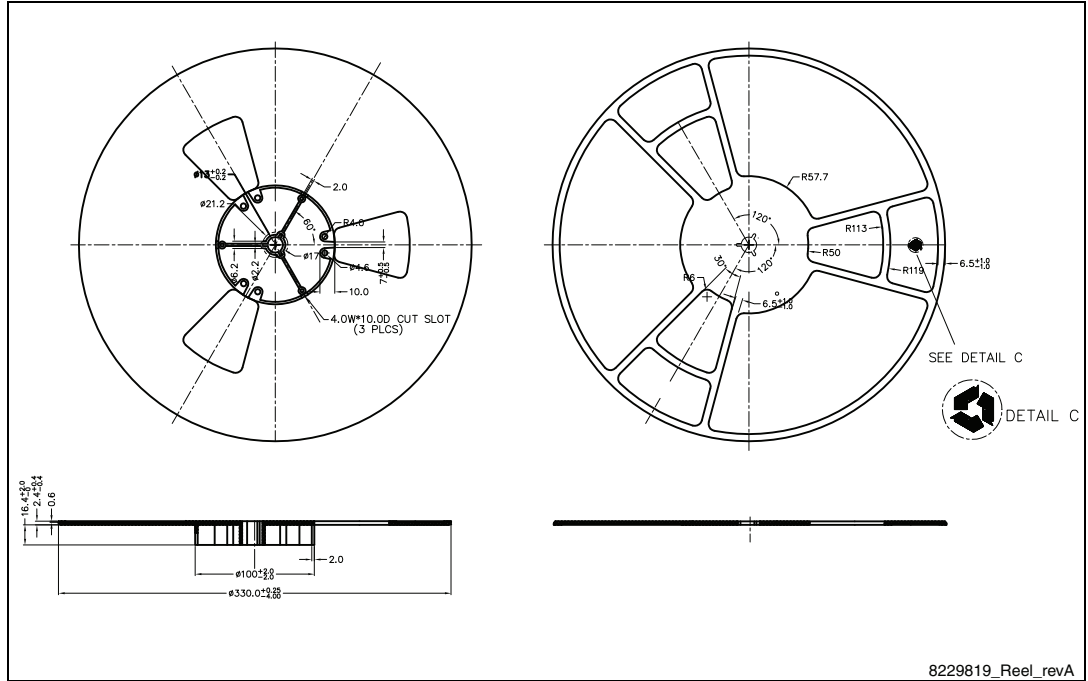
Figure 24. PowerFLAT™ 8x8 HV package orientation in carrier tape.



Packaging mechanical data

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Figure 25. PowerFLAT™ 8x8 HV reel



## 6 Revision history

Table 9. Document revision history

Date	Revision	Changes
14-Dec-2011	1	First release.
17-Oct-2012	2	Updated: <a href="#">Table 5</a> , <a href="#">6</a> and <a href="#">Table 7.:</a> <i>Source drain diode</i> typ. values
24-Jan-2013	3	<ul style="list-style-type: none"> <li>– Modified: <a href="#">Figure 1: Internal schematic diagram 4</a> and <a href="#">6</a></li> <li>– Document status promoted from preliminary data to production data</li> <li>– Modified: <math>V_{DD}</math> on <a href="#">Table 5</a></li> <li>– Minor text changes</li> </ul>
22-Sep-2014	4	<ul style="list-style-type: none"> <li>– Updated title, features and description in cover page.</li> <li>– Updated <a href="#">Figure 1: Internal schematic diagram</a>.</li> <li>– Updated <a href="#">Section 4: Package mechanical data</a>.</li> </ul>



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