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[Bel Fuse Inc.](#)
[1840326-1](#)

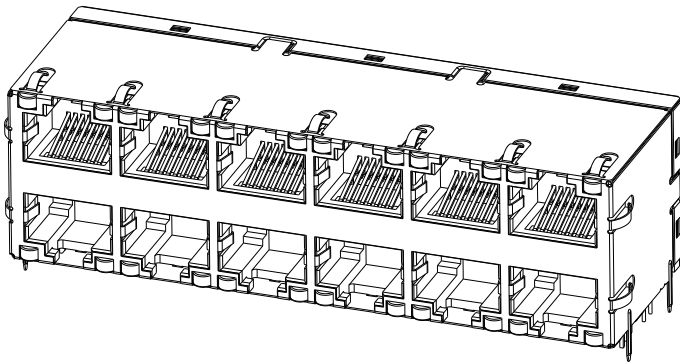
For any questions, you can email us directly:

sales@integrated-circuit.com

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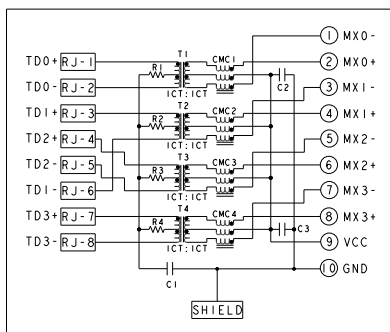
PRODUCT MAY BE PROTECTED BY ONE OR MORE OF THE FOLLOWING US PATENTS:							
5736910	5939955	6425781	6428361	6554638	6840817	7123117	
7429195	7717749	7808751	6217391	6149050	7924130		

REVISIONS					
#	LTN	DESCRIPTION	DATE	BY	APP
	N	EC-1411035 COMPANY LOGO CHANGE	20DEC2014	GZ	TY



S8G56 GIGABIT CIRCUIT 

TOP AND BOTTOM PORTS



C1 = 1000pF, 2kV CAPACITOR
C2 - C3 = 10nF, 50V CAPACITORS
R1 - R4 = 75 Ohms, 1/16W, RESISTORS

PIN DESIGNATIONS

(REPEAT FOR EACH VERTICAL PAIR OF PORTS.)

PCB PINS
(TOP VIEW,
COMP. SIDE)

The diagram illustrates a 16-bit bus architecture. At the top, there are 16 'TOP PORTS' numbered 0 to 15. At the bottom, there are 16 'BOTTOM PORTS' numbered 0 to 15. A central horizontal line represents the 16-bit bus. Each port is connected to the bus via a vertical line. The connections are as follows:

- TOP PORT 0 is connected to the bus.
- TOP PORT 1 is connected to the bus.
- TOP PORT 2 is connected to the bus.
- TOP PORT 3 is connected to the bus.
- TOP PORT 4 is connected to the bus.
- TOP PORT 5 is connected to the bus.
- TOP PORT 6 is connected to the bus.
- TOP PORT 7 is connected to the bus.
- TOP PORT 8 is connected to the bus.
- TOP PORT 9 is connected to the bus.
- TOP PORT 10 is connected to the bus.
- TOP PORT 11 is connected to the bus.
- TOP PORT 12 is connected to the bus.
- TOP PORT 13 is connected to the bus.
- TOP PORT 14 is connected to the bus.
- TOP PORT 15 is connected to the bus.
- BOTTOM PORT 0 is connected to the bus.
- BOTTOM PORT 1 is connected to the bus.
- BOTTOM PORT 2 is connected to the bus.
- BOTTOM PORT 3 is connected to the bus.
- BOTTOM PORT 4 is connected to the bus.
- BOTTOM PORT 5 is connected to the bus.
- BOTTOM PORT 6 is connected to the bus.
- BOTTOM PORT 7 is connected to the bus.
- BOTTOM PORT 8 is connected to the bus.
- BOTTOM PORT 9 is connected to the bus.
- BOTTOM PORT 10 is connected to the bus.
- BOTTOM PORT 11 is connected to the bus.
- BOTTOM PORT 12 is connected to the bus.
- BOTTOM PORT 13 is connected to the bus.
- BOTTOM PORT 14 is connected to the bus.
- BOTTOM PORT 15 is connected to the bus.

TOP PORTS

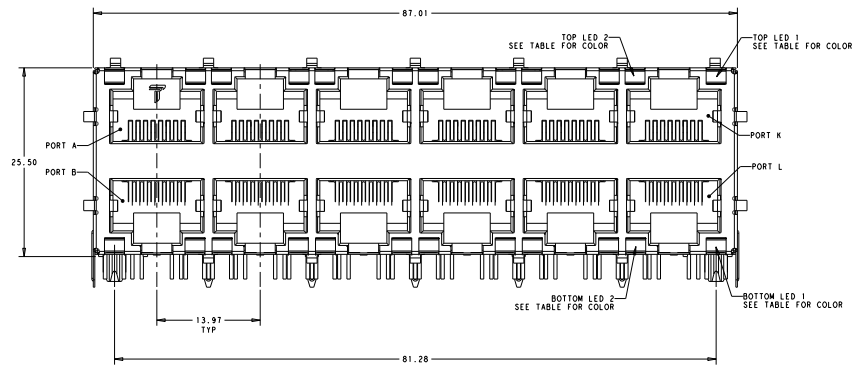
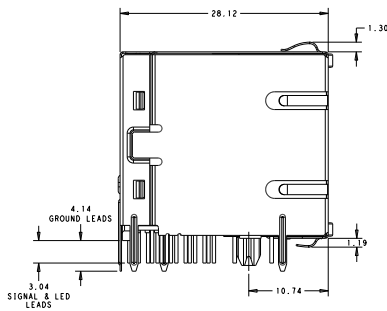
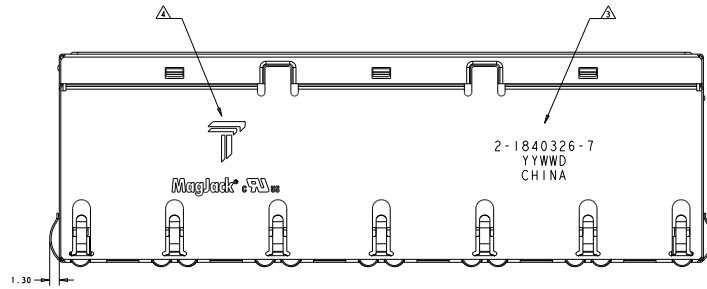
RJ-8  RJ-1

BOTTOM PORTS

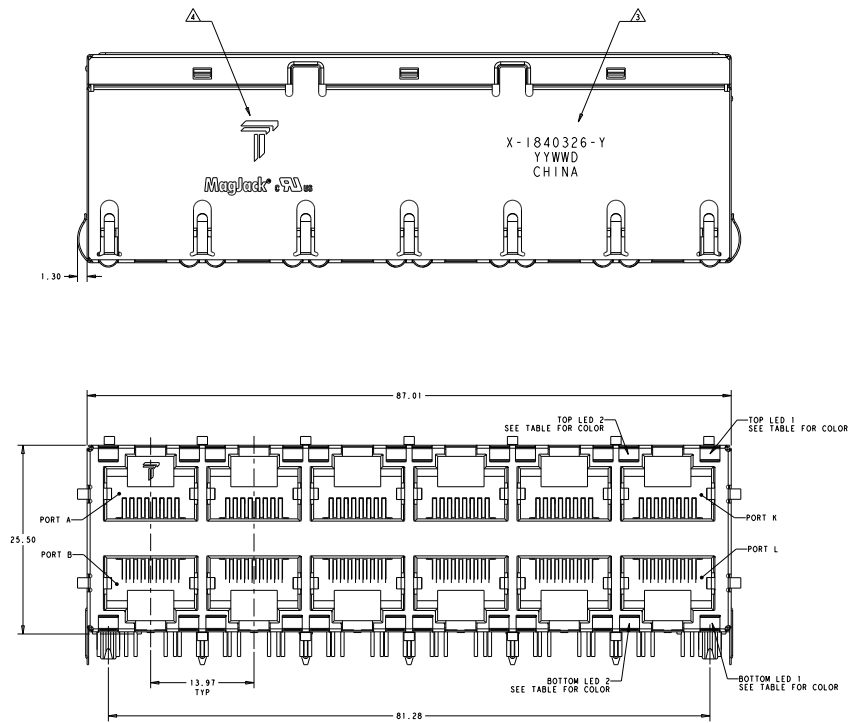
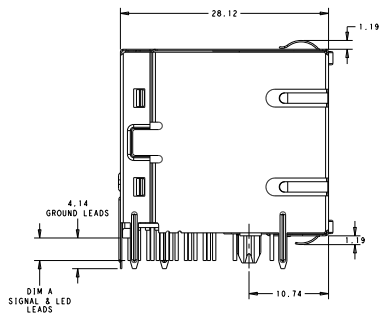
- 1. MATERIALS:**
 PLASTIC HOUSING: BLACK, THERMOPLASTIC FLAMMABILITY RATING UL 94V-0
 SHIELD: BRASS, PREPLATED WITH 0.76μm MIN SEMI-BRIGHT NICKEL,
 POST-PLATED WITH 2.54μm MIN SAC SOLDER ON SOLDER TAILS.
 CONTACTS: PHOSPHOR BRONZE, 1.27μm MIN OVERALL NICKEL UNDERPLATE,
 WITH SELECT 0.05μm MIN GOLD OVER 0.76μm MIN PALLADIUM-NICKEL AT
 MATING INTERFACES AND 2.54μm MIN SOLDER TAIL ON SOLDER TAILS.
 LED: DIFFUSED EPOXY LENS, CARBON STEEL LEAD FRAME TAILS OF LED
 ARE PREPLATED WITH 2.03μm MIN SILVER OVER 1.02μm MIN NICKEL
 UNDERPLATE OVER 0.102μm MIN COPPER UNDERPLATE, POST-PLATED WITH
 2.54μm MIN MATTE TIN AND/OR SAC SOLDER DIP OR PURE TIN SOLDER DIP
 ALL PC BOARDS: HIGH TEMPERATURE PCB,TG170°C
- △ MAGNETICS**
 APPLICATION: 100/1000/1000 BASE-T
 IMPEDANCE: 100 OHMS
 TURNS RATIO (CHIP: CABLE): 1:1 ALL FOUR PAIRS
 OPEN CIRCUIT INDUCTANCE (OCL): 350uH MIN @100KHz, 0.1VRMS,
 UNBIASED BIAS FROM 0°C TO 70°C, ALL FOUR PAIRS
 ALL FOUR PAIRS BI-DIRECTIONAL
 PERFORMANCE @ 25°C:
 INSERTION LOSS (IL): 1.1dB MAX FROM 0.5MHz TO 100MHz
 RETURN LOSS (RL): 18dB MIN FROM 0.5MHz TO 40MHz
 12-20LOG(f/80)dB MIN FROM 40.1MHz TO 100MHz
 CROSSTALK ATTENUATION: 35dB MIN FROM 0.5MHz TO 40MHz
 33-20LOG(f/50)dB MIN FROM 40.1MHz TO 100MHz
 COMMON MODE REJECTION RATIO (CMRR): 30dB MIN FROM 0.5MHz TO 100MHz
 ISOLATION VOLTAGE: 2250VDC(MAX) FOR 60 SECONDS WITH A RISE TIME OF
 500V/SEC AND WITH ALL PORTS CONNECTED.
- △ PART NUMBER, DATE CODE AND COUNTRY OF ORIGIN ARE**
 LOCATED IN APPENDIX A AND SHOWN AS DATE CODE "YY" IS YEAR,
 "WW" IS WEEK, "D" IS DAY OF WEEK, WITH SUNDAY=1.
- △ TRP LOGO AND AGENCY APPROVAL LOGO ARE**
 LOCATED IN APPROXIMATE AREA SHOWN.
5. OPERATING TEMP: FROM 0°C TO +70°C.
6. RJ45 CAVITY CONFORMS TO FCC RULES AND REGULATION PART 68 SUBPART F.
- △ INDICATED MAGNETIC CONNECTIONS ARE SYMMETRICAL AND**
 SUPPORT AUTO-MD/MDX.
- △ DATUM AND BASIC DIMENSION ESTABLISHED BY CUSTOMER.**
- △ BASIC DIMENSION ESTABLISHED BY CUSTOMER, BUT MAY NOT BE**
 GREATER THAN 5.08mm.
- △ LEDS ARE DRIVEN WITH CONSTANT CURRENT AT APPROX 20mA**
 LED COLOR: WAVELENGTH (X.D): GREEN, 568 nm TYP. @ IF=20mA
 FORWARD VOLTAGE (VF): GREEN, 2.2V TYP. @ IF=20mA
 DOMINANT WAVELENGTH (X.D): ORANGE, 605 nm TYP. @ IF=20mA
 FORWARD VOLTAGE (VF): ORANGE, 2.1V TYP. @ IF=20mA
 DOMINANT WAVELENGTH (X.D): YELLOW, 588 nm TYP. @ IF=20mA
 FORWARD VOLTAGE (VF): YELLOW 2.1V TYP. @ IF=20mA
- II. THE PARTS ARE RECOMMENDED FOR WAVE SOLDERING PROCESS,**
 PEAK TEMPERATURE 260°C MAX, 10 SECONDS MAX.

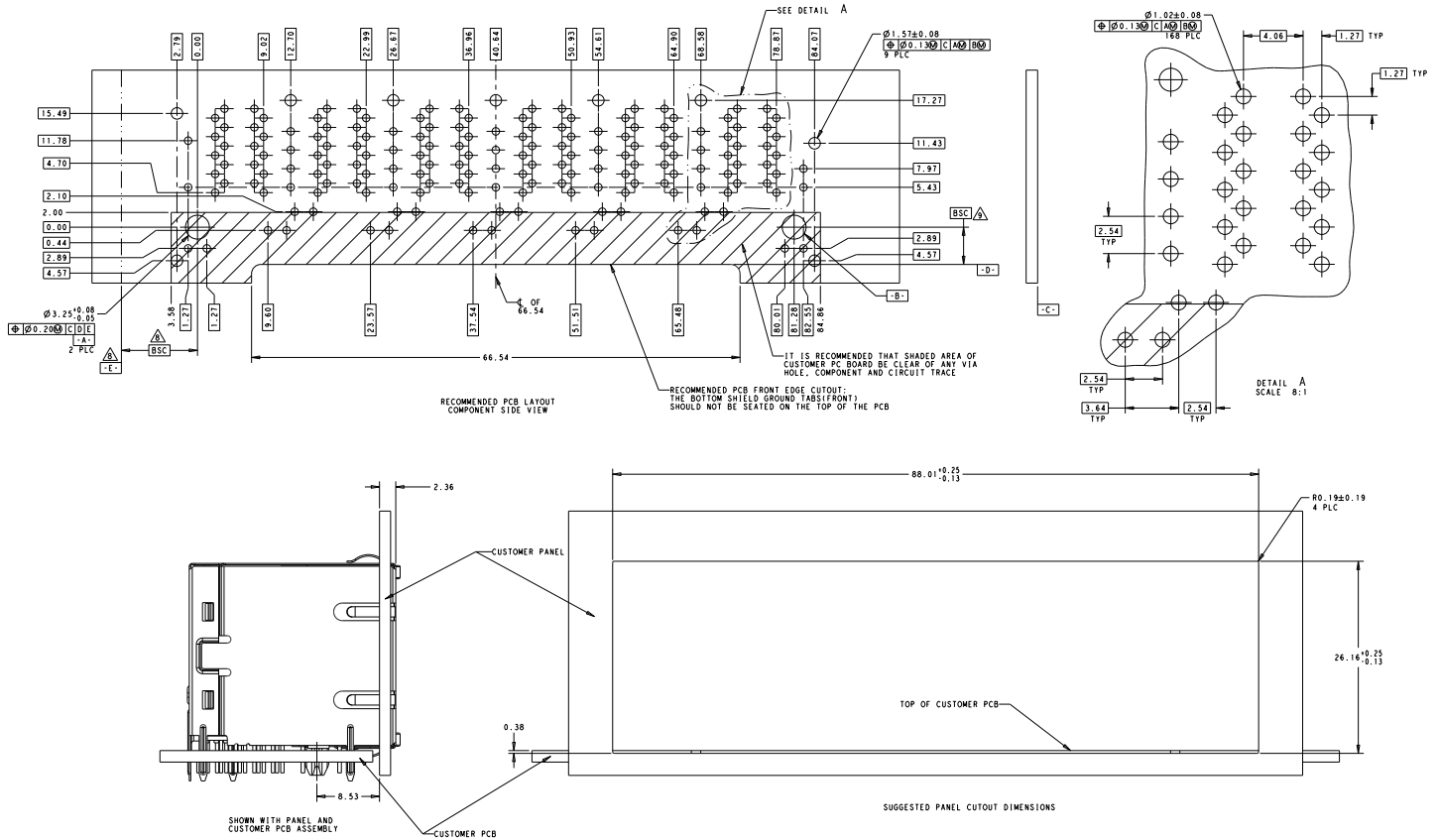
SEE SHEET 3	2.40	GRN/VLT	GRN/VLT	GRN/VLT	GRN/VLT	3-1840326-1
SEE SHEET 3	2.40	GREEN	GREEN	GREEN	GREEN	3-1840326-1
SEE SHEET 3	3.04	GRN/VLT	GRN/VLT	GRN/VLT	GRN/VLT	3-1840326-1
SEE SHEET 3	3.04	GRN/VLT	GRN/VLT	GRN/VLT	GRN/VLT	1840326-1
SEE SHEET 3	3.04	GRN/VLT	GRN/VLT	GRN/VLT	GRN/VLT	1840326-1
SEE SHEET 3	3.56	GRN/VLT	GRN/VLT	GRN/VLT	GRN/VLT	1-1840326-4
SEE SHEET 3	3.56	GREEN	GREEN	GREEN	GREEN	1-1840326-4
SEE SHEET 3	3.04	GREEN	GREEN	GREEN	GREEN	1840326-1
OUTLINE DIMENSION	BOTTOM LED 2 TOP LED 1		TOP LED 2 TOP LED 1		NUMBER	
THIS DRAWING IS A CONTROLLED DOCUMENT				DONGGUAN CHINA		
						
MAG JACK		MAG JACK		MAG JACK		
STACK NON-PO		STACK NON-PO		STACK NON-PO		
CUSTOMER DRAWING		CUSTOMER DRAWING		CUSTOMER DRAWING		
DATE		DATE		DATE		
18-10-0404		18-10-0404		18-10-0404		

THIS SHEET FOR 2-1840326-7 ONLY



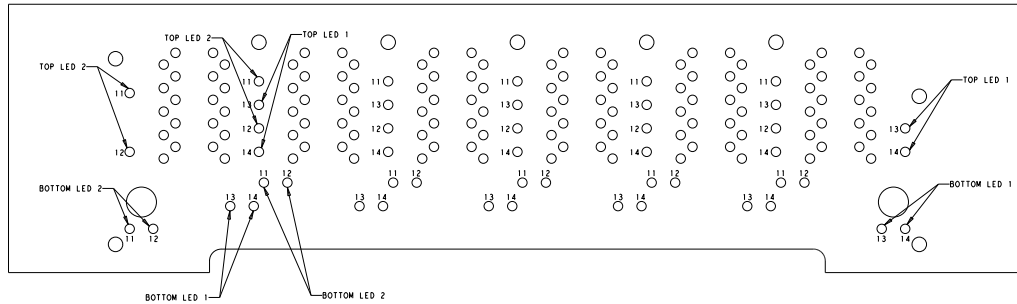
THIS DRAWING IS A CONTROLLED DOCUMENT		REV	DATE	REVISION
DRAWING		1	2016-11-14	1
APP		2	2016-11-14	2
DESIGN		3	2016-11-14	3
CHECK		4	2016-11-14	4
PRODUCT SPEC		5	2016-11-14	5
100-184004		6	2016-11-14	6
APPLICATION SPEC		7	2016-11-14	7
CUSTOMER DRAWING		8	2016-11-14	8
2X6 S8656 GIGABIT W/ LED		MAGJACK		
STACK Non-PoE		1840326		
SCALE		NTS	SHEET	2 OF 2
DRAWN BY		NTS	DATE	2016-11-14

[illegible]

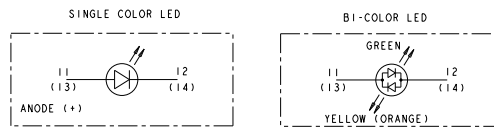


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DATE	2018-01-15	DATE	2018-01-15
DESIGNER	WANG, JIN	DATE	2018-01-15
PRODUCT SPEC	184-184004	DATE	2018-01-15
APPLICATION SPEC		DATE	2018-01-15
CUSTOMER DRAWING		DATE	2018-01-15

		2X6 S8656 GIGABIT W/ LED
MAGJACK		2X6 S8656 GIGABIT W/ LED
STACK Non-PoE		2X6 S8656 GIGABIT W/ LED
1840326		2X6 S8656 GIGABIT W/ LED
CUSTOMER DRAWING		2X6 S8656 GIGABIT W/ LED



LED HOLE DESIGNATIONS
VIEWED FROM COMPONENT SIDE



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DRAWING NO.		DATE	DATE
REV.		DATE	DATE
PRODUCT SPEC		100-184004	
APPLICATION SPEC			
CUSTOMER DRAWING			
MAGJACK		2X6 S8656 GIGABIT W/ LED	
STACK Non-PoE			
A1			
1840326			
SCALE		NTS	
SHEET		5	
OF		5	
REV			