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PMDPB38UNE

20 V dual N-channel Trench MOSFET

26 September 2012

Product data sheet

1. Product profile

1.1 General description

Dual N-channel enhancement mode Field-Effect Transistor (FET) in a leadless medium power DFN2020-6 (SOT1118) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

1.2 Features and benefits

- Very fast switching
- Trench MOSFET technology
- Leadless medium power SMD plastic package: 2 × 2 × 0.6 mm
- Exposed drain pad for excellent thermal conduction
- ESD protection up to 1.6 kV

1.3 Applications

- Charging switch for portable devices
- DC-to-DC converters
- Small brushless DC motor drive
- Power management in battery-driven portables
- Hard disk and computing power management

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	-	20	V
V_{GS}	gate-source voltage		-8	-	8	V
I_D	drain current	$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$	[1]	-	5	A
Static characteristics (per transistor)						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 3\text{ A}; T_j = 25\text{ °C}$	-	38	46	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².



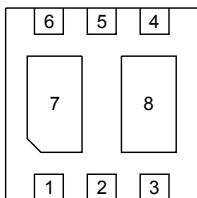
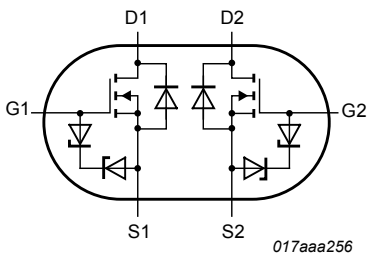
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2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1	 <p>Transparent top view DFN2020-6 (SOT1118)</p>	 <p>017aaa256</p>
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1		
7	D1	drain TR1		
8	D2	drain TR2		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMDPB38UNE	DFN2020-6	plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm	SOT1118

4. Marking

Table 4. Marking codes

Type number	Marking code
PMDPB38UNE	1S

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V_{DS}	drain-source voltage	$T_j = 25\text{ }^{\circ}\text{C}$		-	20	V
V_{GS}	gate-source voltage			-8	8	V
I_D	drain current	$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}; t \leq 5\text{ s}$	[1]	-	5	A
		$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	4	A
		$V_{GS} = 4.5\text{ V}; T_{amb} = 100\text{ }^{\circ}\text{C}$	[1]	-	2.6	A
I_{DM}	peak drain current	$T_{amb} = 25\text{ }^{\circ}\text{C}; \text{single pulse}; t_p \leq 10\text{ }\mu\text{s}$		-	16	A

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Symbol	Parameter	Conditions		Min	Max	Unit
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	510	mW
			[1]	-	1.2	W
		T _{sp} = 25 °C		-	6.25	W
Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	1.1	A
Per device						
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
ESD maximum rating						
V _{ESD}	electrostatic discharge voltage	HBM	[3]	-	1600	V

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[3] Measured between all pins.

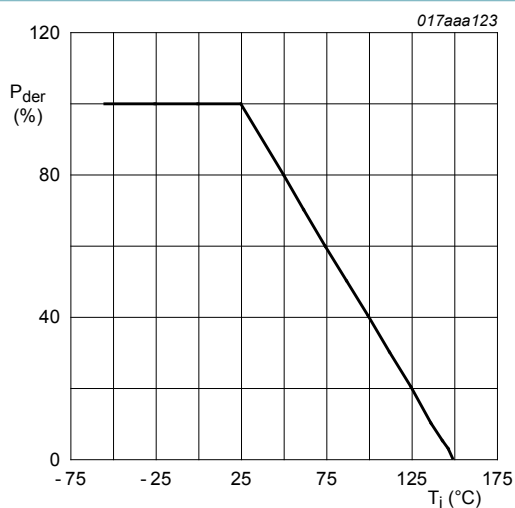


Fig. 1. Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100 \%$$

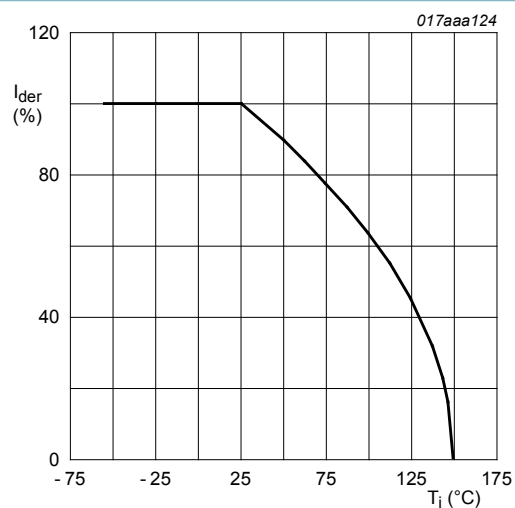


Fig. 2. Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100 \%$$

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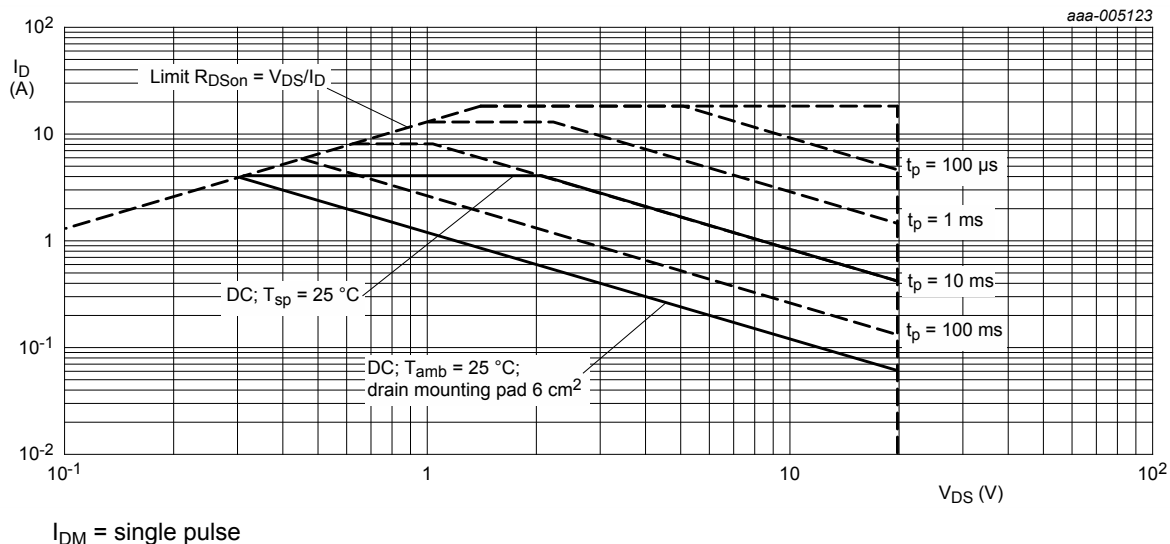


Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	212	245	K/W
			[2]	-	90	105	K/W
		in free air; $t \leq 5\text{ s}$	[2]	-	56	65	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	11	20	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm^2 .

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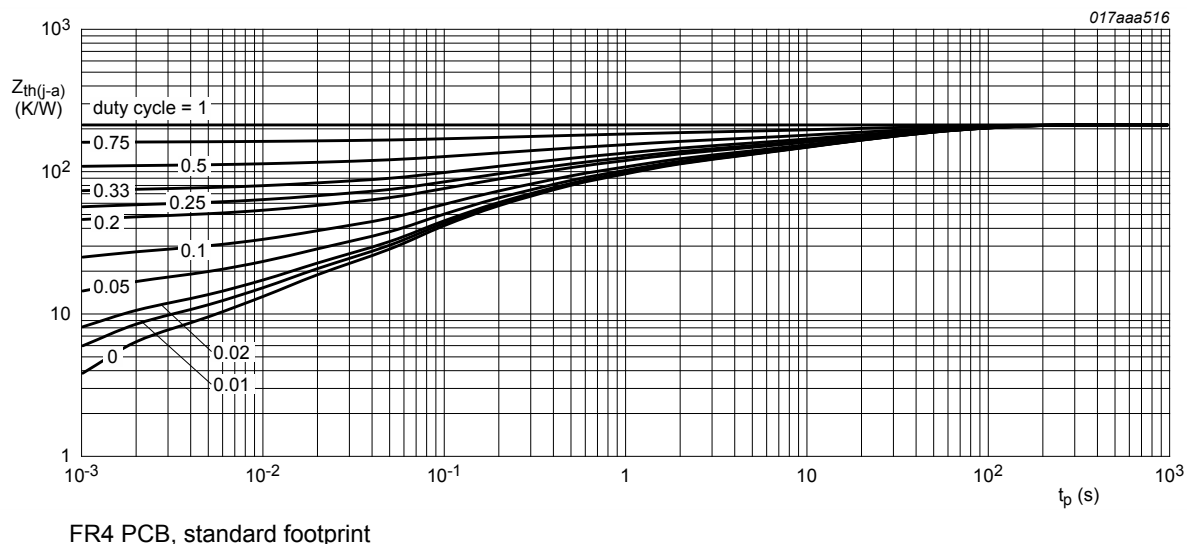


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

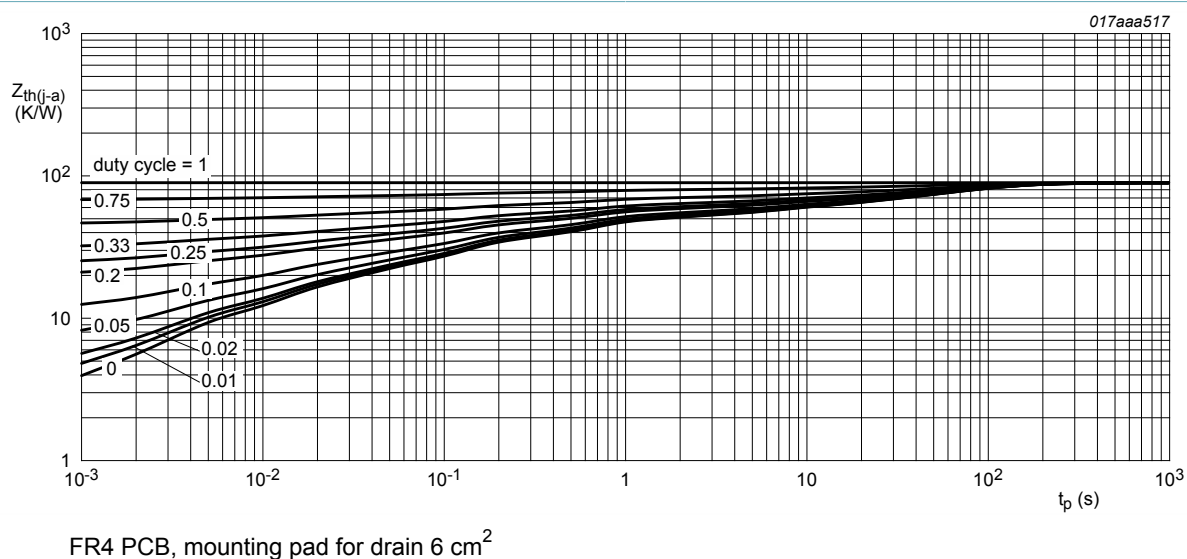


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics (per transistor)						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_j = 25 ^\circ C$	20	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 250 \mu A$; $V_{DS} = V_{GS}$; $T_j = 25 ^\circ C$	0.4	0.7	1	V
I_{DSS}	drain leakage current	$V_{DS} = 20 V$; $V_{GS} = 0 V$; $T_j = 25 ^\circ C$	-	-	1	μA
I_{GSS}	gate leakage current	$V_{GS} = 8 V$; $V_{DS} = 0 V$; $T_j = 25 ^\circ C$	-	-	10	μA

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_{GS} = -8 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^{\circ}\text{C}$	-	-	-10	μA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 3 \text{ A}; T_j = 25 \text{ }^{\circ}\text{C}$	-	38	46	$\text{m}\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 3 \text{ A}; T_j = 150 \text{ }^{\circ}\text{C}$	-	59	72	$\text{m}\Omega$
		$V_{GS} = 2.5 \text{ V}; I_D = 3 \text{ A}; T_j = 25 \text{ }^{\circ}\text{C}$	-	52	61	$\text{m}\Omega$
		$V_{GS} = 1.8 \text{ V}; I_D = 2 \text{ A}; T_j = 25 \text{ }^{\circ}\text{C}$	-	65	90	$\text{m}\Omega$
g_{fs}	forward transconductance	$V_{DS} = 10 \text{ V}; I_D = 3 \text{ A}; T_j = 25 \text{ }^{\circ}\text{C}$	-	10	-	S

Dynamic characteristics (per transistor)

$Q_{G(tot)}$	total gate charge	$V_{DS} = 10 \text{ V}; I_D = 4 \text{ A}; V_{GS} = 4.5 \text{ V}; T_j = 25 \text{ }^{\circ}\text{C}$	-	2.9	4.4	nC
Q_{GS}	gate-source charge		-	0.47	-	nC
Q_{GD}	gate-drain charge		-	0.7	-	nC
C_{iss}	input capacitance	$V_{DS} = 10 \text{ V}; f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^{\circ}\text{C}$	-	268	-	pF
C_{oss}	output capacitance		-	70	-	pF
C_{rss}	reverse transfer capacitance		-	39	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 10 \text{ V}; I_D = 4 \text{ A}; V_{GS} = 4.5 \text{ V}; R_{G(ext)} = 6 \text{ }\Omega; T_j = 25 \text{ }^{\circ}\text{C}$	-	6	-	ns
t_r	rise time		-	15	-	ns
$t_{d(off)}$	turn-off delay time		-	13	-	ns
t_f	fall time		-	10	-	ns

Source-drain diode (per transistor)

V_{SD}	source-drain voltage	$I_S = 0.7 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^{\circ}\text{C}$	-	0.67	1.2	V
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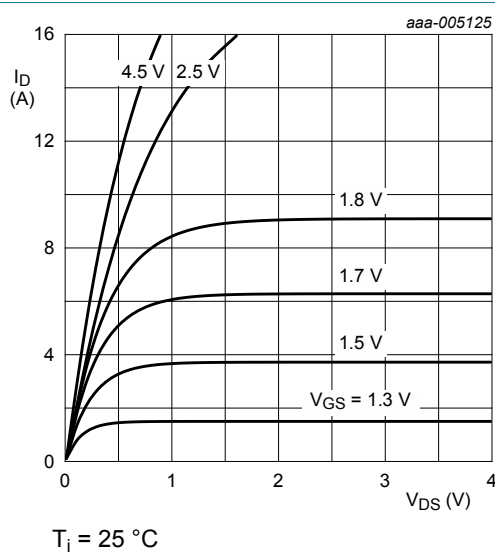


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

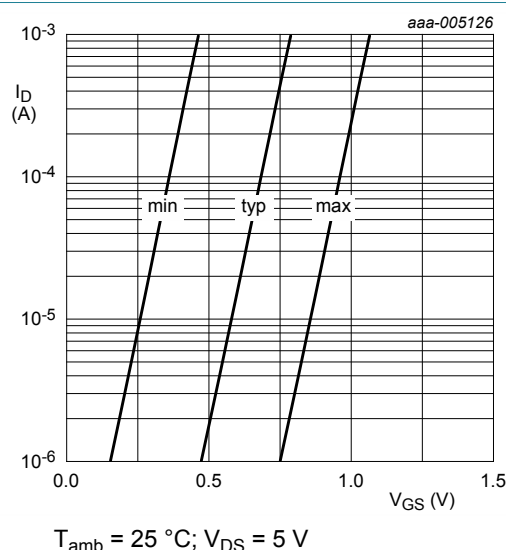


Fig. 7. Subthreshold drain current as a function of gate-source voltage

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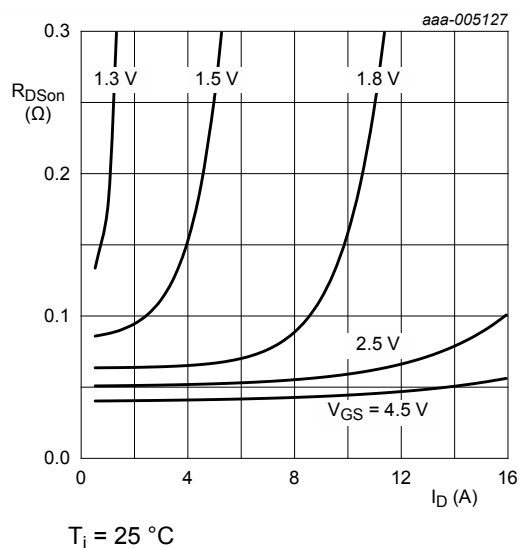


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

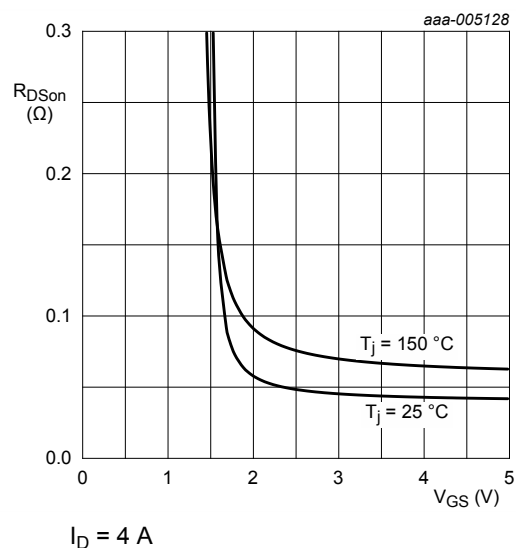


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

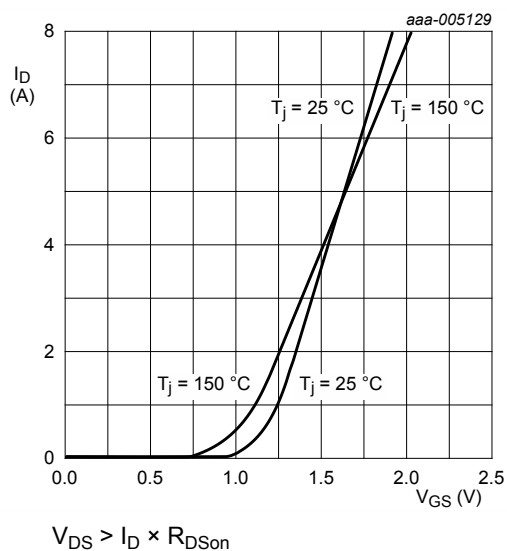


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

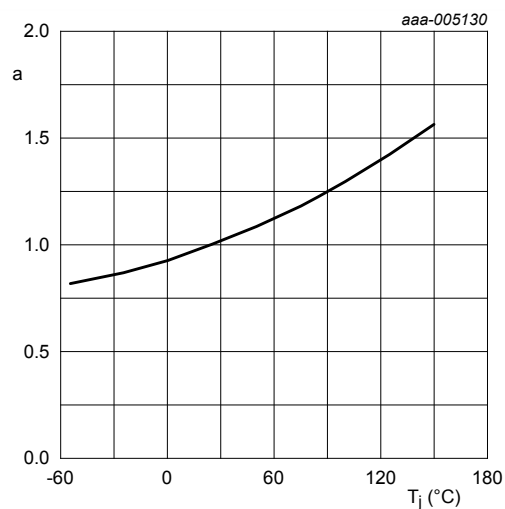


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ C)}}$$

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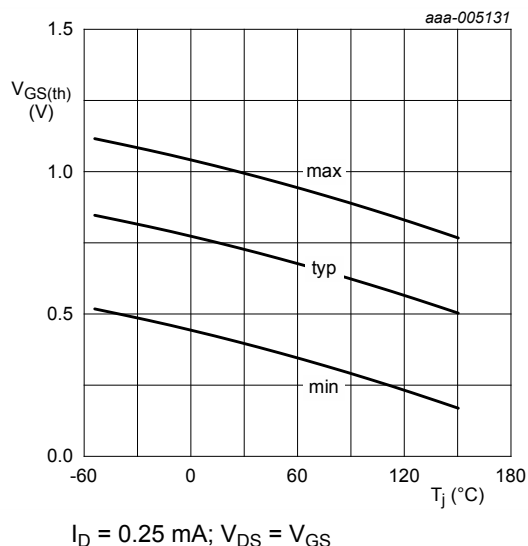


Fig. 12. Gate-source threshold voltage as a function of junction temperature

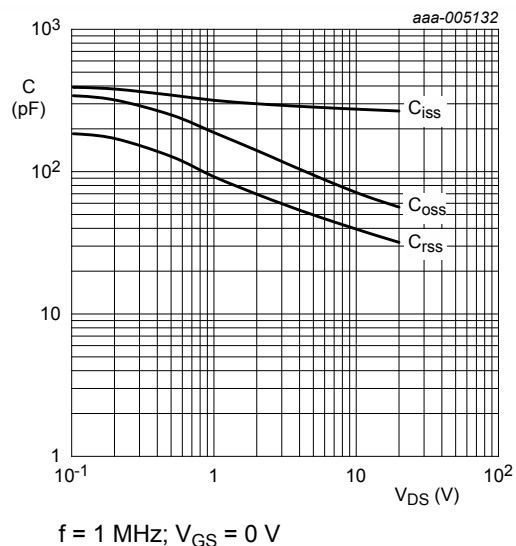


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

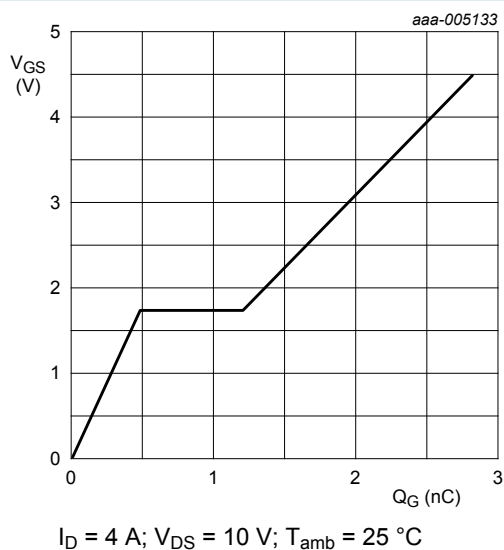


Fig. 14. Gate-source voltage as a function of gate charge; typical values

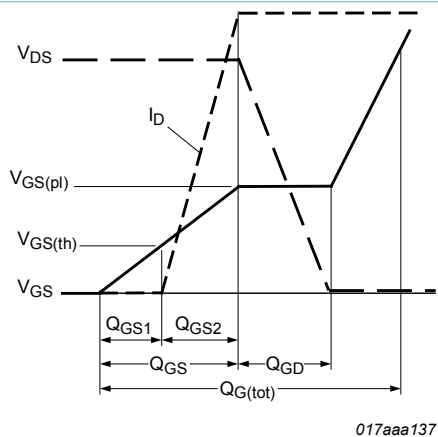
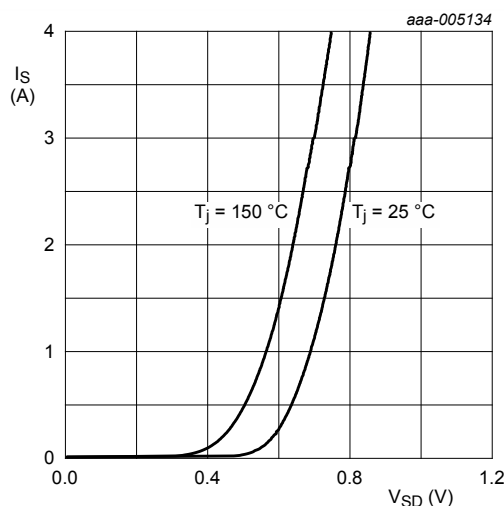


Fig. 15. Gate charge waveform definitions

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$V_{GS} = 0\text{ V}$

Fig. 16. Source current as a function of source-drain voltage; typical values

8. Test information

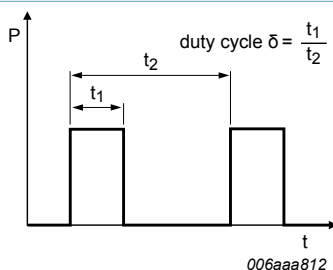


Fig. 17. Duty cycle definition

9. Package outline

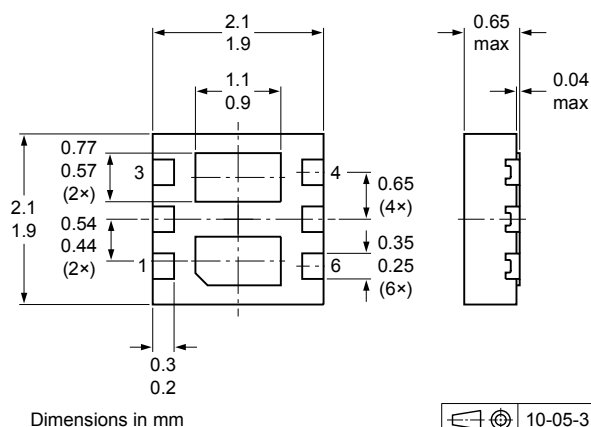


Fig. 18. Package outline DFN2020-6 (SOT1118)

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10. Soldering

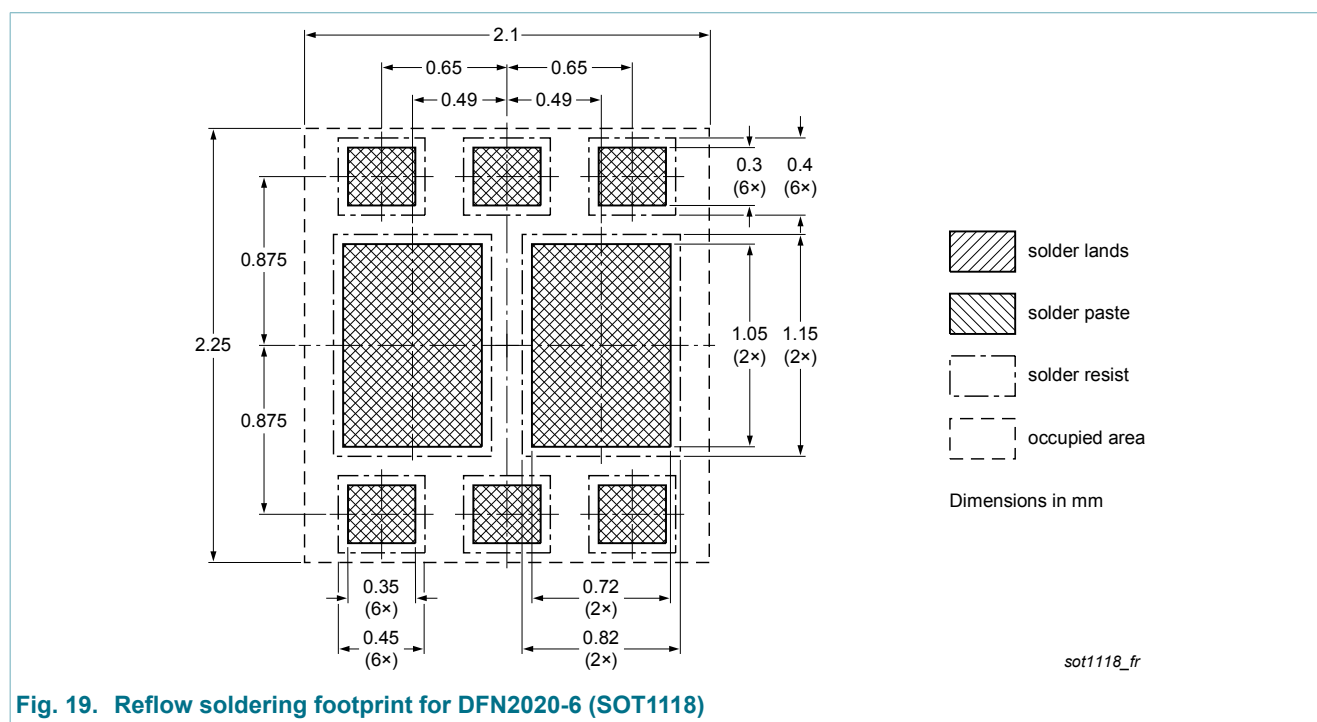


Fig. 19. Reflow soldering footprint for DFN2020-6 (SOT1118)

11. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMDPB38UNE v.1	20120926	Product data sheet	-	-

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12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 26 September 2012