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PMPB10XNE

20 V, single N-channel Trench MOSFET

30 November 2012

Product data sheet

1. Product profile

1.1 General description

N-channel enhancement mode Field-Effect Transistor (FET) in a leadless medium power DFN2020MD-6 (SOT1220) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

1.2 Features and benefits

- 2.2 kV ESD protection
- Small and leadless ultra thin SMD plastic package: 2 x 2 x 0.65 mm
- Exposed drain pad for excellent thermal conduction
- Tin-plated, 100% solderable side pads for optical solder inspection

1.3 Applications

- Charging switch for portable devices
- DC-to-DC converters
- Power management in battery-driven portables
- Hard disk and computing power management

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$		-	-	20	V
V_{GS}	gate-source voltage			-12	-	12	V
I_D	drain current	$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$	[1]	-	-	12.9	A
Static characteristics							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 9\text{ A}; T_j = 25\text{ °C}$		-	10	14	mΩ

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².



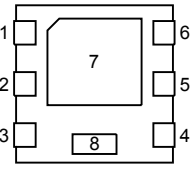
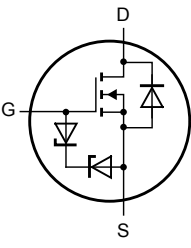
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2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	 <p>Transparent top view DFN2020MD-6 (SOT1220)</p>	 <p>017aaa255</p>
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		
7	D	drain		
8	S	source		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMPB10XNE	DFN2020MD-6	plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals	SOT1220

4. Marking

Table 4. Marking codes

Type number	Marking code
PMPB10XNE	1H

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ }^{\circ}\text{C}$		-	20	V
V_{GS}	gate-source voltage			-12	12	V
I_D	drain current	$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}; t \leq 5\text{ s}$	[1]	-	12.9	A
		$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	9	A
		$V_{GS} = 4.5\text{ V}; T_{amb} = 100\text{ }^{\circ}\text{C}$	[1]	-	5.7	A
I_{DM}	peak drain current	$T_{amb} = 25\text{ }^{\circ}\text{C}; \text{single pulse}; t_p \leq 10\text{ }\mu\text{s}$		-	36	A
P_{tot}	total power dissipation	$T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	1.7	W

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Symbol	Parameter	Conditions		Min	Max	Unit
		$T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$	[1]	-	3.5	W
		$T_{sp} = 25\text{ °C}$		-	12.5	W
T_j	junction temperature			-55	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
Source-drain diode						
I_S	source current	$T_{amb} = 25\text{ °C}$	[1]	-	2	A
ESD maximum rating						
V_{ESD}	electrostatic discharge voltage	HBM	[2]	-	2200	V

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².

[2] Measured between all pins.

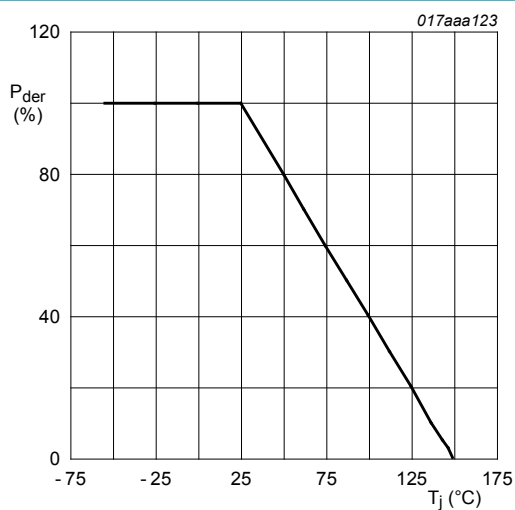


Fig. 1. Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$

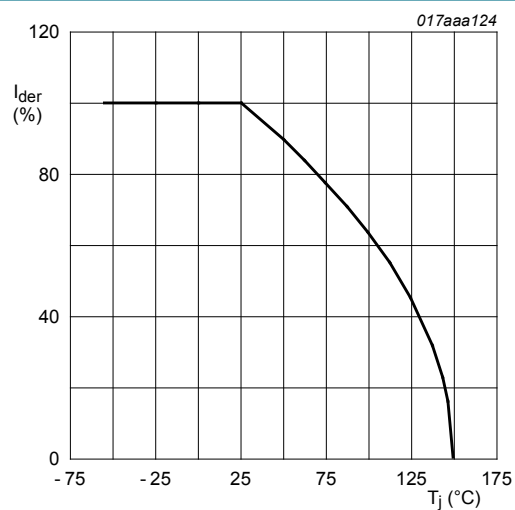


Fig. 2. Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100\%$$

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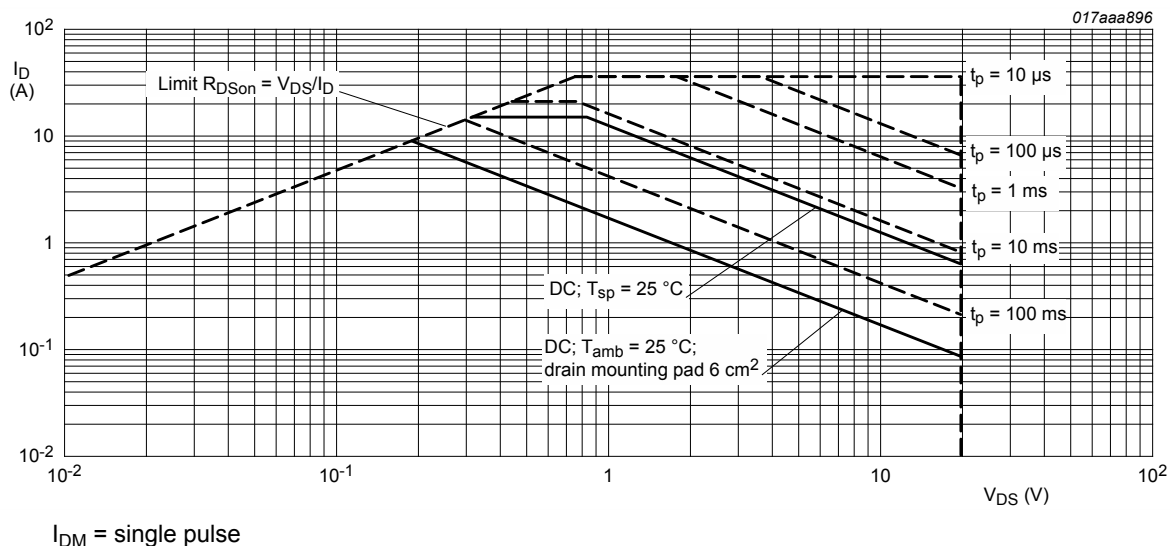


Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	235	270	K/W
			[2]	-	67	74	K/W
		in free air; $t \leq 5\text{ s}$	[2]	-	33	36	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	5	10	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm^2 .

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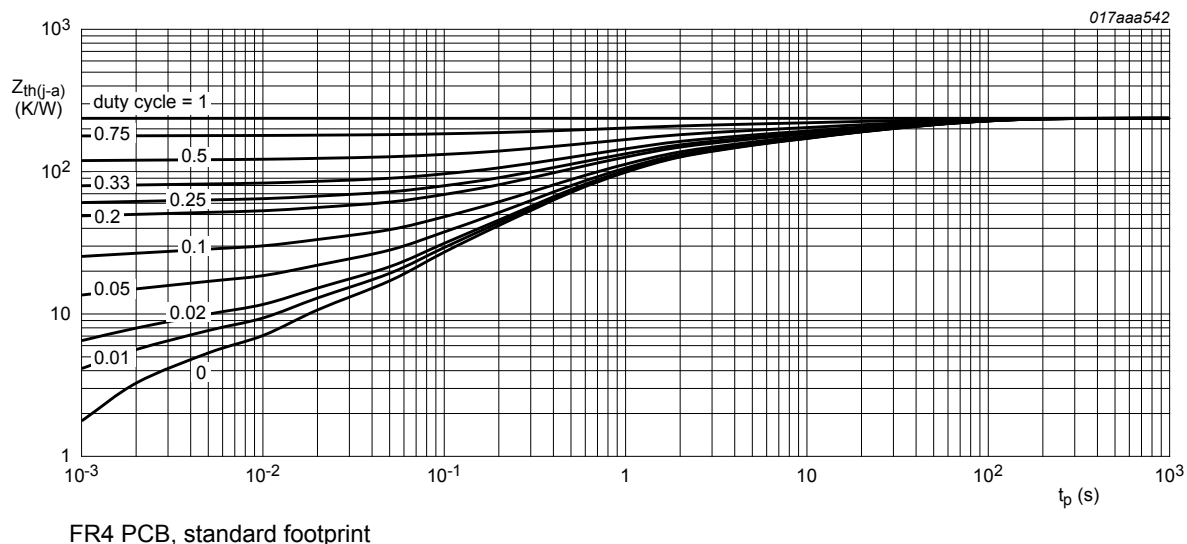


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

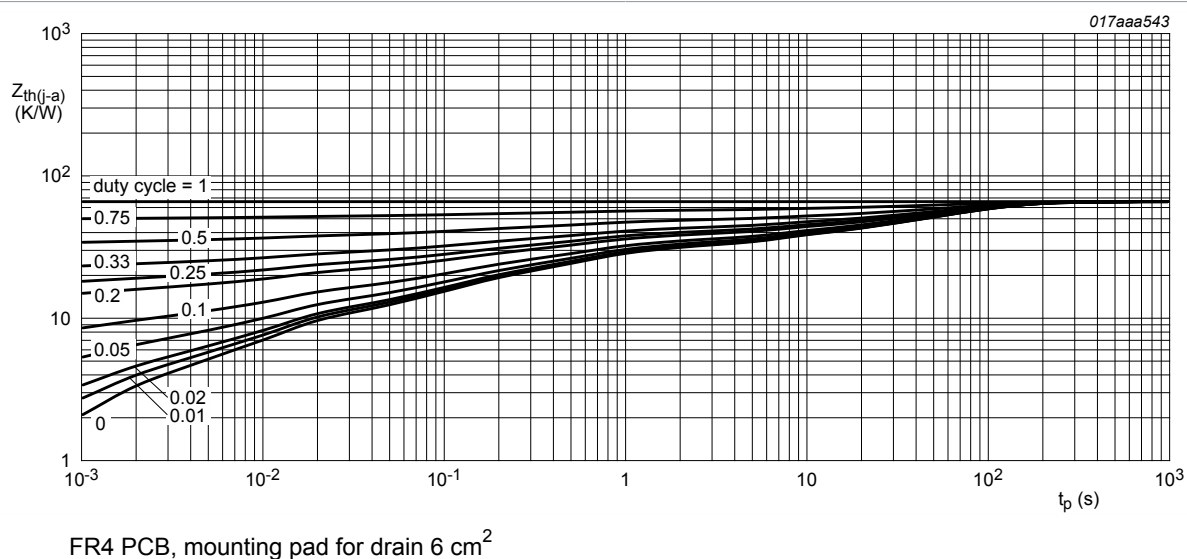


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$		20	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 250\text{ }\mu\text{A}$; $V_{DS} = V_{GS}$; $T_j = 25\text{ }^\circ\text{C}$		0.4	0.65	0.9	V
I_{DSS}	drain leakage current	$V_{DS} = 20\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$		-	-	1	μA
I_{GSS}	gate leakage current	$V_{GS} = 8\text{ V}$; $V_{DS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$		-	-	10	μA

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		$V_{GS} = -8 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^{\circ}\text{C}$		-	-	-10	μA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 9 \text{ A}; T_j = 25 \text{ }^{\circ}\text{C}$		-	10	14	$\text{m}\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 9 \text{ A}; T_j = 150 \text{ }^{\circ}\text{C}$		-	15	21	$\text{m}\Omega$
		$V_{GS} = 2.5 \text{ V}; I_D = 8 \text{ A}; T_j = 25 \text{ }^{\circ}\text{C}$		-	12	18	$\text{m}\Omega$
		$V_{GS} = 1.8 \text{ V}; I_D = 3.7 \text{ A}; T_j = 25 \text{ }^{\circ}\text{C}$		-	16	25	$\text{m}\Omega$
g_{fs}	forward transconductance	$V_{DS} = 10 \text{ V}; I_D = 9 \text{ A}; T_j = 25 \text{ }^{\circ}\text{C}$		-	60	-	S
R_G	gate resistance	$f = 1 \text{ MHz}$		-	2	-	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	$V_{DS} = 10 \text{ V}; I_D = 6 \text{ A}; V_{GS} = 4.5 \text{ V}; T_j = 25 \text{ }^{\circ}\text{C}$		-	23	34	nC
Q_{GS}	gate-source charge			-	2.6	-	nC
Q_{GD}	gate-drain charge			-	4.5	-	nC
C_{iss}	input capacitance	$V_{DS} = 10 \text{ V}; f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^{\circ}\text{C}$		-	2175	-	pF
C_{oss}	output capacitance			-	235	-	pF
C_{rss}	reverse transfer capacitance			-	205	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 10 \text{ V}; I_D = 6 \text{ A}; V_{GS} = 4.5 \text{ V}; R_{G(ext)} = 6 \text{ }\Omega; T_j = 25 \text{ }^{\circ}\text{C}$		-	13	-	ns
t_r	rise time			-	35	-	ns
$t_{d(off)}$	turn-off delay time			-	54	-	ns
t_f	fall time			-	50	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 2 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^{\circ}\text{C}$		-	0.6	1.2	V

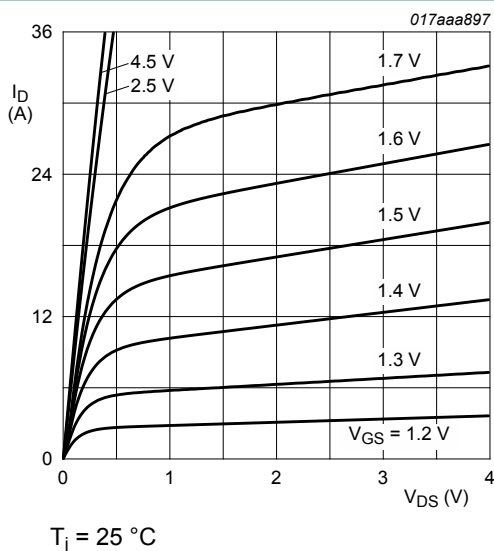


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

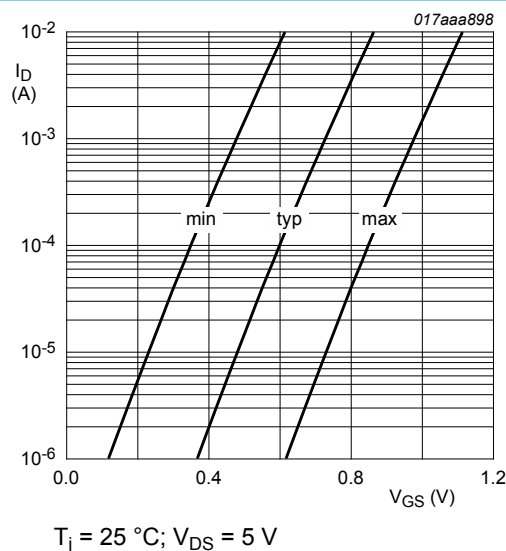


Fig. 7. Subthreshold drain current as a function of gate-source voltage

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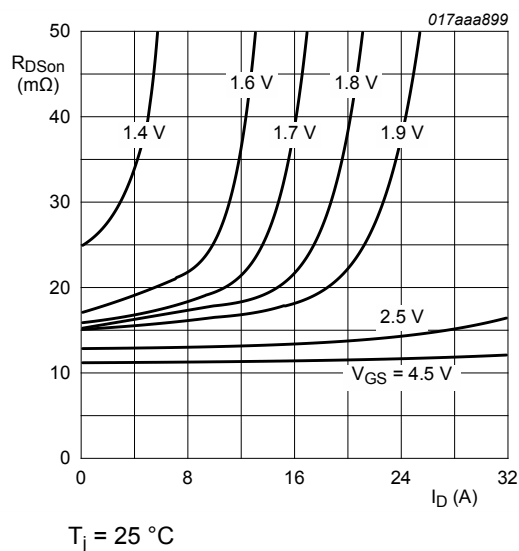


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

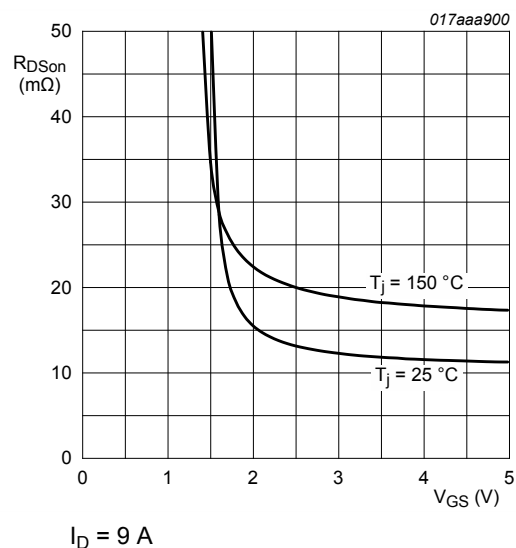


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

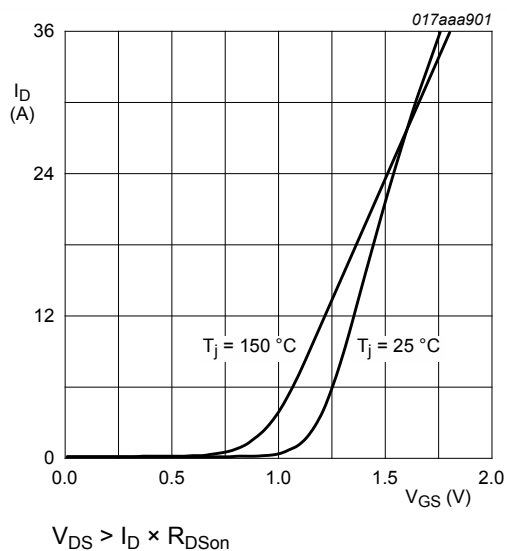


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

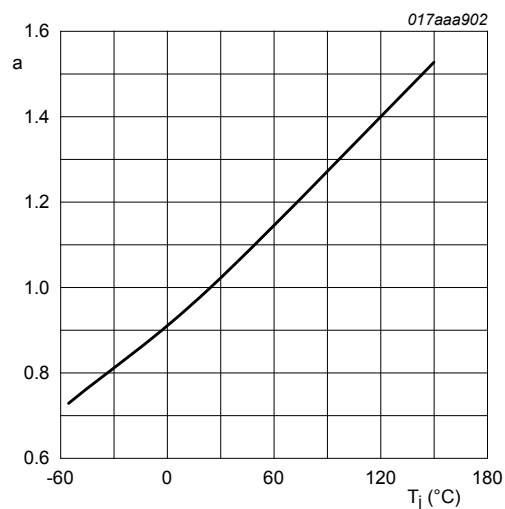


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DS(on)}}{R_{DS(on)(25\text{ °C})}}$$

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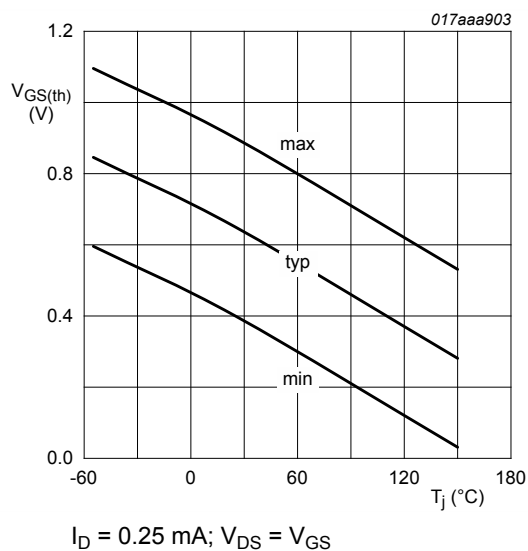


Fig. 12. Gate-source threshold voltage as a function of junction temperature

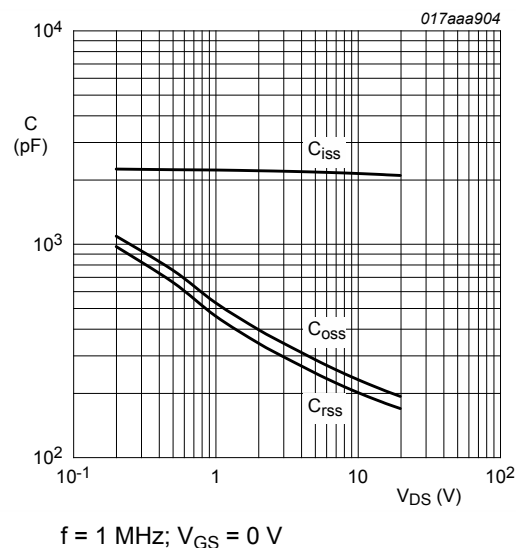


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

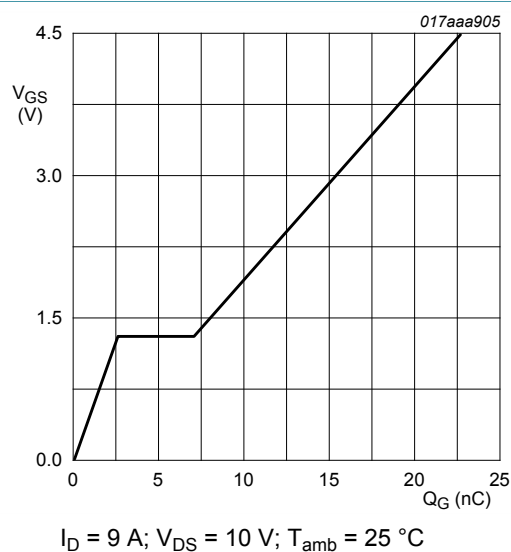


Fig. 14. Gate-source voltage as a function of gate charge; typical values

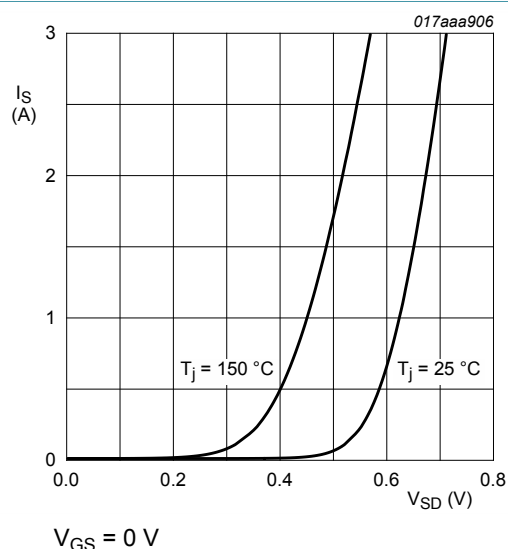


Fig. 15. Source current as a function of source-drain voltage; typical values

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8. Test information

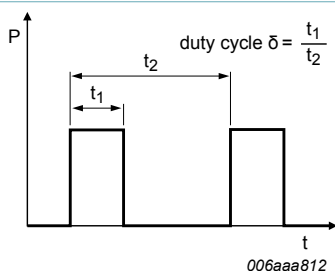


Fig. 16. Duty cycle definition

9. Package outline

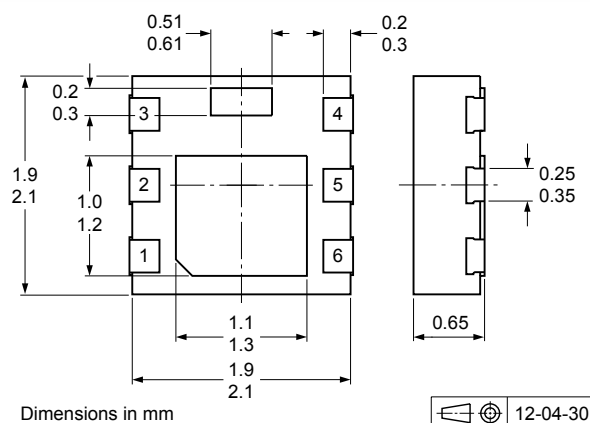


Fig. 17. Package outline DFN2020MD-6 (SOT1220)

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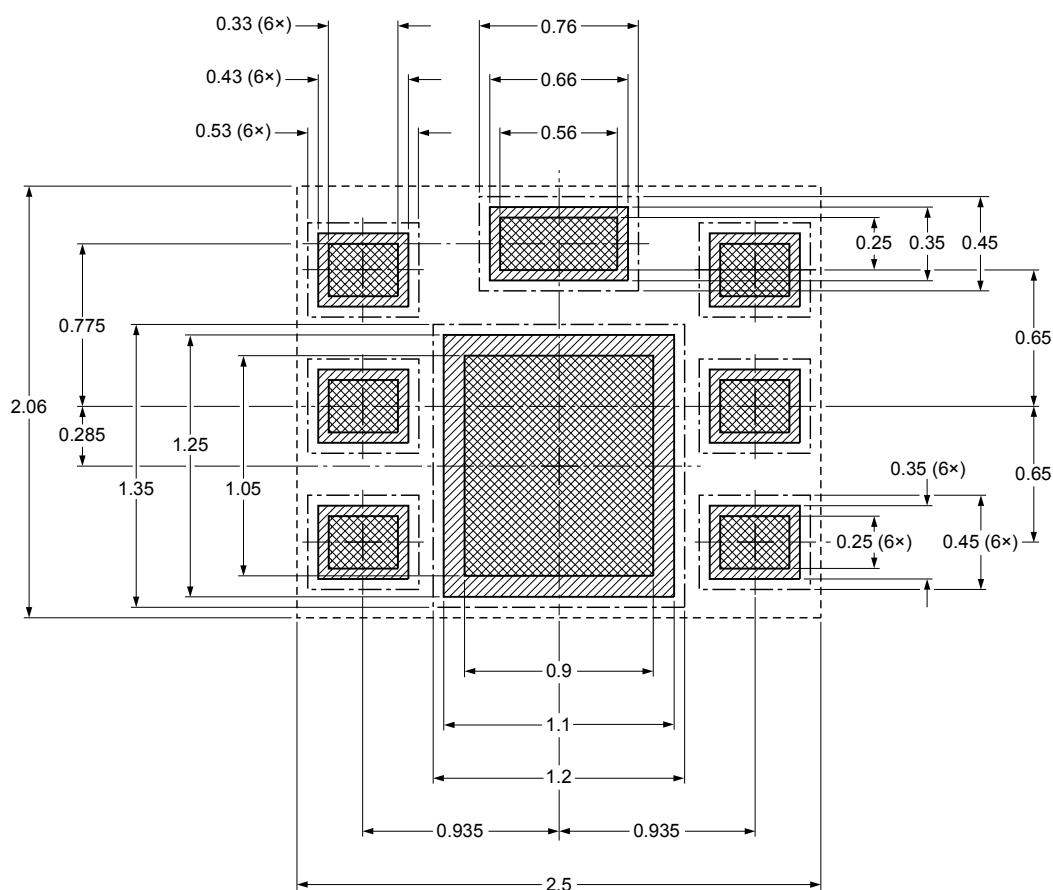
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
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10. Soldering

Footprint information for reflow soldering of DFN2020MD-6 package

SOT1220



-  solder land
 -  solder land plus solder paste
 -  solder paste deposit
 -  solder resist
 -  occupied area
- Dimensions in mm

sot1220_fr

Fig. 18. Reflow soldering footprint for DFN2020MD-6 (SOT1220)

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11. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMPB10XNE v.1	20121130	Product data sheet	-	-

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12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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