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PSMN1R9-40PL

N-channel 40 V, 1.7 mΩ logic level MOSFET in SOT78

1 February 2013

Product data sheet

1. General description

Logic level N-channel MOSFET in SOT78 using TrenchMOS technology. Product design and manufacture has been optimized for use in battery operated power tools.

2. Features and benefits

- High efficiency due to low switching & conduction losses
- Robust construction for demanding applications
- Logic level gate

3. Applications

- Battery-powered tools
- Load switching
- Motor control
- Uninterruptible power supplies

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	-	40	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 1	[1]	-	150	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 2	-	-	349	W
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11	-	1.4	1.7	mΩ
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $V_{DS} = 32\text{ V}$; Fig. 13 ; Fig. 14	-	230	-	nC
Q_{GD}	gate-drain charge		-	40.9	-	nC
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 150\text{ A}$; $V_{sup} \leq 40\text{ V}$; $R_{GS} = 50\text{ Ω}$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped; Fig. 3	-	-	801.1	mJ

[1] Continuous current is limited by package.



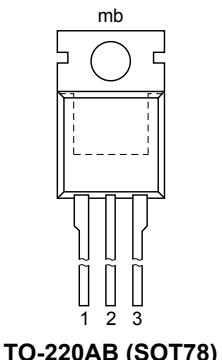
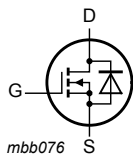
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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>TO-220AB (SOT78)</p>	 <p>mbb076</p>
2	D	drain		
3	S	source		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R9-40PL	TO-220AB	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN1R9-40PL	PSMN1R9-40PL

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ }^\circ\text{C}$; $T_j \leq 175\text{ }^\circ\text{C}$		-	40	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$		-	40	V
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	$T_{mb} = 100\text{ }^\circ\text{C}$; $V_{GS} = 10\text{ V}$; Fig. 1	[1]	-	150	A
		$T_{mb} = 25\text{ }^\circ\text{C}$; $V_{GS} = 10\text{ V}$; Fig. 1	[1]	-	150	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ }^\circ\text{C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Fig. 4		-	1332	A

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Symbol	Parameter	Conditions	Min	Max	Unit
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 2	-	349	W
T _{stg}	storage temperature		-55	175	°C
T _j	junction temperature		-55	175	°C
T _{slid(M)}	peak soldering temperature		-	260	°C
Source-drain diode					
I _S	source current	T _{mb} = 25 °C	[1]	150	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	1332	A
Avalanche ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 150 A; V _{sup} ≤ 40 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; Fig. 3	-	801.1	mJ

[1] Continuous current is limited by package.

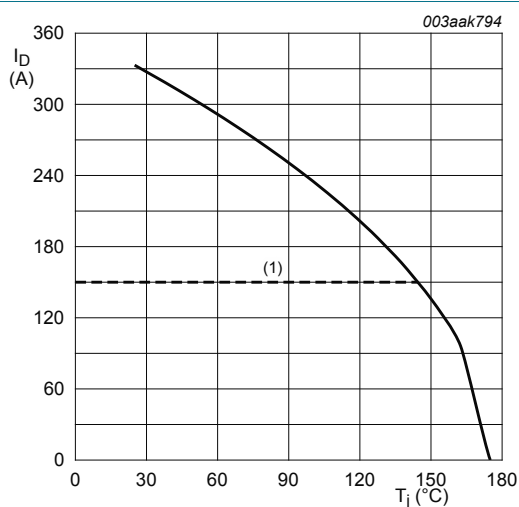


Fig. 1. Continuous drain current as a function of mounting base temperature

$$V_{GS} \geq 10V$$

(1) Capped at 150A due to package

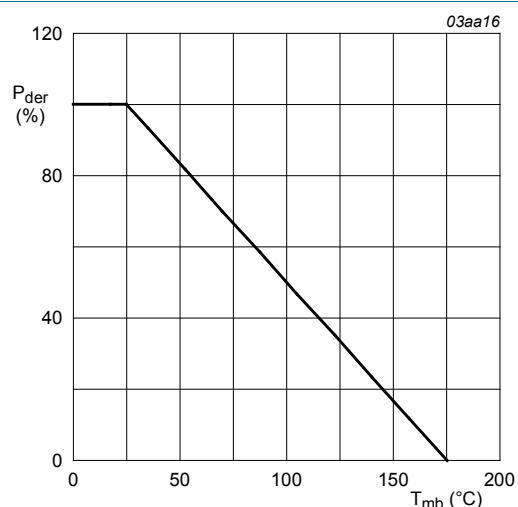


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

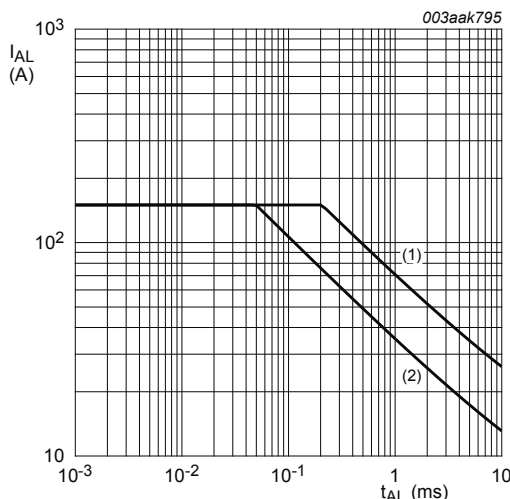


Fig. 3. Avalanche rating; avalanche current as a function of avalanche time

(1) $T_{j (init)} = 25^{\circ}C$; (2) $T_{j (init)} = 100^{\circ}C$

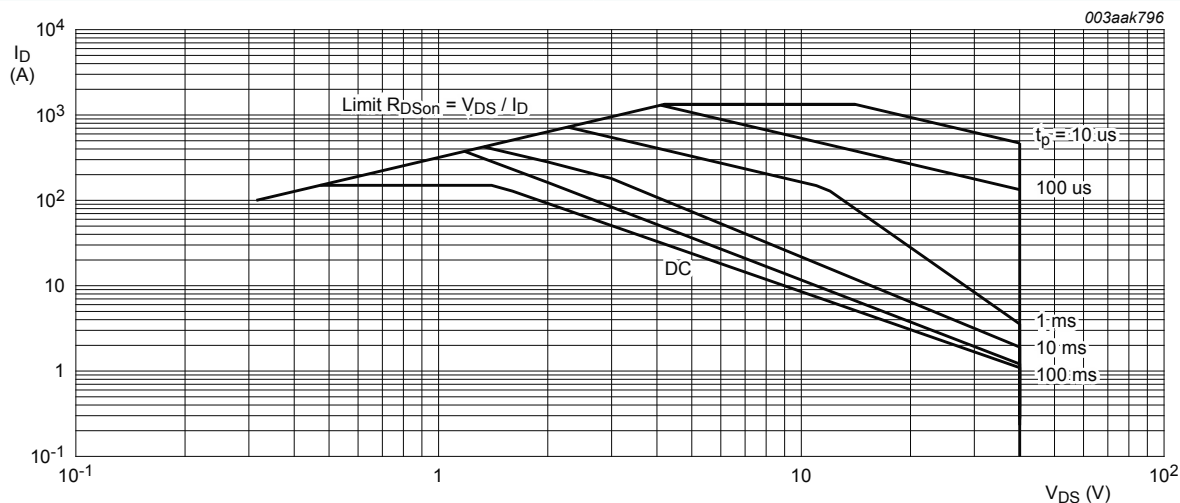


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}C$; I_{DM} is a single pulse

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.35	0.43	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in still air	-	60	-	K/W

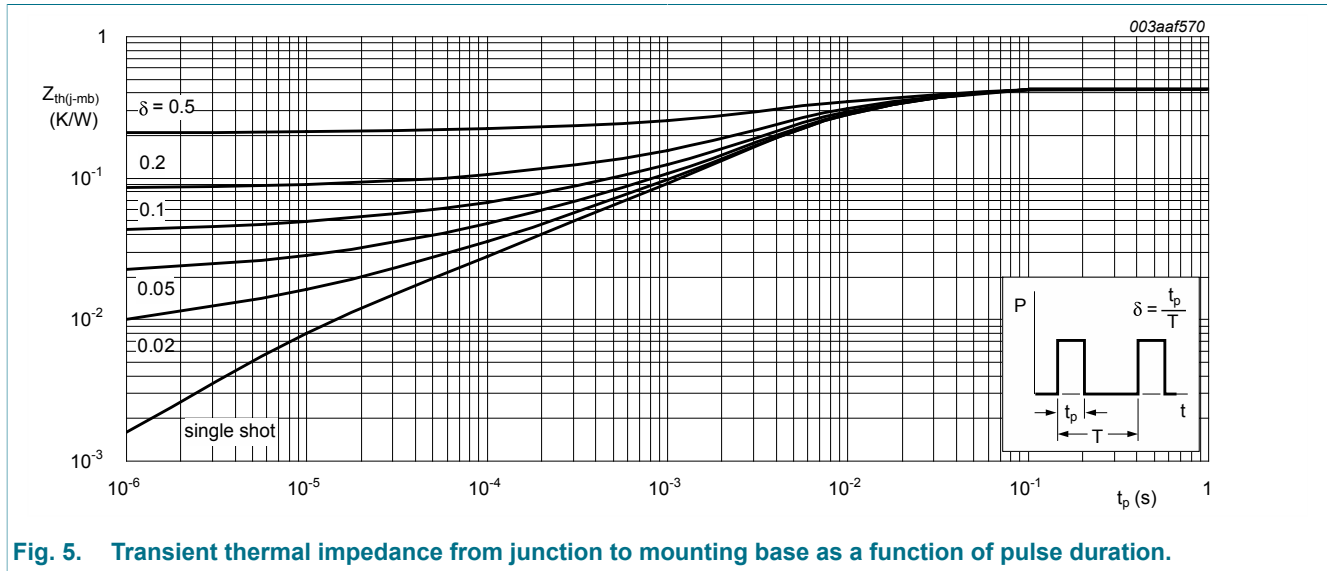


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration.

10. Characteristics

Table 7. Characteristics

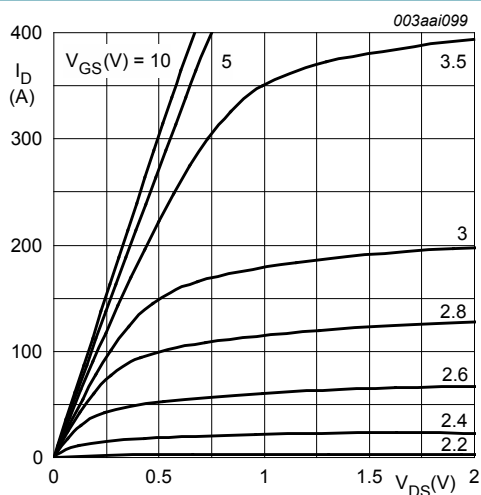
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	40	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C;$ Fig. 9; Fig. 10	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C;$ Fig. 9	-	-	2.45	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C;$ Fig. 9	0.5	-	-	V
I_{DSS}	drain leakage current	$V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	0.13	1	μA
		$V_{DS} = 40 V; V_{GS} = 0 V; T_j = 175 \text{ }^\circ C$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 25 A; T_j = 25 \text{ }^\circ C;$ Fig. 11	-	1.4	1.7	mΩ
		$V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 \text{ }^\circ C;$ Fig. 11	-	1.65	1.94	mΩ
		$V_{GS} = 10 V; I_D = 25 A; T_j = 175 \text{ }^\circ C;$ Fig. 12; Fig. 11	-	-	3.15	mΩ
R_G	gate resistance	$f = 1 \text{ MHz}$	0.38	0.76	1.52	Ω

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 32 V; V _{GS} = 5 V; Fig. 13; Fig. 14	-	120	-	nC
		I _D = 25 A; V _{DS} = 32 V; V _{GS} = 10 V; Fig. 13; Fig. 14	-	230	-	nC
Q _{GS}	gate-source charge		-	26.9	-	nC
Q _{GD}	gate-drain charge		-	40.9	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz;	-	13200	-	pF
C _{oss}	output capacitance	T _j = 25 °C; Fig. 15	-	1530	-	pF
C _{rss}	reverse transfer capacitance		-	740	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 30 V; R _L = 1.2 Ω; V _{GS} = 5 V; R _{G(ext)} = 5 Ω	-	95	-	ns
t _r	rise time		-	118	-	ns
t _{d(off)}	turn-off delay time		-	195	-	ns
t _f	fall time		-	119	-	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 16	-	0.77	1.2	V
t _{rr}	reverse recovery time	I _S = 20 A; di _S /dt = -100 A/μs; V _{GS} = 0 V;	-	57	-	ns
Q _r	recovered charge	V _{DS} = 25 V	-	97	-	nC



T_j = 25 °C; t_p = 300 μs

Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

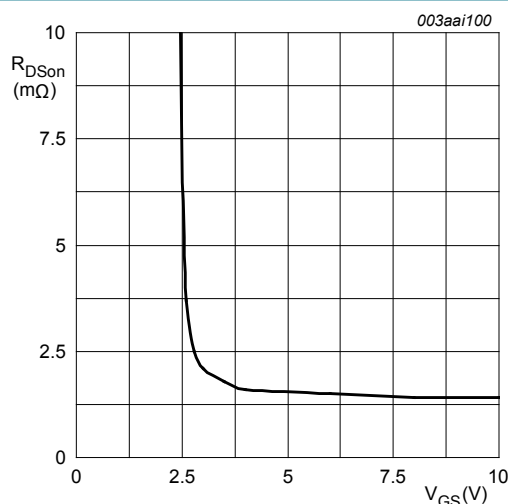


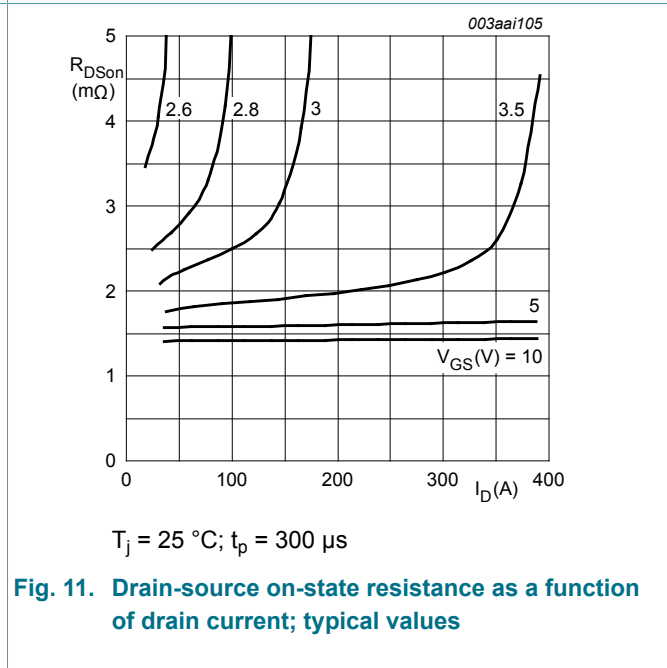
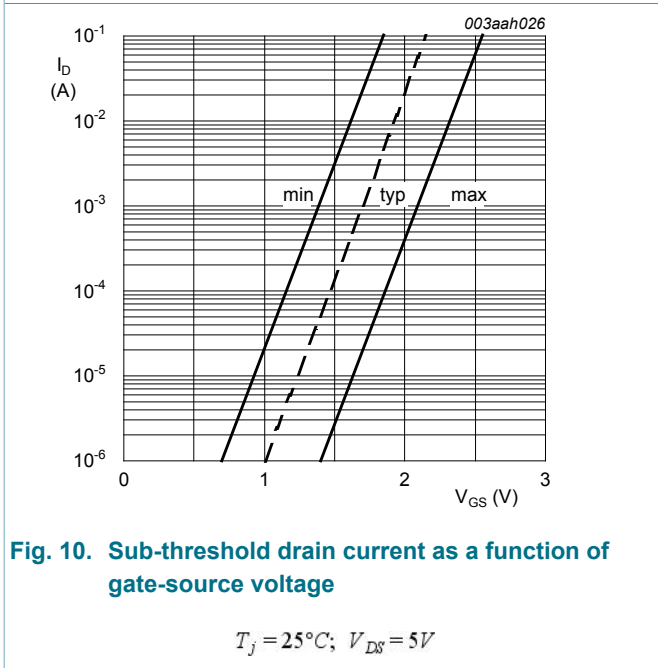
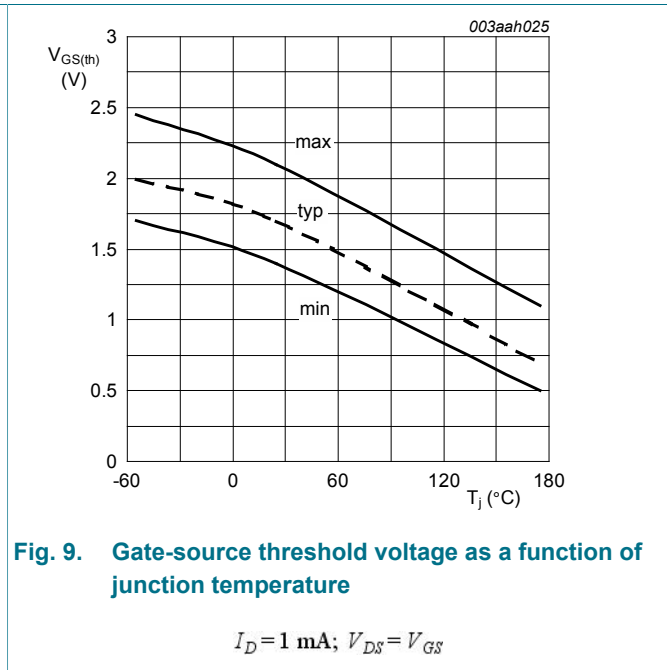
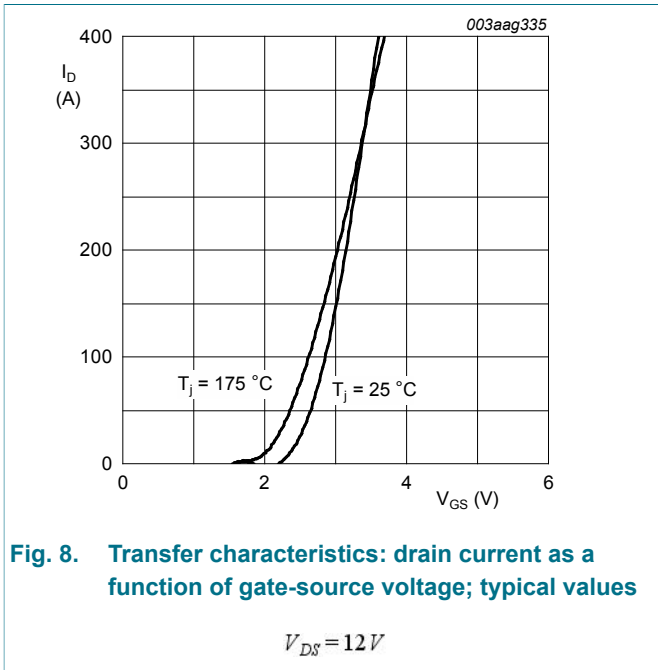
Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

T_j = 25 °C; I_D = 25 A

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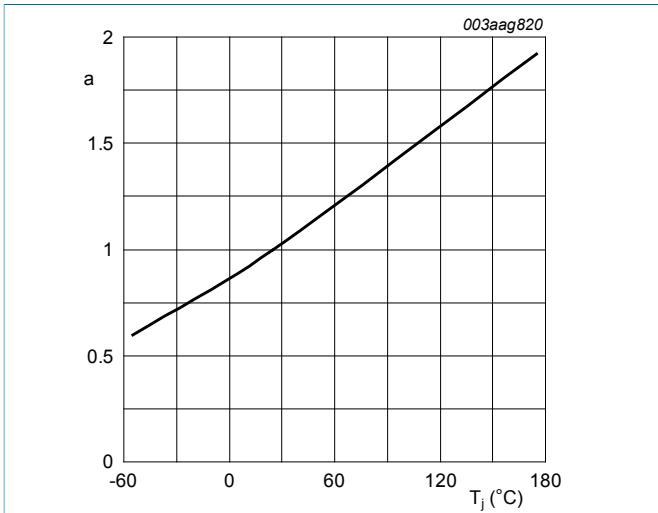


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DS(on)}}{R_{DS(on)(25\text{ }^\circ\text{C})}}$$

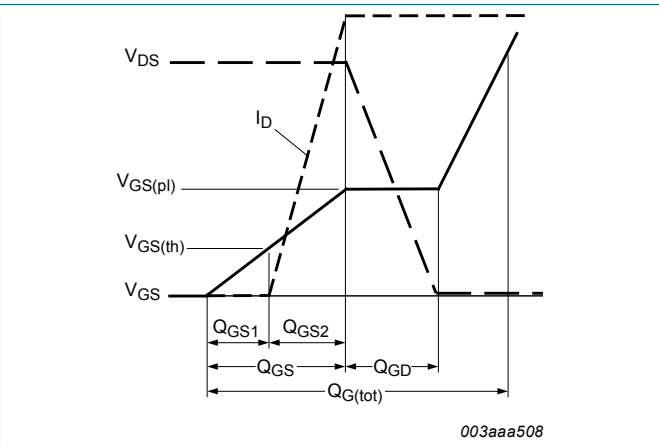
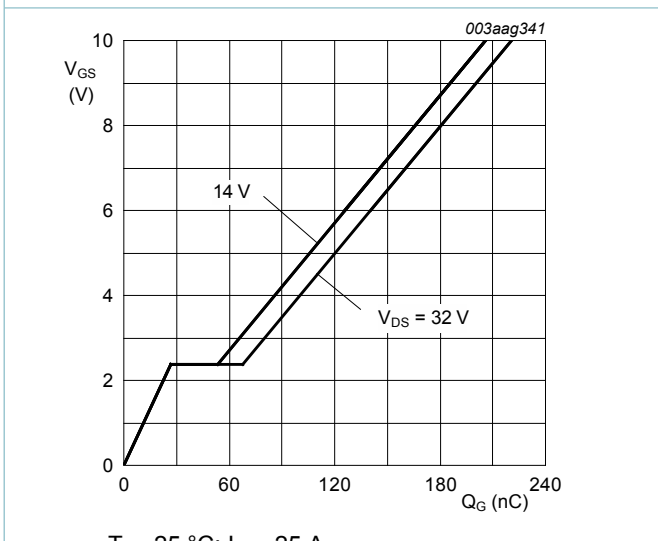
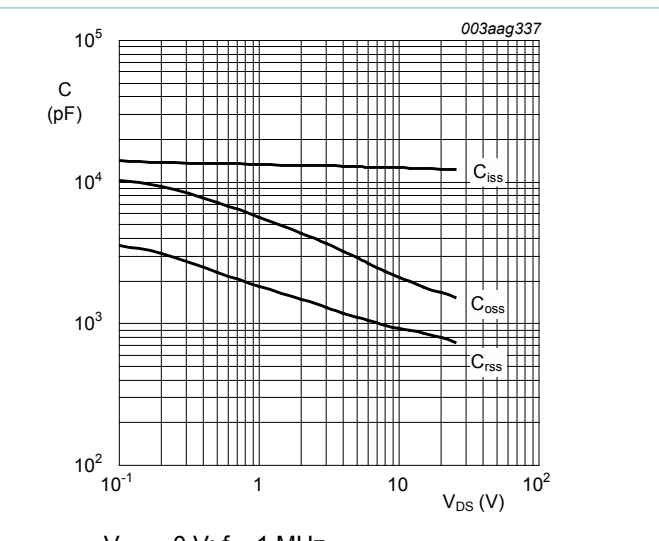


Fig. 13. Gate charge waveform definitions



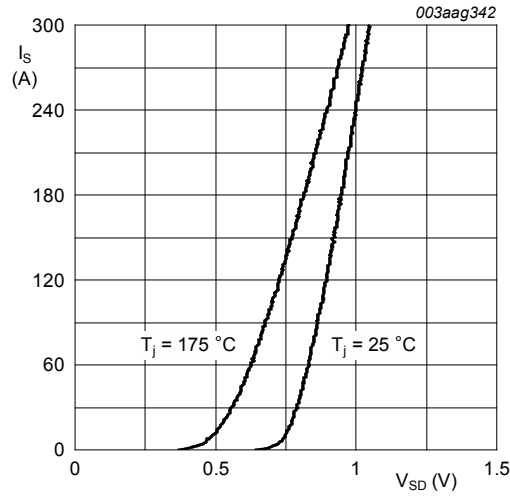
$T_j = 25\text{ }^\circ\text{C}; I_D = 25\text{ A}$

Fig. 14. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0\text{ V}$

Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

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11. Package outline

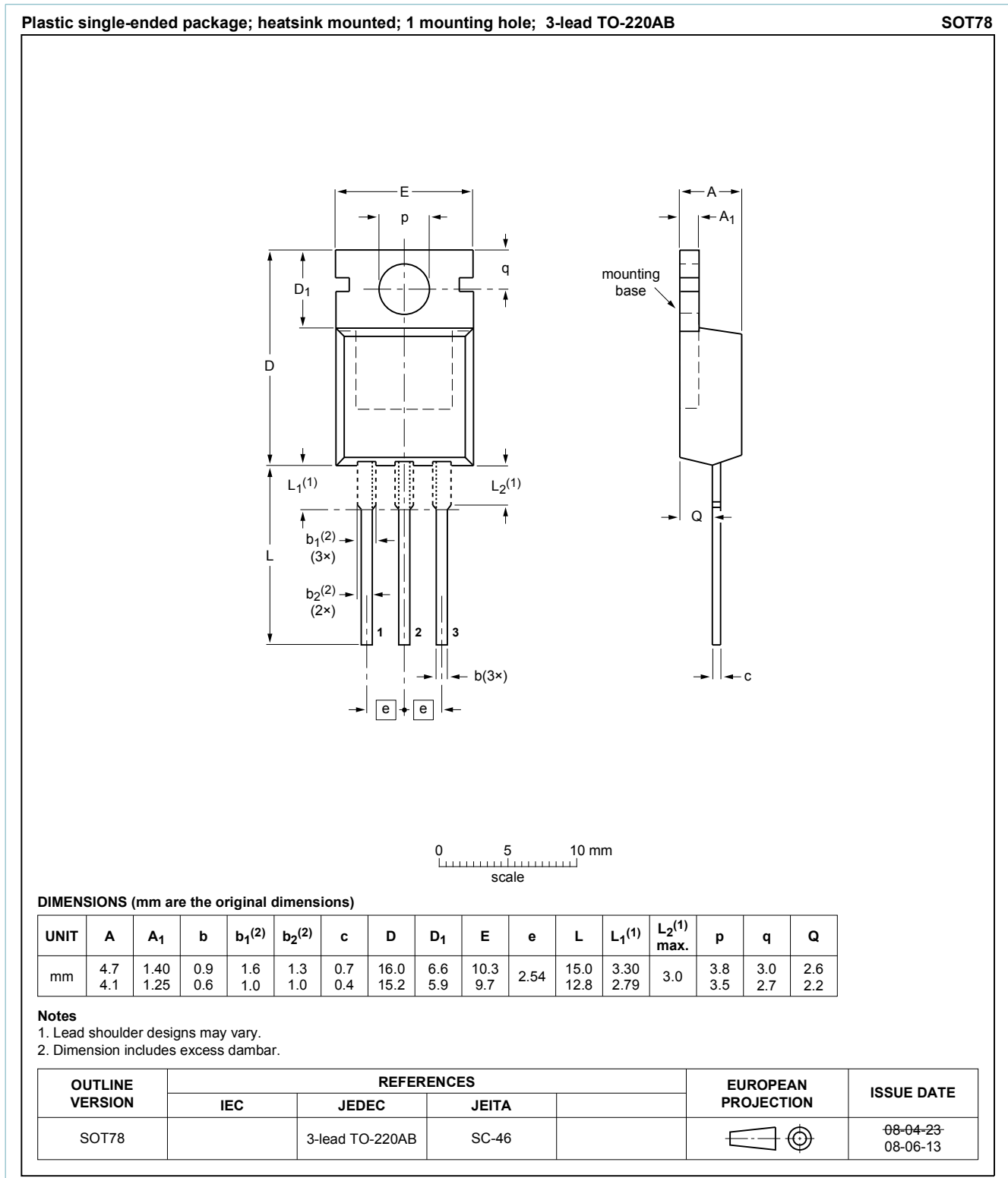


Fig. 17. Package outline TO-220AB (SOT78)

12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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 [2] The term 'short data sheet' is explained in section "Definitions".
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