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DMN2501UFB4

N-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

$V_{(BR)DSS}$	$R_{DS(on)}$ max	I_D $T_A = +25^\circ\text{C}$
20V	0.4Ω @ $V_{GS} = 4.5\text{V}$	1.5A
	0.5Ω @ $V_{GS} = 2.5\text{V}$	1.3A
	0.7Ω @ $V_{GS} = 1.8\text{V}$	1.1A

Description and Applications

This new generation MOSFET is designed to minimize the on-state resistance ($R_{DS(on)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- DC-DC Converters
- Power Management Functions

Features and Benefits

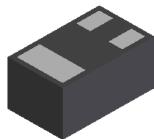
- Low On-Resistance
- Very Low Gate Threshold Voltage $V_{GS(\text{TH})}$, 1.0V Max.
- Low Input Capacitance
- Fast Switching Speed
- Ultra-Small Surfaced Mount Package
- Ultra-Low Package Profile, 0.4mm Maximum Package Height
- ESD Protected Gate
- Totally Lead-Free & Fully RoHS compliant (Notes 1 & 2)**
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability

Mechanical Data

- Case: X2-DFN1006-3
- Case Material: Molded Plastic, "Green" Molding Compound; UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish – NiPdAu over Copper Leadframe; Solderable per MIL-STD-202, Method 208^④
- Weight: 0.001 grams (Approximate)



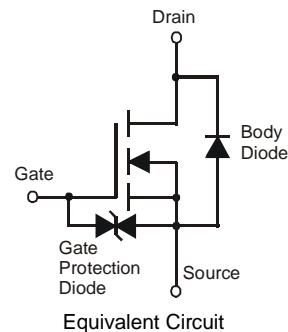
X2-DFN1006-3



Bottom View



Top View
Internal Schematic



Equivalent Circuit

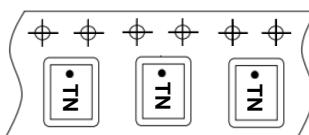
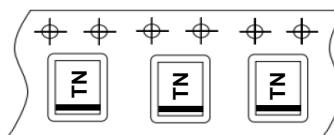
Ordering Information (Note 4)

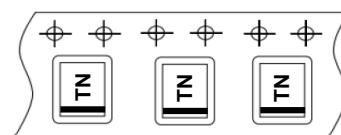
Part Number	Case	Packaging
DMN2501UFB4-7	X2-DFN1006-3	3,000/Tape & Reel
DMN2501UFB4-7B	X2-DFN1006-3	10,000/Tape & Reel

Notes:

- No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen and Antimony free, "Green" and Lead-Free.
- Halogen and Antimony free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- For packaging details, go to our website at <http://www.diodes.com>.

Marking Information

DMN2501UFB4-7	 Top View Dot Denotes Drain Side	From date code 1527 (YYWW), this changes to:	 Top View Bar Denotes Gate and Source Side
			

DMN2501UFB4-7B	 Top View Bar Denotes Gate and Source Side	TN = Part Marking Code
		

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Drain-Source Voltage	V_{DSS}	20	V
Gate-Source Voltage	V_{GSS}	± 8	V
Continuous Drain Current (Note 5) $V_{GS} = 4.5\text{V}$	Steady State	$I_D = 25^\circ\text{C}$ $I_D = 70^\circ\text{C}$	I_D
	$t < 10\text{s}$	$I_D = 25^\circ\text{C}$ $I_D = 70^\circ\text{C}$	I_D
Continuous Drain Current (Note 6) $V_{GS} = 4.5\text{V}$	Steady State	$I_D = 25^\circ\text{C}$ $I_D = 70^\circ\text{C}$	I_D
	$t < 10\text{s}$	$I_D = 25^\circ\text{C}$ $I_D = 70^\circ\text{C}$	I_D
Pulsed Drain Current (10 μs pulse, duty cycle = 1%)	I_{DM}	6	A
Maximum Body Diode continuous Current	I_S	1	A

Thermal Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 5)	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	P_D	0.5
			0.3
Thermal Resistance, Junction to Ambient (Note 5)	Steady State $t < 10\text{s}$	$R_{\theta JA}$	251
			188
Total Power Dissipation (Note 6)	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	P_D	1.2
			0.7
Thermal Resistance, Junction to Ambient (Note 6)	Steady State $t < 10\text{s}$	$R_{\theta JA}$	110
			82
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.

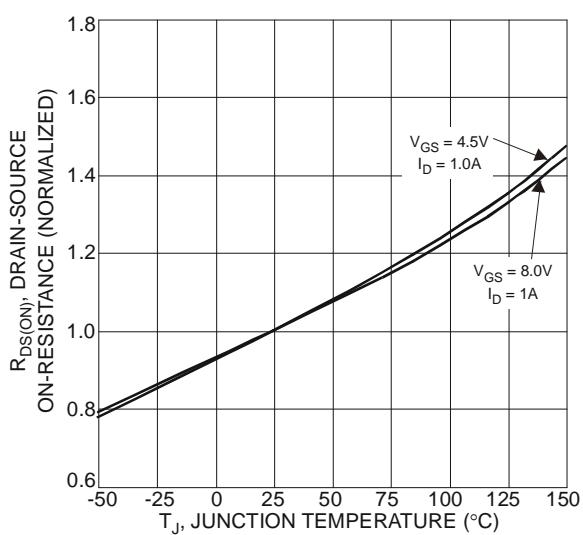
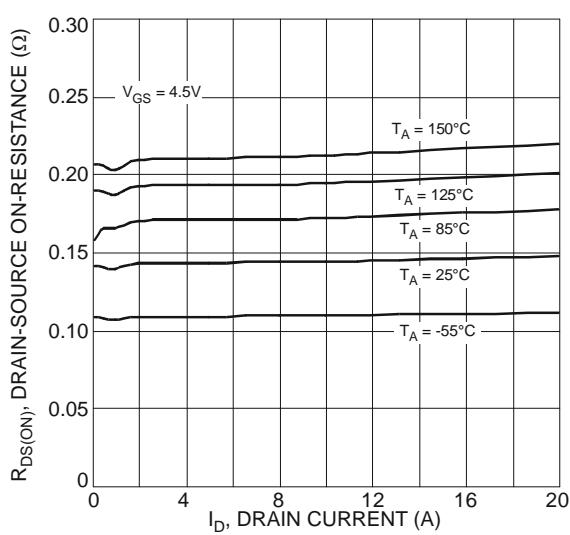
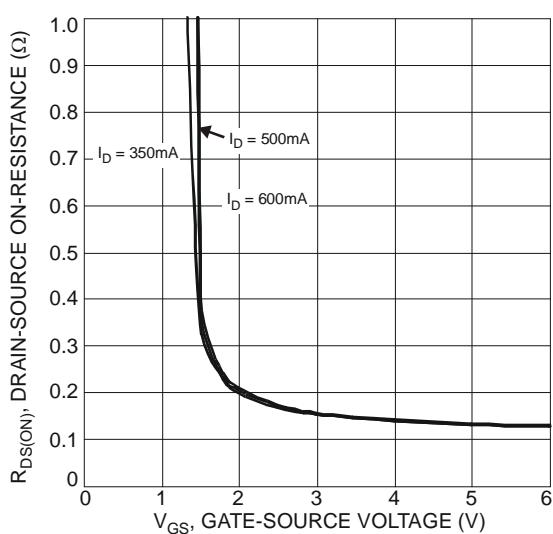
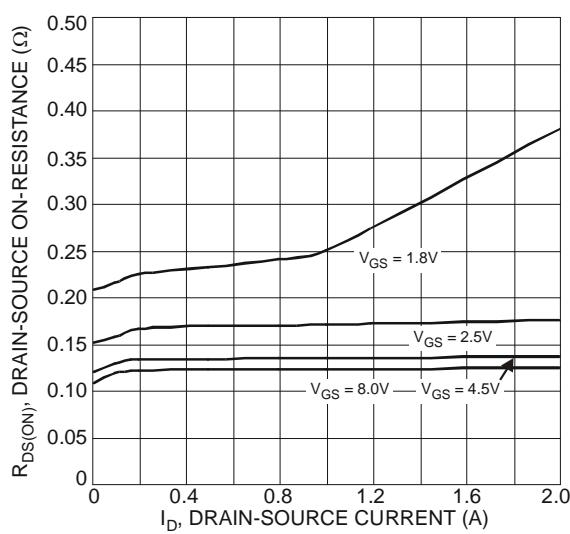
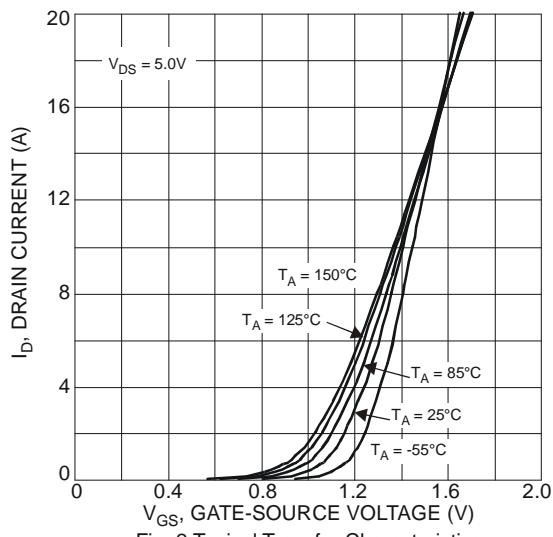
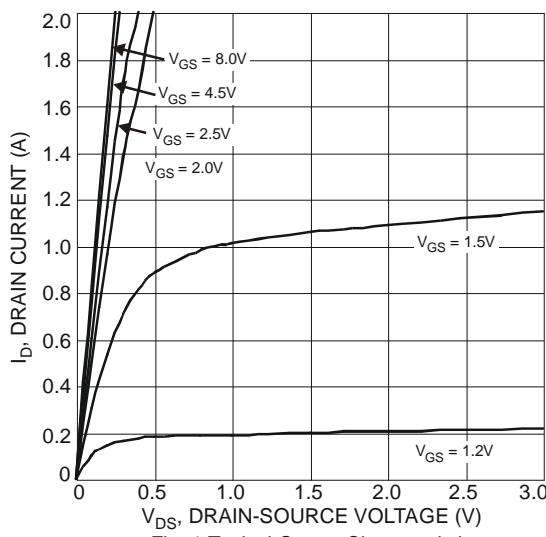
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1-inch square copper plate.

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	20	-	-	V	$\text{V}_{\text{GS}} = 0\text{V}$, $\text{I}_D = 250\mu\text{A}$
Zero Gate Voltage Drain Current $\text{T}_J = +25^\circ\text{C}$	I_{DSS}	-	-	100	nA	$\text{V}_{\text{DS}} = 20\text{V}$, $\text{V}_{\text{GS}} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	-	-	± 1	μA	$\text{V}_{\text{GS}} = \pm 6\text{V}$, $\text{V}_{\text{DS}} = 0\text{V}$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$\text{V}_{\text{GS(th)}}$	0.5	0.76	1.0	V	$\text{V}_{\text{DS}} = \text{V}_{\text{GS}}$, $\text{I}_D = 250\mu\text{A}$
Static Drain-Source On-Resistance	$\text{R}_{\text{DS (ON)}}$	-	170	400	$\text{m}\Omega$	$\text{V}_{\text{GS}} = 4.5\text{V}$, $\text{I}_D = 600\text{mA}$
			200	500		$\text{V}_{\text{GS}} = 2.5\text{V}$, $\text{I}_D = 500\text{mA}$
			260	700		$\text{V}_{\text{GS}} = 1.8\text{V}$, $\text{I}_D = 350\text{mA}$
Forward Transfer Admittance	$ \text{Y}_{\text{fs}} $	-	1.4	-	S	$\text{V}_{\text{DS}} = 10\text{V}$, $\text{I}_D = 400\text{mA}$
Diode Forward Voltage	V_{SD}		0.7	1.2	V	$\text{V}_{\text{GS}} = 0\text{V}$, $\text{I}_S = 150\text{mA}$
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	-	82	-	pF	$\text{V}_{\text{DS}} = 16\text{V}$, $\text{V}_{\text{GS}} = 0\text{V}$, $f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	-	12	-	pF	
Reverse Transfer Capacitance	C_{rss}	-	10	-	pF	
Gate resistance	R_g	-	83	-	Ω	$\text{V}_{\text{DS}} = 0\text{V}$, $\text{V}_{\text{GS}} = 0\text{V}$, $f = 1.0\text{MHz}$
Total Gate Charge ($\text{V}_{\text{GS}} = 4.5\text{V}$)	Q_g	-	1.1	-	nC	$\text{V}_{\text{DS}} = 10\text{V}$, $\text{I}_D = 250\text{mA}$
Total Gate Charge ($\text{V}_{\text{GS}} = 10\text{V}$)	Q_g	-	2.0	-	nC	
Gate-Source Charge	Q_{gs}	-	0.14	-	nC	
Gate-Drain Charge	Q_{gd}	-	0.19	-	nC	$\text{V}_{\text{DD}} = 10\text{V}$, $\text{V}_{\text{GS}} = 4.5\text{V}$, $\text{R}_L = 47\Omega$, $\text{R}_G = 10\Omega$, $\text{I}_D = 200\text{mA}$
Turn-On Delay Time	$\text{t}_{\text{D(on)}}$	-	6.6	-	ns	
Turn-On Rise Time	t_r	-	6.4	-	ns	
Turn-Off Delay Time	$\text{t}_{\text{D(off)}}$	-	40.4	-	ns	
Turn-Off Fall Time	t_f	-	17.3	-	ns	

Notes: 7. Short duration pulse test used to minimize self-heating effect.

8. Guaranteed by design. Not subject to product testing.



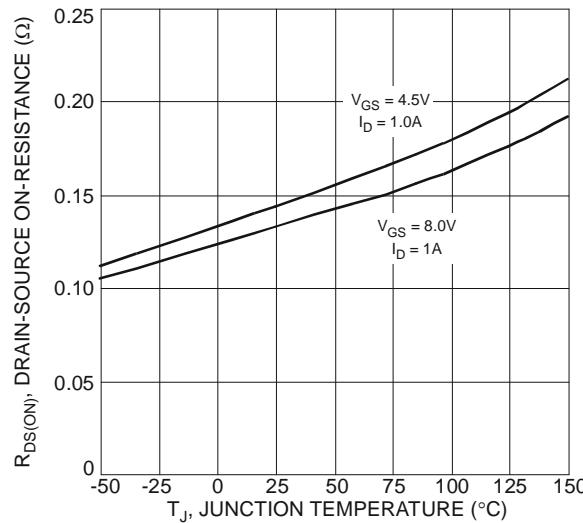


Fig. 7 On-Resistance Variation with Temperature

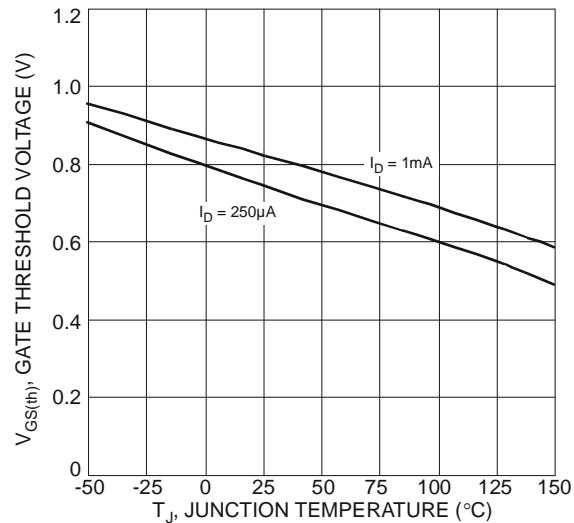


Fig. 8 Gate Threshold Variation vs. Ambient Temperature

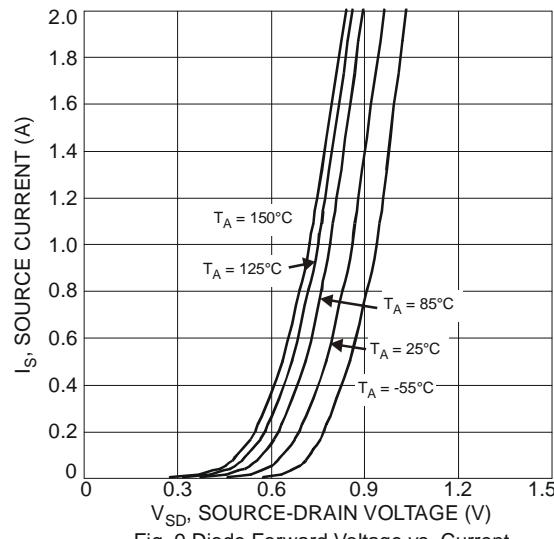


Fig. 9 Diode Forward Voltage vs. Current

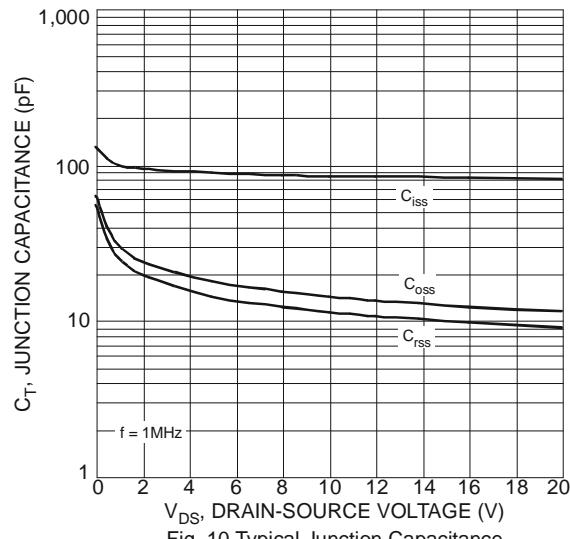


Fig. 10 Typical Junction Capacitance

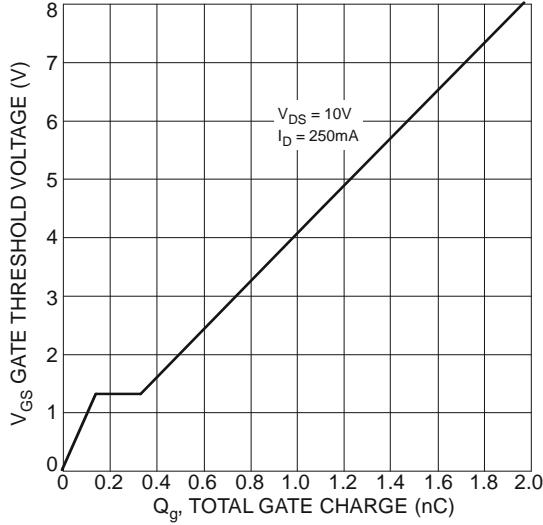


Fig. 11 Gate Charge

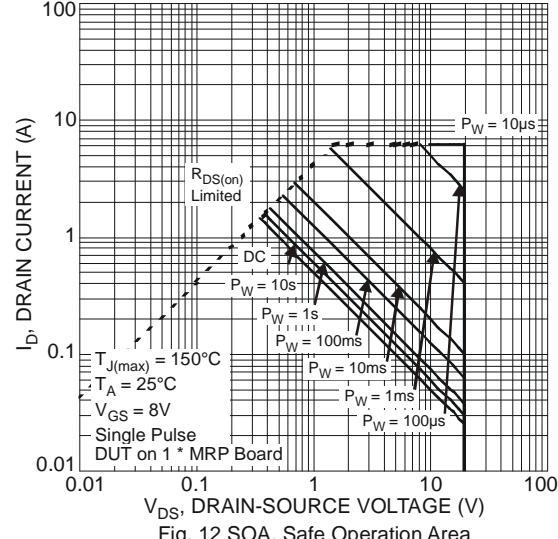
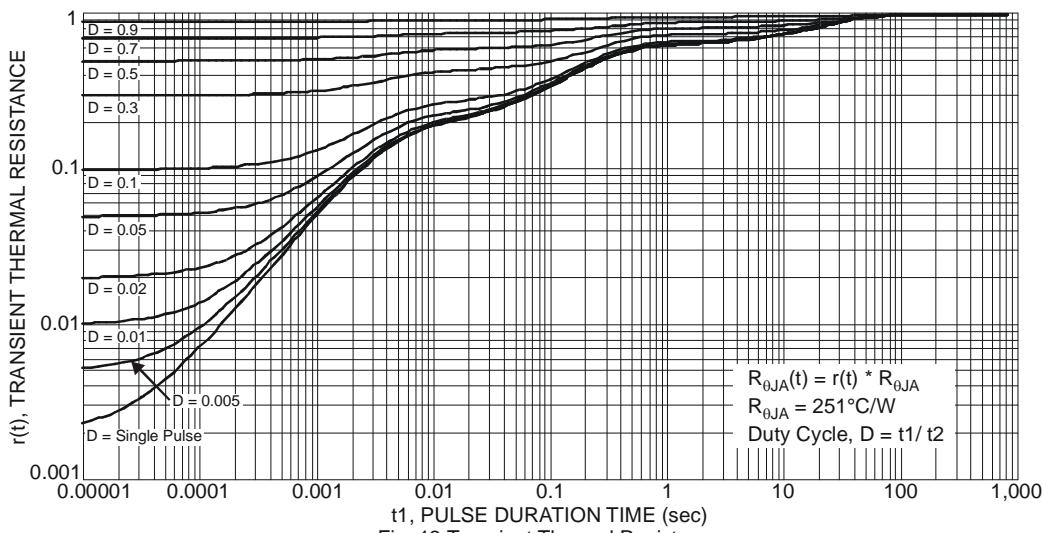
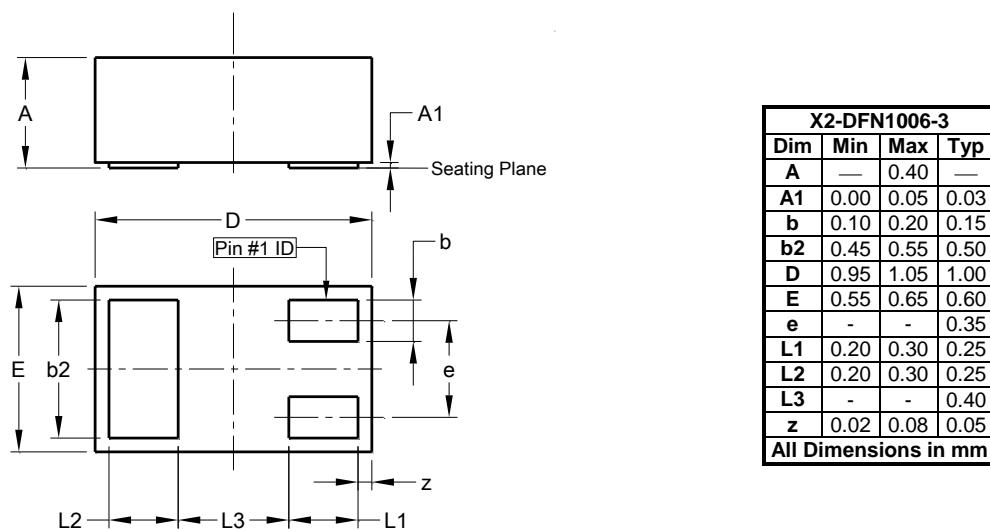


Fig. 12 SOA, Safe Operation Area



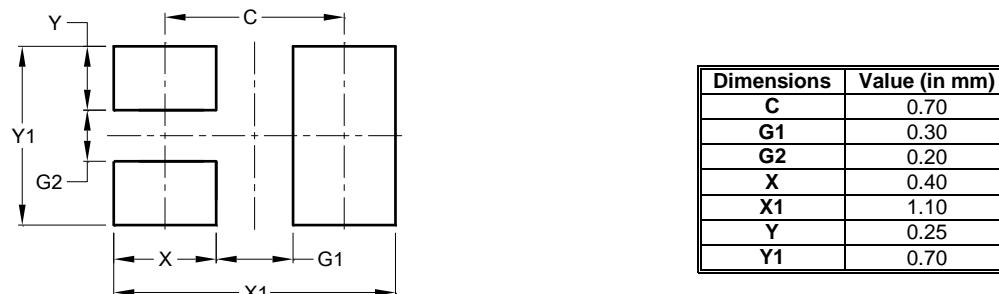
Package Outline Dimensions

Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.



Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



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