

Excellent Integrated System Limited

Stocking Distributor

Click to view price, real time Inventory, Delivery & Lifecycle Information:

[Diodes Incorporated](#)
[ZABG4002JA16TC](#)

For any questions, you can email us directly:

sales@integrated-circuit.com



A Product Line of
Diodes Incorporated



ZABG4002 LOW POWER 4 STAGE FET LNA BIAS CONTROLLER

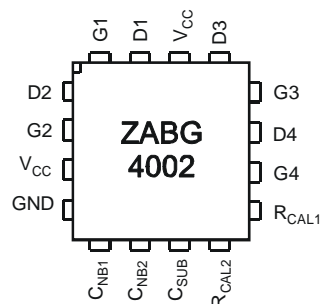
Summary

The ZABG4002 is a four stage depletion mode FET bias controller intended primarily for satellite Low Noise Block's (LNB's), but its also suitable for other LNA applications such as those in found in PMR's and microwave links. The ZABG4002 provides each FET with an independent protected negative gate voltage and positive drain voltage with user programmable drain current. Combining an advanced IC process and packaging techniques, the ZABG4002 helps minimise power consumption, component cost and PCB area whilst enhancing overall reliability.

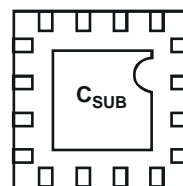
Features

- Four stage FET bias controller
- Operating range of 3.0V to 8.0V
- Low quiescent supply current, 1.2mA typical
- FET drain voltages set at 2.0V
- FET drain current selectable from 0 to 15mA
- Switchable FETs for power management
- Allows first and second stage FETs to be run at different (optimum) drain currents
- FET drain voltages and currents held stable over temperature and Vcc variations
- FETs protected against overstress during power-up and power-down.
- Internal negative supply generator allowing single supply operation (available for external use)
- Low external component count

Pin Assignments



Top View

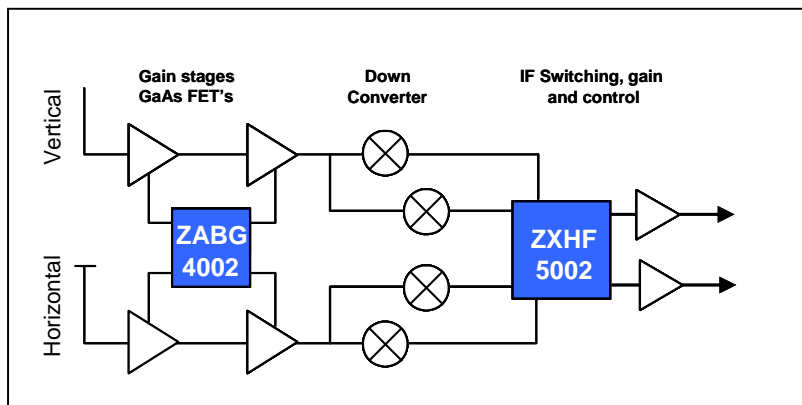


Bottom View

Applications

- Twin LNB's
- Quad LNB's
- US LNB's
- Microwave links
- PMR and Cellular telephone systems

Single Universal LNB System Diagram





A Product Line of
Diodes Incorporated



ZABG4002

Device Description

The ZABG series of devices are designed to meet the bias requirements of GaAs and HEMT FETs commonly used in satellite receiver LNBs with a minimum of external components whilst operating from a minimal voltage supply and using minimal current.

The ZABG4002 provides four FET bias stages, arranged in two pairs of two. Resistors connected to pins Rcal1 and Rcal2 set the FET drain currents of each pair over the range of 0 to 15mA, allowing input FETs to be biased for optimum noise and amplifier FETs for optimum gain.

Drain voltages of all stages are set at 2.0V. The drain supplies are current limited to approximately 5% above the operating currents set by the Rcal resistors.

As an additional feature the Rcal pins can also be used as logic inputs to disable pairs of FETs as part of a power management scheme or simply an alternative to LNA switching. Driven to a logic high (>3.0V), the inputs disable their associated FET bias stages by switching gate feeds to -2.5V and drain feeds open circuit.

Depletion mode FETs require a negative voltage bias supply when operated in grounded source circuits. The ZABG4002 includes an integrated low noise switched capacitor DC-DC converter generating a regulated output of -2.5V to allow single supply operation.

To facilitate the design of efficient low voltage 3.3V LNB systems and to maintain compatibility with higher voltage legacy designs, the ZABG4002 is capable of operating within the supply of 3.0V to 8V.

These devices are unconditionally stable over the full working temperature with the FETs in place, subject to the inclusion of the recommended gate and drain capacitors. These ensure RF stability and minimal injected noise.

It is possible to use less than the devices full complement of FET bias controls, unused drain and gate connections can be left open circuit without affecting operation of the remaining bias circuits.

To protect the external FETs the circuits have been designed to ensure that, under any conditions including power up/down transients, the gate drive from the bias circuits cannot exceed -3V. Additionally each stage has its own individual current limiter. Furthermore if the negative rail experiences a fault condition, such as overload or short circuit, the drain supply to the FETs will shut down avoiding excessive current flow.

To minimise PCB space ZABG4002 is packaged in the 16 pin 3mm x 3mm QFN package.

Device operating temperature is -40°C to 85°C to suit a wide range of environmental conditions.

Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.6 to +10	V
Supply Current	80	mA
Power Dissipation	500	mW
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-40 to +150	°C

Electrical Characteristics (Measured at T_{AMB} = 25°C, V_{CC} = 3.3V (note 1), R_{CAL1} = R_{CAL2} = 39k (setting I_D to 10mA) unless otherwise stated)

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Operating Voltage Range (note 1)		V _{CC}	3.0		8.0	V
Supply Current	I _{D1} = I _{D2} = I _{D3} = I _{D4} = 0	I _{CC}		1.2	4.0	mA
	I _{D1} = I _{D2} = I _{D3} = I _{D4} = 10mA	I _{CC(L)}		42	44	mA
Substrate Voltage	I _{CSUB} = 0	V _{CSUB}	-3.0	-2.65	-2.0	V
	I _{CSUB} = -200uA	V _{CSUB(L)}		-2.55	-2.0	V
Oscillator Frequency		F _{OSC}	150	240	600	kHz

Gate Characteristics

Gate (G1 to G4)

Current Range		I _G	-100		+500	uA
Voltage Low	I _D = 12mA, I _G = -10uA	V _{G(L)}	-3.0	-2.5	-2.0	V
Voltage High	I _D = 8mA, I _G = 0	V _{G(H)}	0	0.7	1.0	V
Voltage Disabled	I _D = 0, I _G = -10uA, V _{RCAL} = 3.0V	V _{G(DIS)}	-3.0	-2.5	-2.0	V

Drain Characteristics

Drain (D1 to D4)

Current Range		I _D	0		15	mA
Current Operating	Standard Application Circuit	I _{D(OP)}	8	10	12	mA
Current Disabled	V _D = 0, V _{RCAL} = 3.0V	I _{D(DIS)}			10	uA
Voltage Operating	I _D = 10mA	V _{D(OP)}	1.8	2.0	2.2	V
delta I _D vs V _{CC}	V _{CC} = 3.3 to 8.0V	dI _D /dV _{CC}		1.2		%/V
delta I _D vs T _{OP}	T _{OP} = -40°C to +85°C	dI _D /dT _{OP}		0.05		%/°C
delta V _D vs V _{CC}	V _{CC} = 3.3 to 8.0V	dV _D /dV _{CC}		0.05		%/V
delta V _D vs T _{OP}	T _{OP} = -40°C to +85°C	dV _D /dT _{OP}		50		ppm/°C

R_{CAL}(1 and 2)

Disable Threshold		V _{RCAL(DIS)}	1.8	2.7	3.0	V
Input Current	V _{RCAL} = 3.0V	I _{RCAL(DIS)}		1.7	10	uA

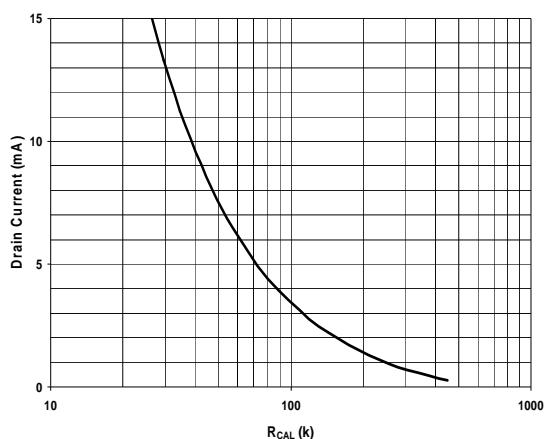
Output Noise

Drain Voltage	C _{GATE-GND} = 10nF, C _{DRAIN-GND} = 10nF	V _{D(Noise)}			0.02	Vpk-pk
Gate Voltage	C _{GATE-GND} = 10nF, C _{DRAIN-GND} = 10nF	V _{G(Noise)}			0.005	Vpk-pk

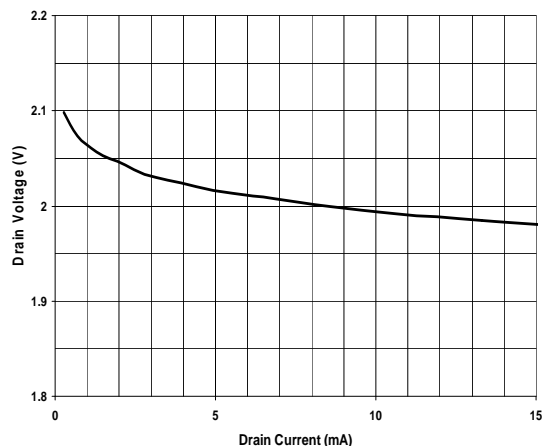
- Notes:
1. The two V_{CC} pins are internally connected, only one of the pins needs to be powered for the device to function. See applications section for further information.
 2. ESD sensitive, handling precautions are recommended.
 3. The negative bias voltages are generated on-chip using an internal oscillator. Two external capacitors, C_{NB} and C_{SUB} of value 47nF are required for this purpose.
 4. The package (QFN1633) exposed pad must either be connected to C_{SUB} or left open circuit.
 5. The characteristics are measured using two external reference resistors R_{CAL1} and R_{CAL2} of value 39k, wired from pins R_{CAL1/2} to ground. Resistor R_{CAL1} sets the drain current of FETs 1 and 3, resistor R_{CAL2} sets the drain currents of FETs 2 and 4.
 6. Noise voltage measurements are made with FETs and gate and drain capacitors of value 10nF in place. Noise voltages are not measured in production.

Typical Characteristics (Measured at $T_{AMB} = 25^{\circ}\text{C}$, $V_{CC} = 3.3\text{V}$, $R_{CAL1} = R_{CAL2} = 39\text{k}$ (setting I_D to 10mA) unless otherwise stated)

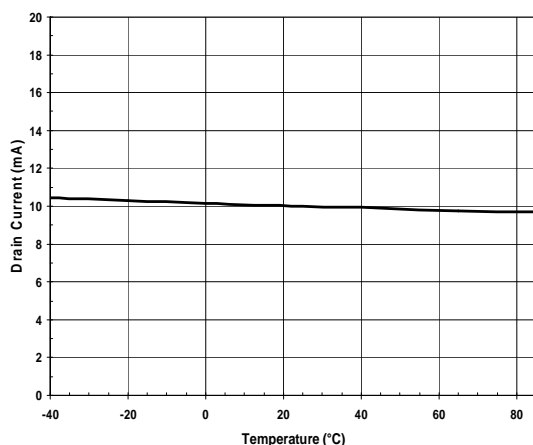
ZABG4002 Drain Current vs R_{CAL}



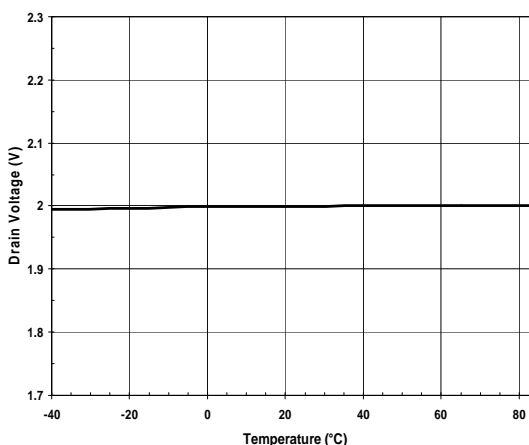
ZABG4002 Drain Voltage vs Drain Current



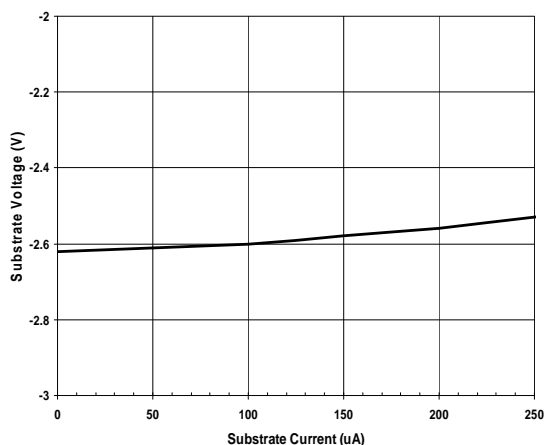
ZABG4002 Drain Current vs Temperature



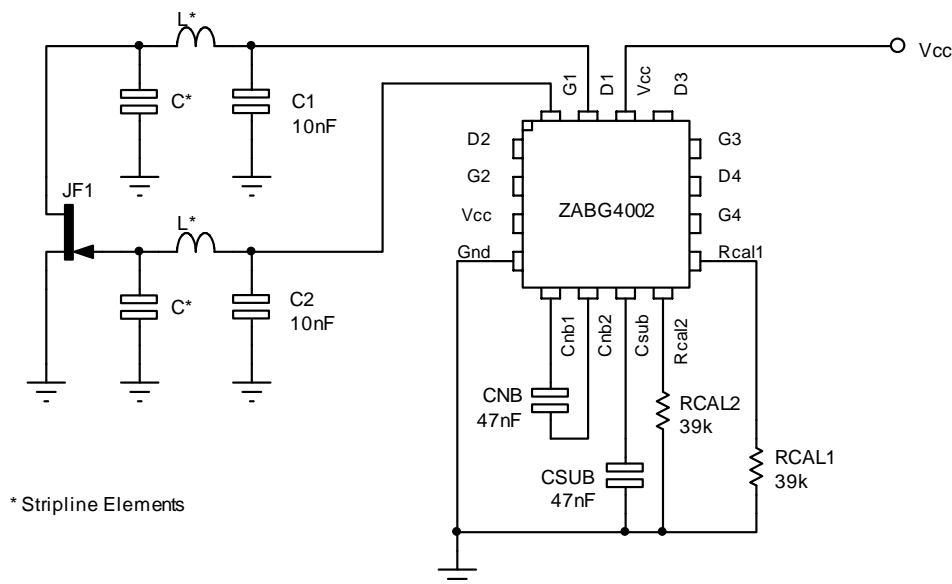
ZABG4002 Drain Voltage vs Temperature



ZABG4002 Substrate Voltage vs Substrate Current



Applications Circuit



Applications Information

Above is a partial applications circuit for the ZABG4002 showing all external components needed for biasing one of the four FET stages available. Each bias stage is provided with a gate and drain pin. The drain pin provides a regulated 2.0V supply that includes a drain current monitor. The drain current taken by the external FET is compared with a user selected level, generating a signal that adjusts the gate voltage of the FET to obtain the required drain current. If for any reason, an attempt is made to draw more than the user set drain current from the drain pin, the drain voltage will be reduced to ensure excess current is not taken. The gate pin drivers are also current limited.

The bias stages are split up into two pairs, with the drain current of each pair set by an external R_{CAL} resistor. R_{CAL1} sets the drain currents of stages 1 and 3, whilst R_{CAL2} sets the drain currents of stages 2 and 4. This allows the optimisation of drain currents for differing tasks such as input stages where noise can be critical and later amplifier stages where gain may be more important. A graph showing the relationship between the value of R_{CAL} and I_D is provided in the Typical Characteristics section of this datasheet. The R_{CAL} pins can also be used as logic inputs. If set to a logic high state ($>3.0V$), the associated FET bias stages are disabled, driving gate pins to $-2.5V$ and switching drain pins open-circuit. This feature can be used as part of a power management system that turns off any unwanted stages in a multi input receiver.

The ZABG4002 includes a switched capacitor DC-DC converter that is used to generate the negative supply required to bias depletion mode FETs used in common source circuit configuration as shown above. This converter uses two external capacitors, C_{NB} the charge transfer capacitor and C_{SUB} the output reservoir capacitor. The circuit provides a regulated $-2.5V$ supply both for gate driver use and for external use if required (for extra discrete bias stages, mixer bias, local oscillator bias etc.). The $-2.5V$ supply is available from the C_{SUB} pin.

If any bias stages are not required, their gate and drain pins may be left open circuit. If all bias stages associated with an R_{CAL} resistor are not required, then this resistor may be omitted.

To ease PCB layout, the pinout for the ZABG4002 includes two V_{CC} pins. These pins are internally connected so only one of the pins needs to be powered for the device to function. It is probable that the extra pin will help avoid the need for trace cross-over components or ground plane disruption from reverse side PCB links. Note that the exposed pad of the package must be either left floating or connected to C_{sub} .

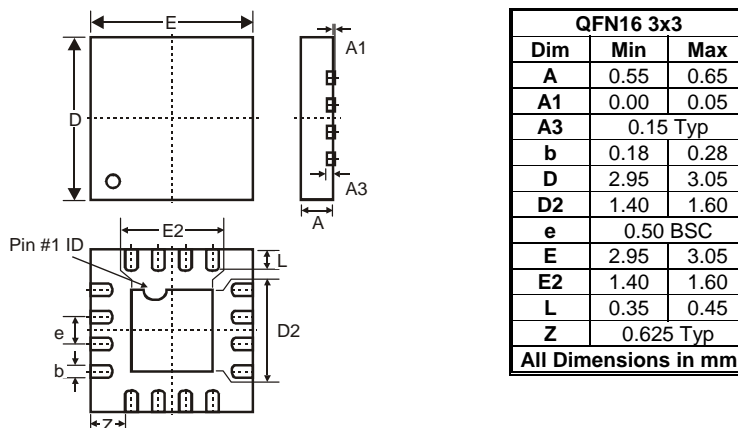


A Product Line of
Diodes Incorporated



ZABG4002

Package Outline Dimensions



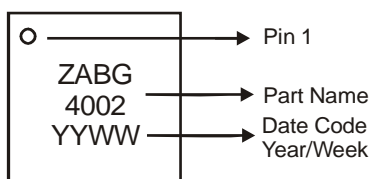
Note: Controlling dimensions are in millimetres. Approximate dimensions are provided in inches.

The package appearance may vary as shown, for further details please contact your local Diodes sales office.

Ordering Information (Note x)

Device	Package	Reel Size (inches)	Tape Width (mm)	Quantity (per reel)
ZABG4002JA16TC	QFN1633	13	8	3000

Marking Information





A Product Line of
Diodes Incorporated



ZABG4002

NEW PRODUCT

IMPORTANT NOTICE

DIODES INCORPORATED MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

Diodes Incorporated and its subsidiaries reserve the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. Diodes Incorporated does not assume any liability arising out of the application or use of this document or any product described herein; neither does Diodes Incorporated convey any license under its patent or trademark rights, nor the rights of others. Any Customer or user of this document or products described herein in such applications shall assume all risks of such use and will agree to hold Diodes Incorporated and all the companies whose products are represented on Diodes Incorporated website, harmless against all damages.

Diodes Incorporated does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel. Should Customers purchase or use Diodes Incorporated products for any unintended or unauthorized application, Customers shall indemnify and hold Diodes Incorporated and its representatives harmless against all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized application.

Products described herein may be covered by one or more United States, international or foreign patents pending. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks.

LIFE SUPPORT

Diodes Incorporated products are specifically not authorized for use as critical components in life support devices or systems without the express written approval of the Chief Executive Officer of Diodes Incorporated. As used herein:

A. Life support devices or systems are devices or systems which:

1. are intended to implant into the body, or
2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

Customers represent that they have all necessary expertise in the safety and regulatory ramifications of their life support devices or systems, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of Diodes Incorporated products in such safety-critical, life support devices or systems, notwithstanding any devices- or systems-related information or support that may be provided by Diodes Incorporated. Further, Customers must fully indemnify Diodes Incorporated and its representatives against any damages arising out of the use of Diodes Incorporated products in such safety-critical, life support devices or systems.

Copyright © 2010, Diodes Incorporated

www.diodes.com