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## Low-Jitter, Precision Clock Generator with Three Outputs

### General Description

The MAX3625B is a low-jitter, precision clock generator optimized for networking applications. The device integrates a crystal oscillator and a phase-locked loop (PLL) clock multiplier to generate high-frequency clock outputs for Ethernet, 10G Fibre Channel, and other networking applications.

This proprietary PLL design features ultra-low jitter and excellent power-supply noise rejection, minimizing design risk for network equipment.

The MAX3625B has three LVPECL outputs. Selectable output dividers and a selectable feedback divider allow a range of output frequencies.

### Applications

Ethernet Networking Equipment  
Fibre Channel Storage Area Network

*Typical Application Circuit appears at end of data sheet.*

### Features

- ◆ Crystal Oscillator Interface: 24.8MHz to 27MHz
- ◆ CMOS Input: Up to 320MHz
- ◆ Output Frequencies
  - Ethernet: 62.5MHz, 125MHz, 156.25MHz, 312.5MHz
  - 10G Fibre Channel: 159.375MHz, 318.75MHz
- ◆ Low Jitter
  - 0.14psRMS (1.875MHz to 20MHz)
  - 0.36psRMS (12kHz to 20MHz)
- ◆ Excellent Power-Supply Noise Rejection
- ◆ No External Loop Filter Capacitor Required

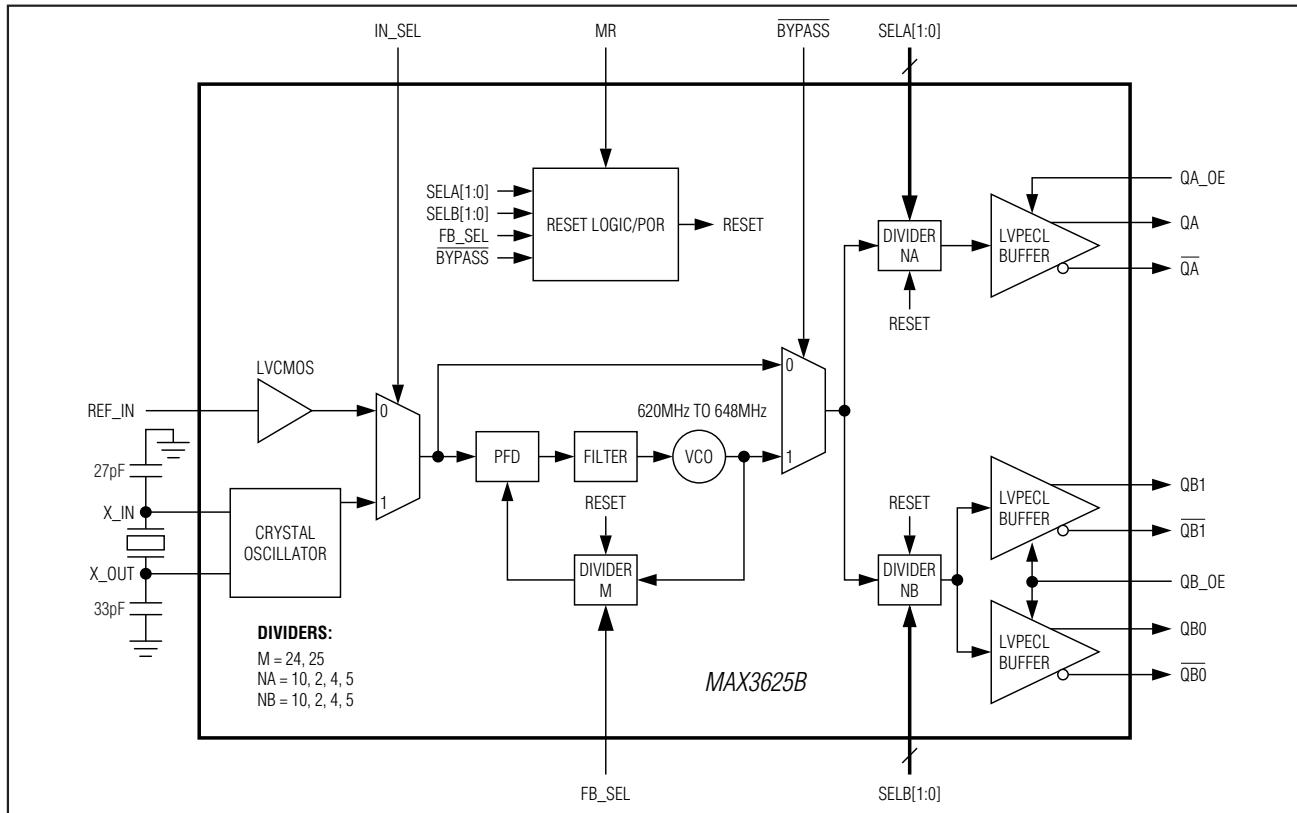
### Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3625BEUG+	-40°C to +85°C	24 TSSOP-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

\*EP = Exposed pad.

### Block Diagram



**MAX3625B**

## Low-Jitter, Precision Clock Generator with Three Outputs

### ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range V <sub>CC</sub> , V <sub>CCA</sub> , V <sub>CCO_A</sub> , V <sub>CCO_B</sub> .....	-0.3V to +4.0V
Voltage Range at REF_IN, IN_SEL, FB_SEL, SELA[1:0], SELB[1:0], QA_OE, QB_OE, MR, BYPASS .....	-0.3V to (V <sub>CC</sub> + 0.3V)
Voltage Range at X_IN .....	-0.3V to +1.2V

Voltage Range at X_OUT .....	-0.3V to (V <sub>CC</sub> - 0.6V)
Current into QA, $\overline{QA}$ , QB0, $\overline{QB0}$ , QB1, $\overline{QB1}$ .....	-56mA
Continuous Power Dissipation (T <sub>A</sub> = +70°C)	
24-Pin TSSOP (derate 26.7mW/°C above +70°C)	..2133.3mW
Operating Junction Temperature Range .....	-55°C to +150°C
Storage Temperature Range .....	-65°C to +160°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = +3.0V to +3.6V, T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at V<sub>CC</sub> = +3.3V, T<sub>A</sub> = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Current (Note 3)	I <sub>CC</sub>	IN_SEL = high	72	98		mA
		IN_SEL = low	74			
<b>CONTROL INPUT CHARACTERISTICS</b> <b>(SELA[1:0], SELB[1:0], FB_SEL, IN_SEL, QA_OE, QB_OE, MR, BYPASS Pins)</b>						
Input Capacitance	C <sub>IN</sub>		2			pF
Input Pulldown Resistor	R <sub>PULLDOWN</sub>	Pins MR, FB_SEL	75			kΩ
Input Logic Bias Resistor	R <sub>BIAS</sub>	Pins SELA[1:0], SELB[1:0]	50			kΩ
Input Pullup Resistor	R <sub>PULLUP</sub>	Pins QA_OE, QB_OE, IN_SEL, BYPASS	75			kΩ
<b>LVPECL OUTPUTS (QA, <math>\overline{QA}</math>, QB0, <math>\overline{QB0}</math>, QB1, <math>\overline{QB1}</math> Pins)</b>						
Output High Voltage	V <sub>OH</sub>		V <sub>CC</sub> - 1.18	V <sub>CC</sub> - 0.98	V <sub>CC</sub> - 0.83	V
Output Low Voltage	V <sub>OL</sub>		V <sub>CC</sub> - 1.90	V <sub>CC</sub> - 1.7	V <sub>CC</sub> - 1.55	V
Peak-to-Peak Output-Voltage Swing (Single-Ended)		(Note 2)	0.6	0.72	0.9	V <sub>P-P</sub>
Clock Output Rise/Fall Time		20% to 80% (Note 2)	200	350	600	ps
Output Duty-Cycle Distortion		PLL enabled	48	50	52	%
		PLL bypassed (Note 4)	45	50	55	
<b>LVC MOS/LV TTL INPUTS</b> <b>(SELA[1:0], SELB[1:0], FB_SEL, IN_SEL, QA_OE, QB_OE, MR, BYPASS Pins)</b>						
Input-Voltage High	V <sub>IH</sub>		2.0			V
Input-Voltage Low	V <sub>IL</sub>			0.8		V
Input High Current	I <sub>IH</sub>	V <sub>IN</sub> = V <sub>CC</sub>			80	μA
Input Low Current	I <sub>IL</sub>	V <sub>IN</sub> = 0V	-80			μA

## **Low-Jitter, Precision Clock Generator with Three Outputs**

### **ELECTRICAL CHARACTERISTICS (continued)**

( $V_{CC} = +3.0V$  to  $+3.6V$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise noted. Typical values are at  $V_{CC} = +3.3V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>REF_IN SPECIFICATIONS (Input DC- or AC-Coupled)</b>						
Reference Clock Frequency		PLL enabled	24.8	27.0	320	MHz
		PLL bypassed				
Input-Voltage High	$V_{IH}$		2.0			V
Input-Voltage Low	$V_{IL}$			0.8		V
Input High Current	$I_{IH}$	$V_{IN} = V_{CC}$		240		$\mu A$
Input Low Current	$I_{IL}$	$V_{IN} = 0V$	-240			$\mu A$
Reference Clock Duty Cycle		PLL enabled	30	70		%
Input Capacitance				2.5		$pF$
<b>CLOCK OUTPUT AC SPECIFICATIONS</b>						
VCO Frequency Range			620	648		MHz
Random Jitter (Note 5)	RJRMS	12kHz to 20MHz	0.36	1.0	0.14	psRMS
		1.875MHz to 20MHz				
Spurs Induced by Power-Supply Noise		(Notes 6, 7, 8)		-60		dBc
Deterministic Jitter Induced by Power-Supply Noise		(Note 9)		5.6		psP-P
Nonharmonic and Subharmonic Spurs				-70		dBc
Output Skew		Between any output pair		5		ps
Clock Output SSB Phase Noise at 125MHz (Note 10)		$f = 1kHz$		-124	dBc/Hz	
		$f = 10kHz$		-127		
		$f = 100kHz$		-131		
		$f = 1MHz$		-145		
		$f > 10MHz$		-153		

**Note 1:** A series resistor of up to  $10.5\Omega$  is allowed between  $V_{CC}$  and  $V_{CCA}$  for filtering supply noise when system power-supply tolerance is  $V_{CC} = 3.3V \pm 5\%$ . See Figure 1.

**Note 2:** LVPECL outputs guaranteed up to 320MHz.

**Note 3:** All outputs enabled and unloaded.

**Note 4:** Measured with a crystal (see Table 4) or an AC-coupled, 50% duty-cycle signal on REF\_IN.

**Note 5:** Measured with crystal source, see Table 4.

**Note 6:** Measured using setup shown in Figure 1.

**Note 7:** Measured with 40mVp-p, 100kHz sinusoidal signal on the supply.

**Note 8:** Measured at 156.25MHz output.

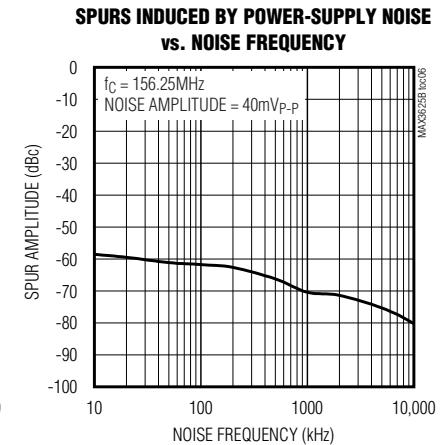
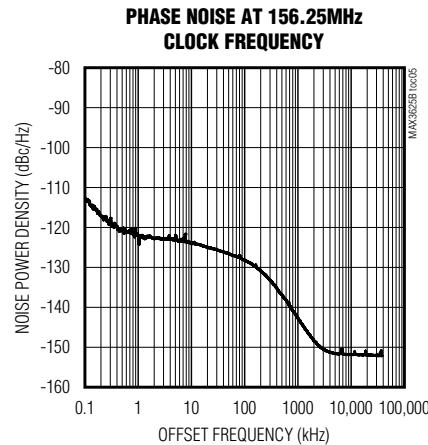
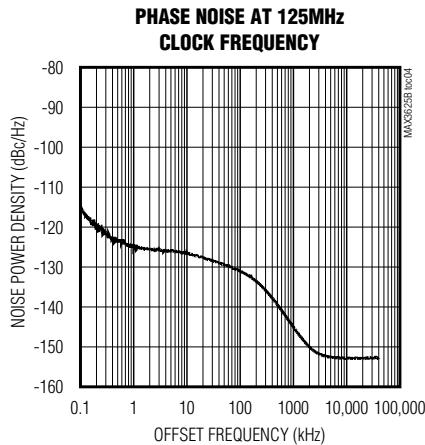
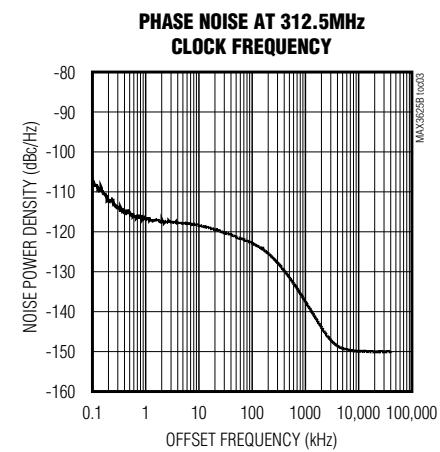
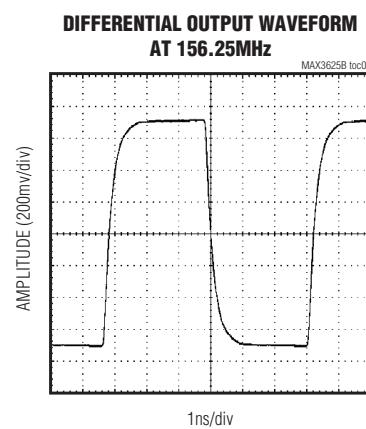
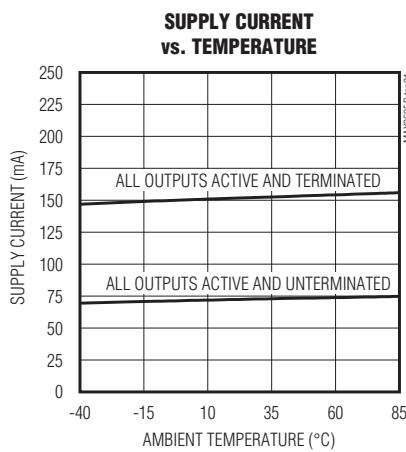
**Note 9:** Calculated based on measured spurs induced by power-supply noise (refer to Application Note 4461: HFAN-04.5.5: *Characterizing Power-Supply Noise Rejection in PLL Clock Synthesizers*).

**Note 10:** Measured with 25MHz crystal or 25MHz reference clock at REF\_IN with a slew rate of 0.5V/ns or greater.

## Low-Jitter, Precision Clock Generator with Three Outputs

### Typical Operating Characteristics

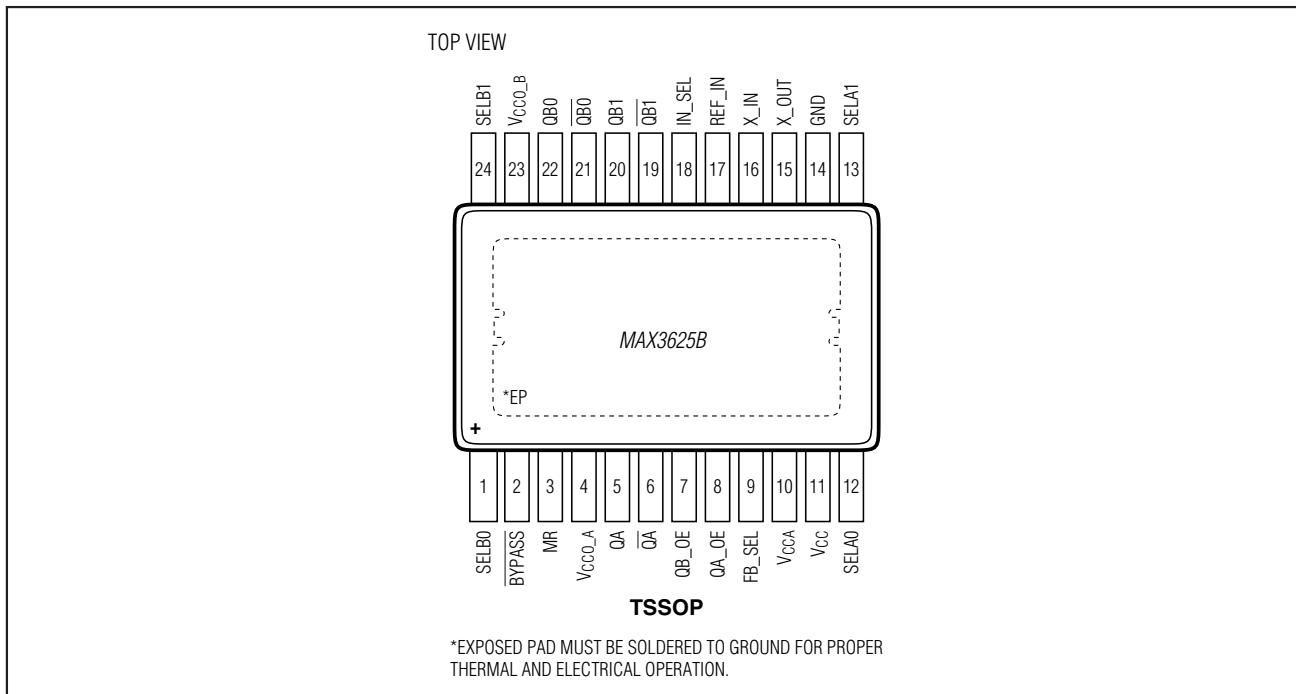
(Typical values are at  $V_{CC} = +3.3V$ ,  $T_A = +25^\circ C$ , crystal frequency = 25MHz.)



## Low-Jitter, Precision Clock Generator with Three Outputs

### Pin Configuration

**MAX3625B**



### Pin Description

PIN	NAME	FUNCTION
1, 24	SELB0, SELB1	LVCMOS/LVTTL Inputs. Control NB divider setting. Has 50kΩ input impedance. See Table 2 for more information.
2	<u>BYPASS</u>	LVCMOS/LVTTL Input (Active Low). Connect low to bypass the internal PLL. Connect high or leave open for normal operation. When in bypass mode the output dividers are set to divide by 1. Has internal 75kΩ pullup to Vcc.
3	MR	LVCMOS/LVTTL Input. Master reset input. Pulse high for > 1µs to reset all dividers. Has internal 75kΩ pulldown to GND. Not required for normal operation.
4	VCCO_A	Power Supply for QA Clock Output. Connect to +3.3V.
5	QA	Noninverting Clock Output, LVPECL
6	<u>QA</u>	Inverting Clock Output, LVPECL
7	QB_OE	LVCMOS/LVTTL Input. Enables/disables QB clock outputs. Connect pin high or leave open to enable LVPECL clock outputs QB0 and QB1. Connect low to set QB0 and QB1 to a logic 0. Has internal 75kΩ pullup to Vcc.
8	QA_OE	LVCMOS/LVTTL Input. Enables/disables the QA clock output. Connect high or leave open to enable the LVPECL clock output QA. Connect low to set QA to a logic 0. Has internal 75kΩ pullup to Vcc.
9	FB_SEL	LVCMOS/LVTTL Input. Controls M divider setting. See Table 3 for more information. Has internal 75kΩ pulldown to GND.

## Low-Jitter, Precision Clock Generator with Three Outputs

### Pin Description (continued)

PIN	NAME	FUNCTION
10	V <sub>CCA</sub>	Analog Power Supply for the VCO. Connect to +3.3V. For additional power-supply noise filtering, this pin can connect to V <sub>CC</sub> through 10.5Ω as shown in Figure 1 (requires V <sub>CC</sub> = 3.3V ±5%).
11	V <sub>CC</sub>	Core Power Supply. Connect to +3.3V.
12, 13	SEL <sub>A0</sub> , SEL <sub>A1</sub>	LVC MOS/LVTTL Inputs. Control NA divider setting. See Table 2 for more information. 50kΩ input impedance.
14	GND	Supply Ground
15	X <sub>OUT</sub>	Crystal Oscillator Output
16	X <sub>IN</sub>	Crystal Oscillator Input
17	REF <sub>_IN</sub>	LVC MOS Reference Clock Input. Self-biased to allow AC- or DC-coupling.
18	IN <sub>_SEL</sub>	LVC MOS/LVTTL Input. Connect high or leave open to use a crystal. Connect low to use REF <sub>_IN</sub> . Has internal 75kΩ pullup to V <sub>CC</sub> .
19	QB1	LVPECL, Inverting Clock Output
20	QB1	LVPECL, Noninverting Clock Output
21	QB0	LVPECL, Inverting Clock Output
22	QB0	LVPECL, Noninverting Clock Output
23	V <sub>CCO_B</sub>	Power Supply for QB0 and QB1 Clock Output. Connect to +3.3V.
—	EP	Exposed Pad. Supply ground; connect to PCB ground for proper electrical and thermal performance.

### Detailed Description

The MAX3625B is a low-jitter clock generator designed to operate at Ethernet and Fibre Channel frequencies. It consists of an on-chip crystal oscillator, PLL, programmable dividers, and LVPECL output buffers. Using a low-frequency clock (crystal or CMOS input) as a reference, the internal PLL generates a high-frequency output clock with excellent jitter performance.

#### Crystal Oscillator

An integrated oscillator provides the low-frequency reference clock for the PLL. This oscillator requires an external crystal connected between X<sub>IN</sub> and X<sub>OUT</sub>. The crystal frequency is 24.8MHz to 27MHz.

#### REF<sub>\_IN</sub> Buffer

An LVC MOS-compatible clock source can be connected to REF<sub>\_IN</sub> to serve as the reference clock.

The LVC MOS REF<sub>\_IN</sub> buffer is internally biased to the threshold voltage (1.4V typ) to allow AC- or DC-coupling, and is designed to operate up to 320MHz.

#### PLL

The PLL takes the signal from the crystal oscillator or reference clock input and synthesizes a low-jitter, high-frequency clock. The PLL contains a phase-frequency detector (PFD), a lowpass filter, and a voltage-

controlled oscillator (VCO) with a 620MHz to 648MHz operating range. The VCO is connected to the PFD input through a feedback divider. See Table 3 for divider values. The PFD compares the reference frequency to the divided-down VCO output (f<sub>VCO</sub>/M) and generates a control signal that keeps the VCO locked to the reference clock. The high-frequency VCO output clock is sent to the output dividers. To minimize noise-induced jitter, the VCO supply (V<sub>CCA</sub>) is isolated from the core logic and output buffer supplies.

#### Output Dividers

The output dividers are programmable to allow a range of output frequencies. See Table 2 for the divider input settings. The output dividers are automatically set to divide by 1 when the MAX3625B is in bypass mode (BYPASS = 0).

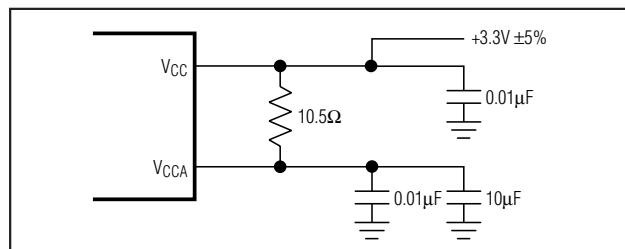


Figure 1. Analog Supply Filtering

# **Low-Jitter, Precision Clock Generator with Three Outputs**

**Table 1. Output Frequency Determination**

CRYSTAL OR CMOS INPUT FREQUENCY (MHz)	FEEDBACK DIVIDER, M	VCO FREQUENCY (MHz)	OUTPUT DIVIDER, NA AND NB	OUTPUT FREQUENCY (MHz)	APPLICATIONS
25	25	625	2	312.5	Ethernet
			4	156.25	
			5	125	
			10	62.5	
25.78125	25	644.53125	4	161.132812	10Gbps Ethernet
26.04166	24	625	2	312.5	Ethernet
			4	156.25	
			5	125	
			10	62.5	
26.5625	24	637.5	2	318.75	10G Fibre Channel
			4	159.375	

### **LVPECL Drivers**

The high-frequency outputs—QA, QB0, and QB1—are differential PECL buffers designed to drive transmission lines terminated with  $50\Omega$  to VCC - 2.0V. The maximum operating frequency is specified up to 320MHz. The outputs can be disabled, if not used. The outputs go to a logic 0 when disabled.

### **Reset Logic/POR**

During power-on, a power-on reset (POR) signal is generated to synchronize all dividers. An external master reset (MR) signal is not required.

### **Applications Information**

#### **Power-Supply Filtering**

The MAX3625B is a mixed analog/digital IC. The PLL contains analog circuitry susceptible to random noise. In addition to excellent on-chip power-supply noise rejection, the MAX3625B provides a separate power-supply pin, VCCA, for the VCO circuitry. Figure 1 illustrates the recommended power-supply filter network for VCCA. The purpose of this design technique is to ensure a clean power supply to the VCO circuitry and to improve the overall immunity to power-supply noise. This network requires that the power supply is  $+3.3V \pm 5\%$ . Decoupling capacitors should be used on all supply pins for best performance.

### **Output Divider Configuration**

Table 2 shows the input settings required to set the output dividers. Note that when the MAX3625B is in bypass mode (BYPASS set low), the output dividers are automatically set to divide by 1.

### **PLL Divider Configuration**

Table 3 shows the input settings required to set the PLL feedback divider.

**Table 2. Output Divider Configuration**

INPUT		NA/NB DIVIDER
SELA1/SELB1	SELA0/SELB0	
0	0	$\div 10$
0	1	$\div 2$
1	0	$\div 4$
1	1	$\div 5$

**Table 3. PLL Divider Configuration**

FB_SEL INPUT	M DIVIDER
0	$\div 25$
1	$\div 24$

**MAX3625B**

## Low-Jitter, Precision Clock Generator with Three Outputs

### Crystal Selection

The crystal oscillator is designed to drive a fundamental mode, AT-cut crystal resonator. See Table 4 for recommended crystal specifications. See Figure 3 for external capacitance connection.

**Table 4. Crystal Selection Parameters**

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Crystal Oscillation Frequency	$f_{osc}$	24.8		27	MHz
Shunt Capacitance	$C_0$		2.0	7.0	pF
Load Capacitance	$C_L$		18		pF
Equivalent Series Resistance (ESR)	$R_S$			50	$\Omega$
Maximum Crystal Drive Level				300	$\mu$ W

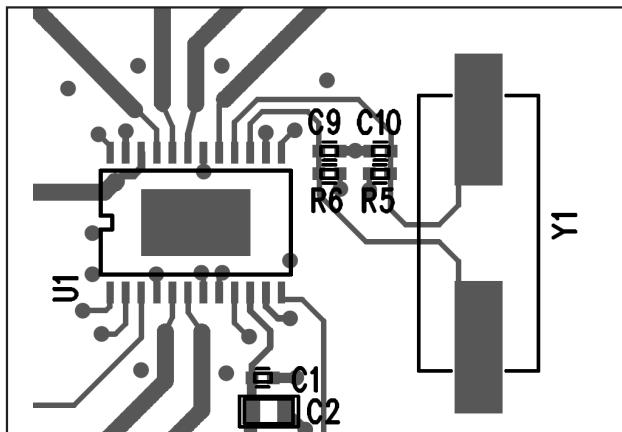


Figure 2. Crystal Layout

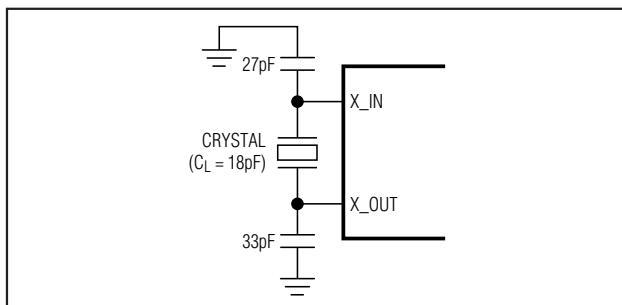


Figure 3. Crystal, Capacitors Connection

### Crystal Input Layout

The crystal, trace, and two external capacitors should be placed on the board as close as possible to the MAX3625B's X\_IN and X\_OUT pins to reduce crosstalk of active signals into the oscillator. The example layout shown in Figure 2 gives approximately 3pF of trace plus footprint capacitance per side of the crystal. The dielectric material is FR4 and dielectric thickness of the reference board is 15 mils. Using a 25MHz crystal and the capacitor values of  $C_{10} = 27\text{pF}$  and  $C_9 = 33\text{pF}$ , the measured output frequency accuracy is -14ppm at +25°C ambient temperature.

### Interfacing with LVPECL Outputs

The equivalent LVPECL output circuit is given in Figure 7. These outputs are designed to drive a pair of  $50\Omega$  transmission lines terminated with  $50\Omega$  to  $V_{TT} = V_{CC} - 2\text{V}$ . If a separate termination voltage ( $V_{TT}$ ) is not available, other termination methods can be used such as shown in Figures 4 and 5. Unused outputs should be disabled and may be left open. For more information on LVPECL terminations and how to interface with other logic families, refer to Application Note 291: HFAN-01.0: *Introduction to LVDS, PECL, and CML*.

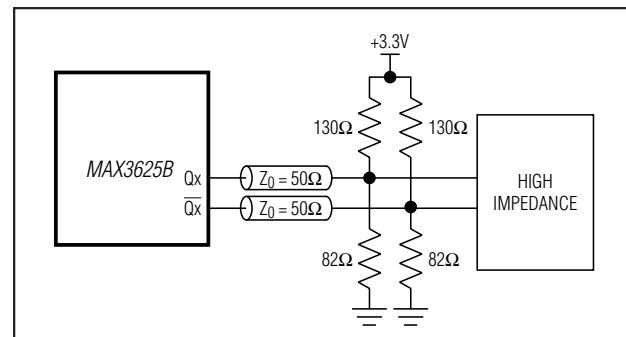


Figure 4. Thevenin Equivalent of Standard PECL Termination

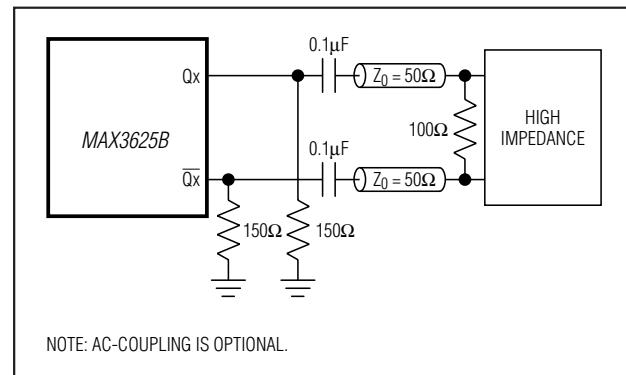


Figure 5. AC-Coupled PECL Termination

## Low-Jitter, Precision Clock Generator with Three Outputs

### Interface Models

Figures 6 and 7 show examples of interface models.

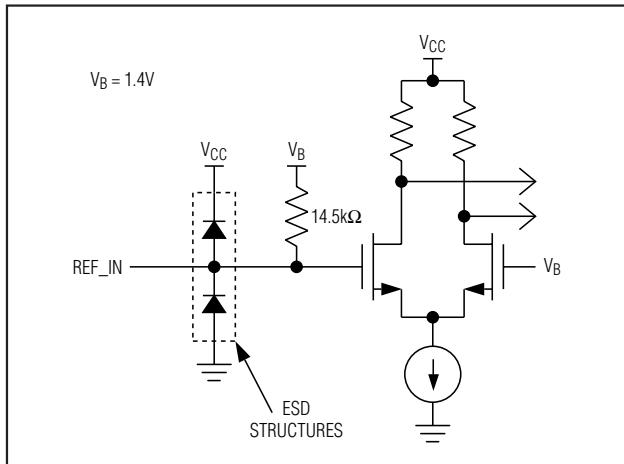


Figure 6. Simplified REF\_IN Pin Circuit Schematic

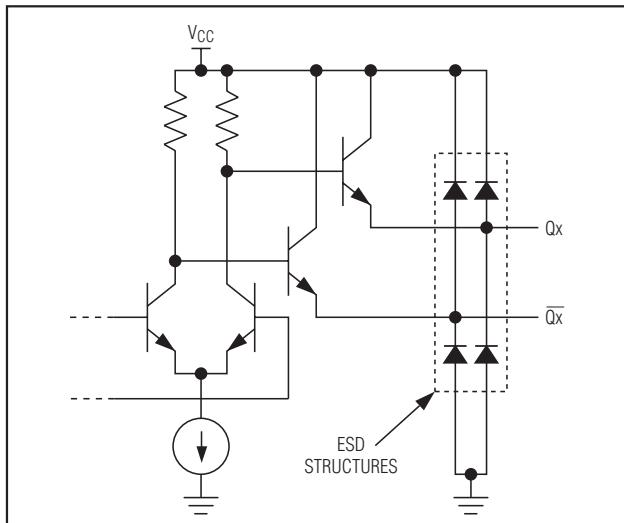


Figure 7. Simplified LVPECL Output Circuit Schematic

### Layout Considerations

The inputs and outputs are critical paths for the MAX3625B, and care should be taken to minimize discontinuities on these transmission lines. Here are some suggestions for maximizing the MAX3625B's performance:

- An uninterrupted ground plane should be positioned beneath the clock I/Os.
- Supply and ground pin vias should be placed close to the IC and the input/output interfaces to allow a return current path to the MAX3625B and the receive devices.
- Supply decoupling capacitors should be placed close to the MAX3625B supply pins.
- Maintain  $100\Omega$  differential (or  $50\Omega$  single-ended) transmission line impedance out of the MAX3625B.
- Use good high-frequency layout techniques and multilayer boards with an uninterrupted ground plane to minimize EMI and crosstalk.
- The 24-pin TSSOP-EP package features an exposed pad (EP), which provides a low-resistance thermal path for heat removal from the IC, and must be connected to the circuit board ground plane for proper operation.

Refer to the MAX3625B Evaluation Kit for more information.

### Chip Information

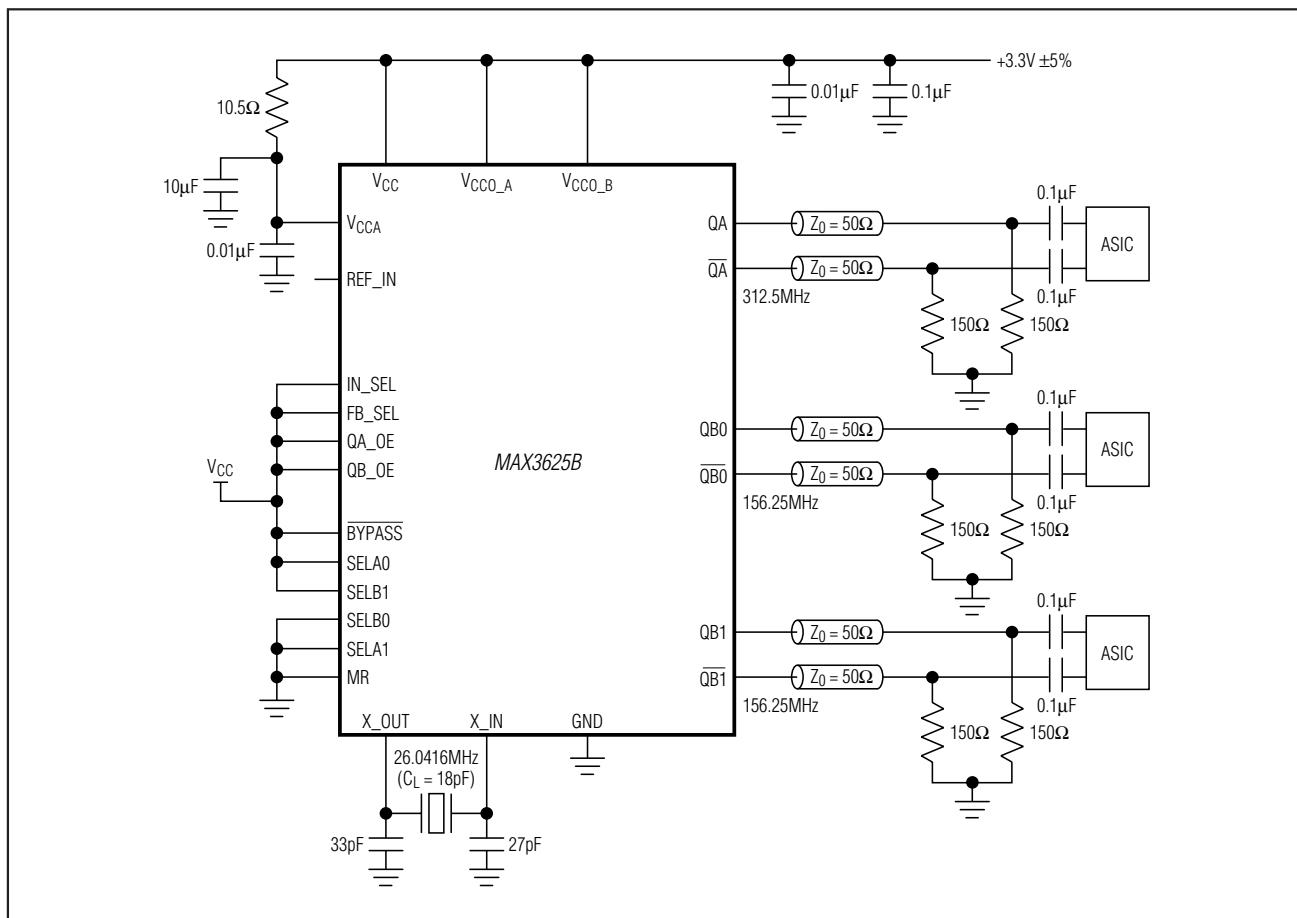
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PROCESS: BiCMOS

## **Low-Jitter, Precision Clock Generator with Three Outputs**

**MAX3625B**

### **Typical Application Circuit**



### **Package Information**

For the latest package outline information and land patterns, go to [www.microsemi.com](http://www.microsemi.com). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
24 TSSOP-EP	U24E+1	<a href="#">21-0108</a>

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