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PBSS4230QA

30 V, 2 A NPN low V_{CEsat} (BISS) transistor

23 August 2013

Product data sheet

1. General description

NPN low V_{CEsat} Breakthrough In Small Signal (BISS) transistor in a leadless ultra small DFN1010D-3 (SOT1215) Surface-Mounted Device (SMD) plastic package with visible and solderable side pads.

PNP complement: PBSS5230QA.

2. Features and benefits

- Very low collector-emitter saturation voltage V_{CEsat}
- High collector current capability I_C and I_{CM}
- High collector current gain h_{FE} at high I_C
- High energy efficiency due to less heat generation
- Reduced Printed-Circuit Board (PCB) area requirements
- Solderable side pads
- AEC-Q101 qualified

3. Applications

- Loadswitch
- Battery-driven devices
- Power management
- Charging circuits
- Power switches (e.g. motors, fans)

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CEO}	collector-emitter voltage	open base		-	-	30	V
I_C	collector current			-	-	2	A
I_{CM}	peak collector current	single pulse; $t_p \leq 1 \text{ ms}$		-	-	3	A
R_{CEsat}	collector-emitter saturation resistance	$I_C = 1 \text{ A}; I_B = 100 \text{ mA}; \text{pulsed}; t_p \leq 300 \mu\text{s}; \delta \leq 0.02; T_{amb} = 25^\circ\text{C}$		-	135	180	$\text{m}\Omega$



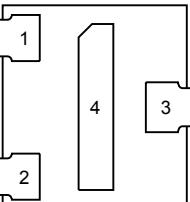
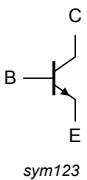
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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	B	base		
2	E	emitter		
3	C	collector		
4	C	collector	 Transparent top view DFN1010D-3 (SOT1215)	 sym123

6. Ordering information

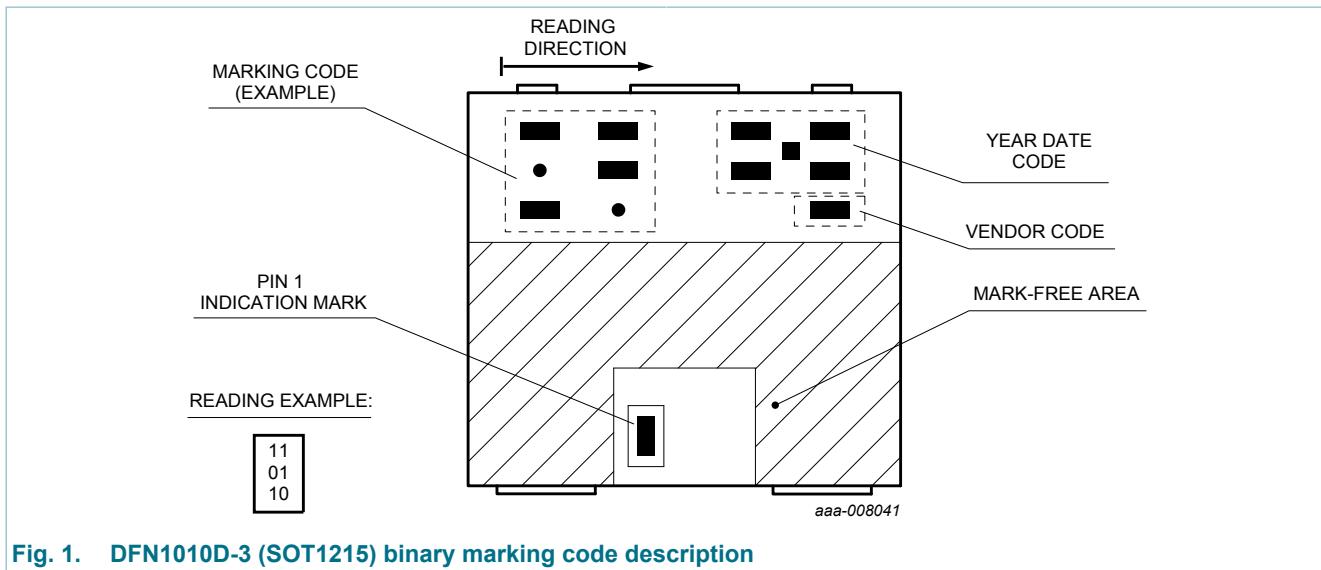
Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PBSS4230QA	DFN1010D-3	plastic thermal enhanced ultra thin small outline package; no leads; 3 terminals	SOT1215

7. Marking

Table 4. Marking codes

Type number	Marking code
PBSS4230QA	01 11 00



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8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

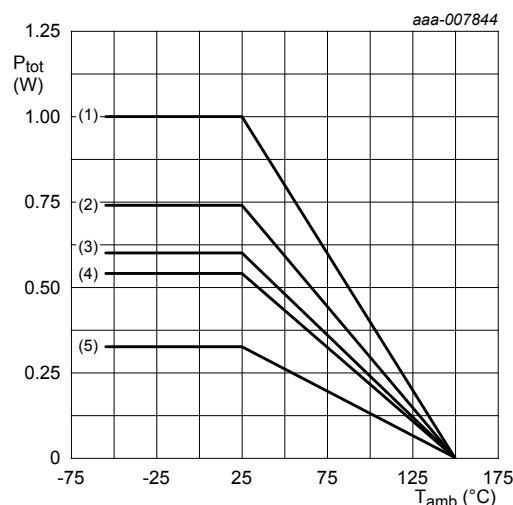
Symbol	Parameter	Conditions		Min	Max	Unit
V_{CBO}	collector-base voltage	open emitter		-	30	V
V_{CEO}	collector-emitter voltage	open base		-	30	V
V_{EBO}	emitter-base voltage	open collector		-	7	V
I_C	collector current			-	2	A
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms		-	3	A
I_B	base current			-	0.3	A
I_{BM}	peak base current	single pulse; $t_p \leq 1$ ms		-	1	A
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	325	mW
			[2]	-	600	mW
			[3]	-	740	mW
			[4]	-	540	mW
			[5]	-	1000	mW
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C

- [1] Device mounted on an FR4 PCB single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated mounting pad for collector 1 cm².
- [3] Device mounted on an FR4 PCB, single-sided copper, tin-plated mounting pad for collector 6 cm².
- [4] Device mounted on an FR4 PCB, 4-layer copper, tin-plated and standard footprint.
- [5] Device mounted on an FR4 PCB, 4-layer copper, tin-plated mounting pad for collector 1 cm².

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- (1) FR4 PCB, 4-layer copper, 1 cm²
- (2) FR4 PCB, single-sided copper, 6 cm²
- (3) FR4 PCB, single-sided copper, 1 cm²
- (4) FR4 PCB, 4-layer copper, standard footprint
- (5) FR4 PCB, single-sided copper, standard footprint

Fig. 2. Power derating curves

9. Thermal characteristics

Table 6. Thermal characteristics

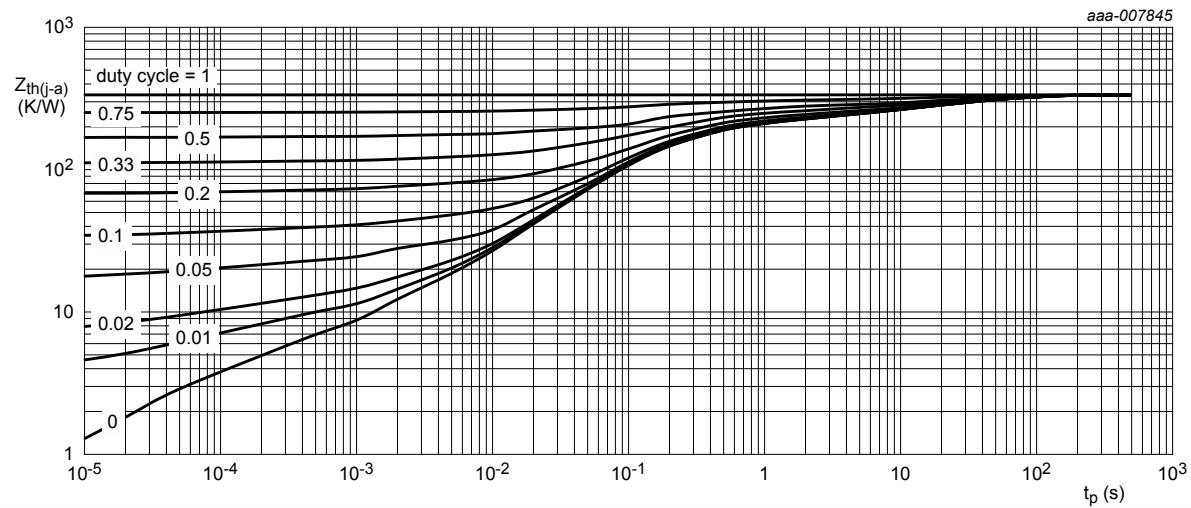
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	-	385	K/W
			[2]	-	-	209	K/W
			[3]	-	-	169	K/W
			[4]	-	-	232	K/W
			[5]	-	-	125	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated mounting pad for collector 1 cm².
- [3] Device mounted on an FR4 PCB, single-sided copper, tin-plated mounting pad for collector 6 cm².
- [4] Device mounted on an FR4 PCB, 4-layer copper, tin-plated and standard footprint.
- [5] Device mounted on an FR4 PCB, 4-layer copper, tin-plated mounting pad for collector 1 cm².

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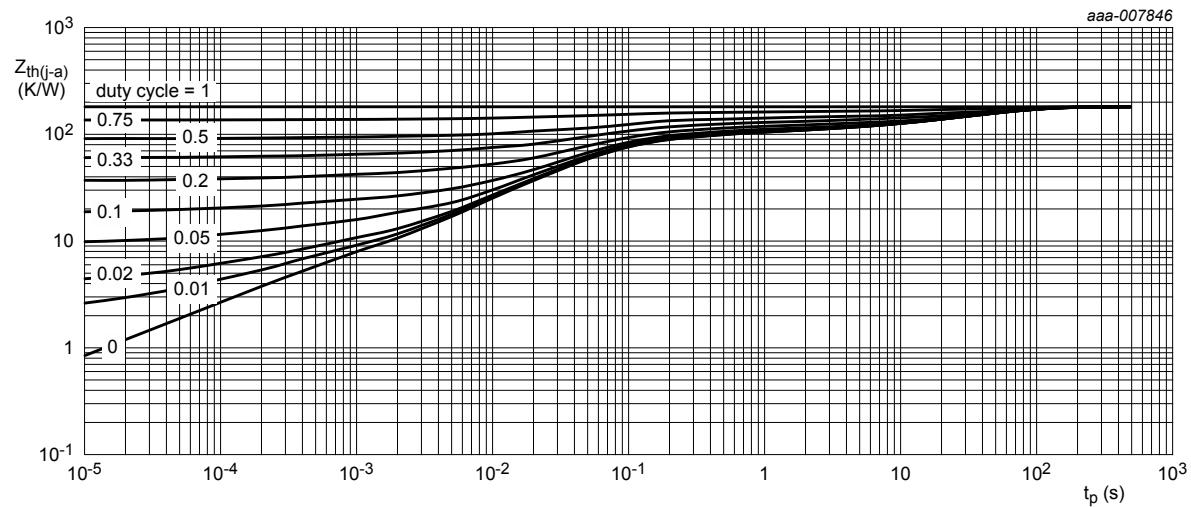
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FR4 PCB, single-sided copper, standard footprint

Fig. 3. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



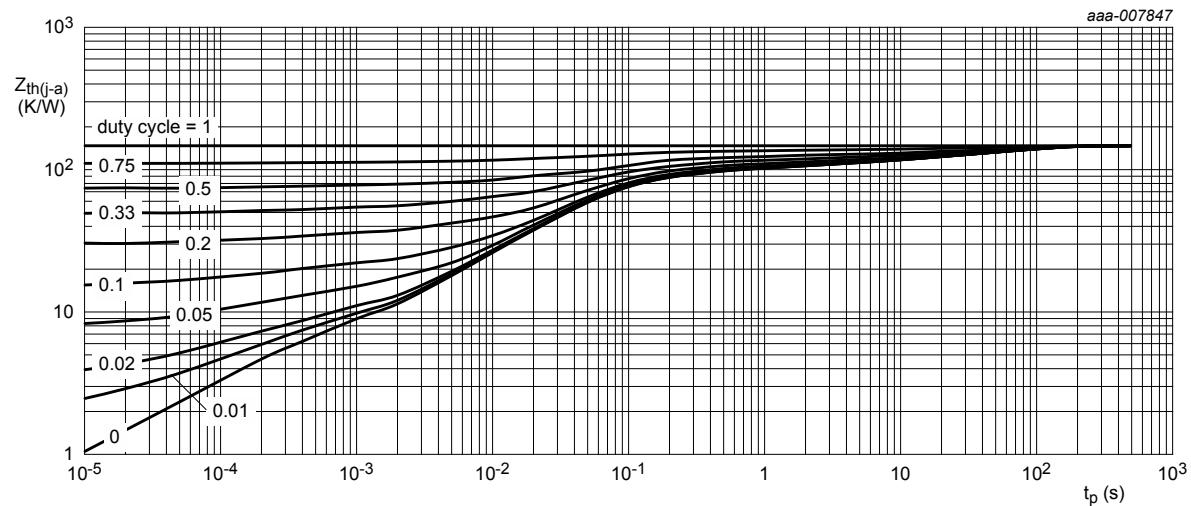
FR4 PCB, single-sided copper, 1 cm^2

Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

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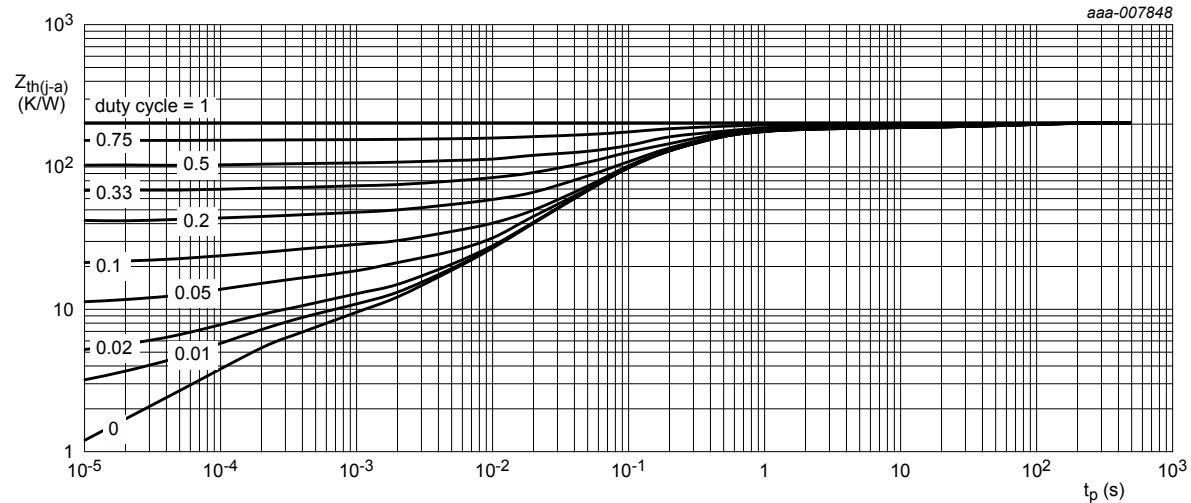
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FR4 PCB, single-sided copper, 6 cm²

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



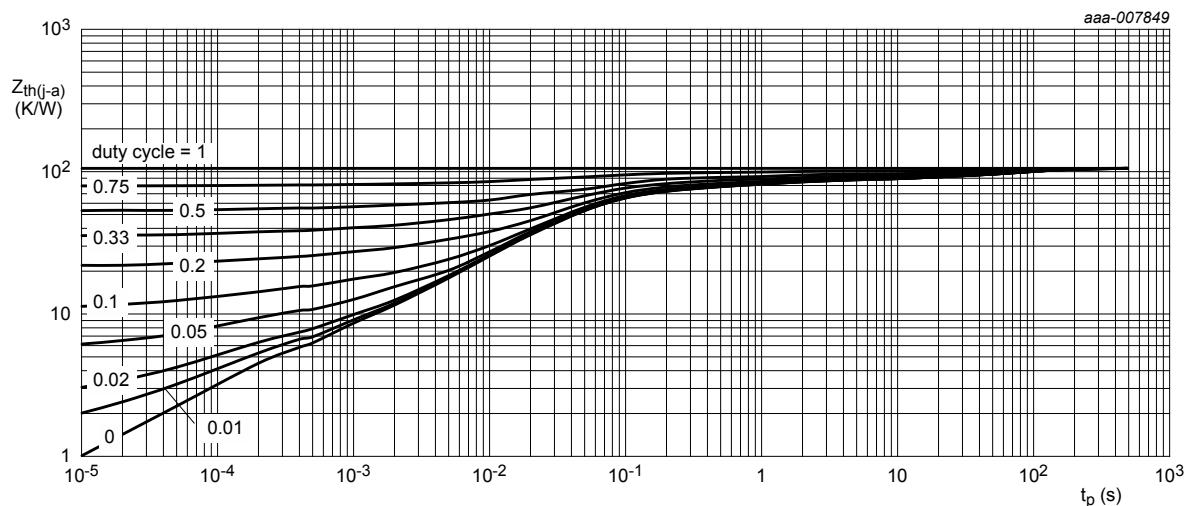
FR4 PCB, 4-layer copper, standard footprint

Fig. 6. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

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FR4 PCB, 4-layer copper, 1 cm²

Fig. 7. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I _{CBO}	collector-base cut-off current	V _{CB} = 24 V; I _E = 0 A; T _{amb} = 25 °C	-	-	100	nA
		V _{CB} = 24 V; I _E = 0 A; T _j = 150 °C	-	-	50	µA
I _{CES}	collector-emitter cut-off current	V _{CE} = 24 V; V _{BE} = 0 V; T _{amb} = 25 °C	-	-	100	nA
I _{EBO}	emitter-base cut-off current	V _{EB} = 5 V; I _C = 0 A; T _{amb} = 25 °C	-	-	100	nA
h _{FE}	DC current gain	V _{CE} = 2 V; I _C = 100 mA; pulsed; t _p ≤ 300 µs; δ ≤ 0.02 ; T _{amb} = 25 °C	250	430	-	
		V _{CE} = 2 V; I _C = 500 mA; pulsed; t _p ≤ 300 µs; δ ≤ 0.02 ; T _{amb} = 25 °C	230	380	-	
		V _{CE} = 2 V; I _C = 1 A; pulsed; t _p ≤ 300 µs; δ ≤ 0.02 ; T _{amb} = 25 °C	180	290	-	
		V _{CE} = 2 V; I _C = 2 A; pulsed; t _p ≤ 300 µs; δ ≤ 0.02 ; T _{amb} = 25 °C	100	160	-	
V _{CEsat}	collector-emitter saturation voltage	I _C = 500 mA; I _B = 50 mA; pulsed; t _p ≤ 300 µs; δ ≤ 0.02 ; T _{amb} = 25 °C	-	75	100	mV
		I _C = 1 A; I _B = 50 mA; pulsed; t _p ≤ 300 µs; δ ≤ 0.02 ; T _{amb} = 25 °C	-	140	190	mV
		I _C = 1 A; I _B = 100 mA; pulsed; t _p ≤ 300 µs; δ ≤ 0.02 ; T _{amb} = 25 °C	-	135	180	mV

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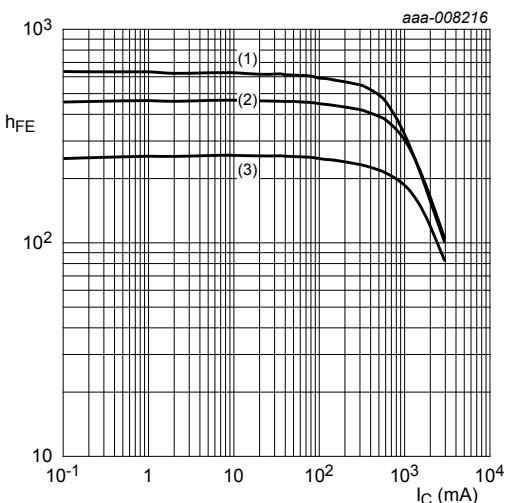
30 V, 2 A NPN low VCEsat (BISS) transistor

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		$I_C = 2 A$; $I_B = 100 \text{ mA}$; pulsed; $t_p \leq 300 \mu\text{s}$; $\delta \leq 0.02$; $T_{\text{amb}} = 25^\circ\text{C}$		-	265	360	mV
		$I_C = 2 A$; $I_B = 200 \text{ mA}$; pulsed; $t_p \leq 300 \mu\text{s}$; $\delta \leq 0.02$; $T_{\text{amb}} = 25^\circ\text{C}$					
R_{CEsat}	collector-emitter saturation resistance	$I_C = 1 A$; $I_B = 100 \text{ mA}$; pulsed; $t_p \leq 300 \mu\text{s}$; $\delta \leq 0.02$; $T_{\text{amb}} = 25^\circ\text{C}$		-	135	180	$\text{m}\Omega$
V_{BEsat}	base-emitter saturation voltage	$I_C = 500 \text{ mA}$; $I_B = 50 \text{ mA}$; pulsed; $t_p \leq 300 \mu\text{s}$; $\delta \leq 0.02$; $T_{\text{amb}} = 25^\circ\text{C}$		-	0.86	1	V
		$I_C = 1 A$; $I_B = 50 \text{ mA}$; pulsed; $t_p \leq 300 \mu\text{s}$; $\delta \leq 0.02$; $T_{\text{amb}} = 25^\circ\text{C}$					
		$I_C = 2 A$; $I_B = 100 \text{ mA}$; pulsed; $t_p \leq 300 \mu\text{s}$; $\delta \leq 0.02$; $T_{\text{amb}} = 25^\circ\text{C}$					
		$I_C = 2 A$; $I_B = 200 \text{ mA}$; pulsed; $t_p \leq 300 \mu\text{s}$; $\delta \leq 0.02$; $T_{\text{amb}} = 25^\circ\text{C}$					
V_{BEon}	base-emitter turn-on voltage	$V_{\text{CE}} = 2 \text{ V}$; $I_C = 0.5 \text{ A}$; pulsed; $t_p \leq 300 \mu\text{s}$; $\delta \leq 0.02$; $T_{\text{amb}} = 25^\circ\text{C}$		-	0.75	0.9	V
t_d	delay time	$V_{\text{CC}} = 10 \text{ V}$; $I_C = 0.5 \text{ A}$; $I_{\text{Bon}} = 25 \text{ mA}$; $I_{\text{Boff}} = -25 \text{ mA}$; $T_{\text{amb}} = 25^\circ\text{C}$		-	15	-	ns
t_r	rise time						
t_{on}	turn-on time						
t_s	storage time						
t_f	fall time						
t_{off}	turn-off time						
f_T	transition frequency	$V_{\text{CE}} = 10 \text{ V}$; $I_C = 50 \text{ mA}$; $f = 100 \text{ MHz}$; $T_{\text{amb}} = 25^\circ\text{C}$		130	190	-	MHz
C_c	collector capacitance	$V_{\text{CB}} = 10 \text{ V}$; $I_E = 0 \text{ A}$; $i_e = 0 \text{ A}$; $f = 1 \text{ MHz}$; $T_{\text{amb}} = 25^\circ\text{C}$		-	8	10	pF

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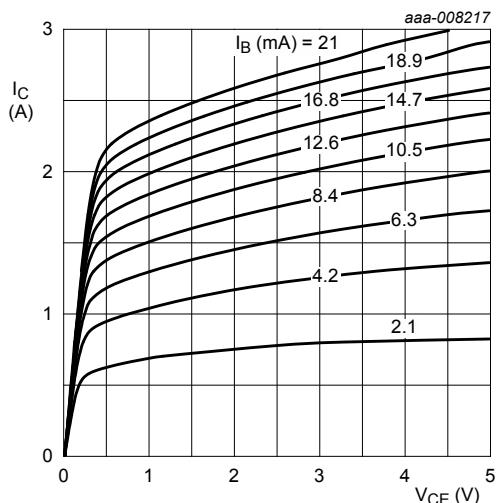
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$V_{CE} = 2 \text{ V}$

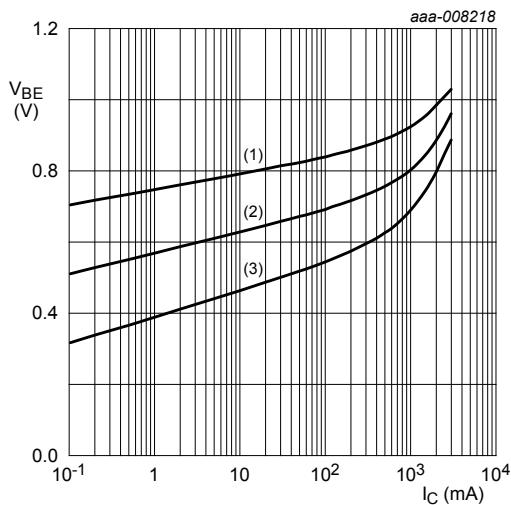
- (1) $T_{amb} = 100 \text{ }^{\circ}\text{C}$
- (2) $T_{amb} = 25 \text{ }^{\circ}\text{C}$
- (3) $T_{amb} = -55 \text{ }^{\circ}\text{C}$

Fig. 8. DC current gain as a function of collector current; typical values



$T_{amb} = 25 \text{ }^{\circ}\text{C}$

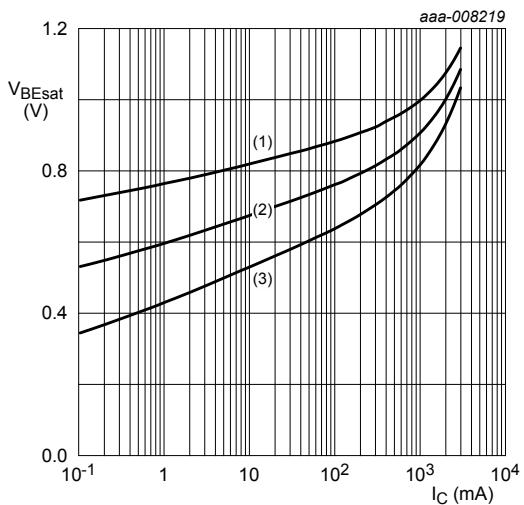
Fig. 9. Collector current as a function of collector-emitter voltage; typical values



$V_{CE} = 2 \text{ V}$

- (1) $T_{amb} = -55 \text{ }^{\circ}\text{C}$
- (2) $T_{amb} = 25 \text{ }^{\circ}\text{C}$
- (3) $T_{amb} = 100 \text{ }^{\circ}\text{C}$

Fig. 10. Base-emitter voltage as a function of collector current; typical values



$I_C/I_B = 20$

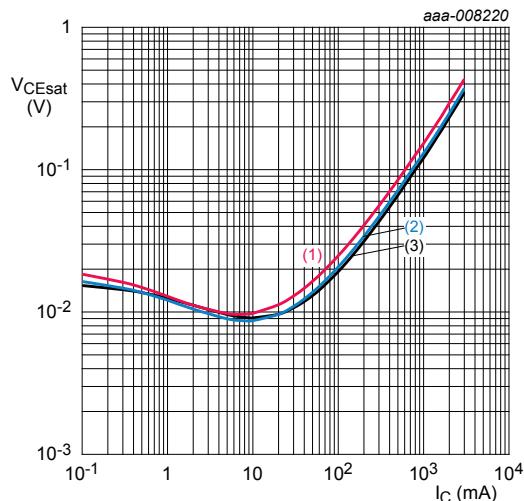
- (1) $T_{amb} = -55 \text{ }^{\circ}\text{C}$
- (2) $T_{amb} = 25 \text{ }^{\circ}\text{C}$
- (3) $T_{amb} = 100 \text{ }^{\circ}\text{C}$

Fig. 11. Base-emitter saturation voltage as a function of collector current; typical values

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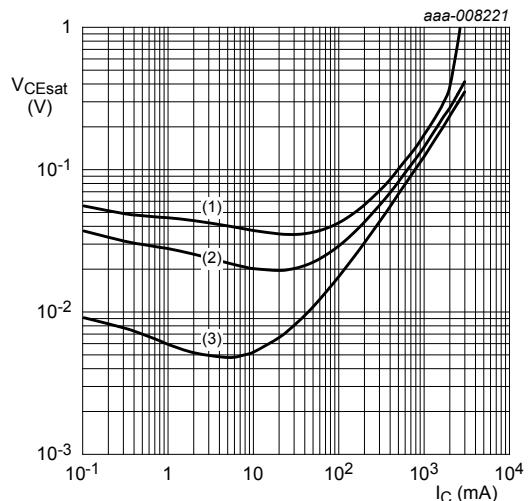
$I_C/I_B = 20$

(1) $T_{amb} = 100 \text{ } ^\circ\text{C}$

(2) $T_{amb} = 25 \text{ } ^\circ\text{C}$

(3) $T_{amb} = -55 \text{ } ^\circ\text{C}$

Fig. 12. Collector-emitter saturation voltage as a function of collector current; typical values



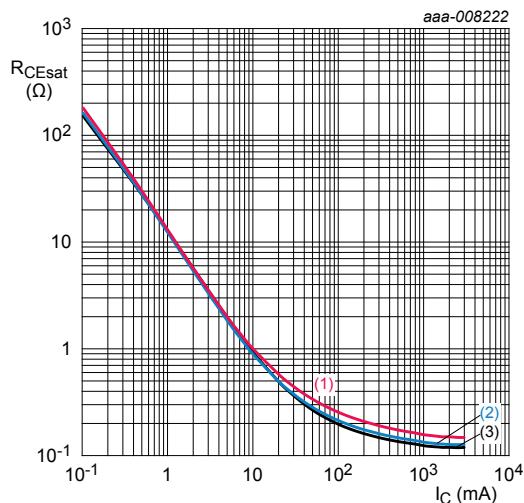
$T_{amb} = 25 \text{ } ^\circ\text{C}$

(1) $I_C/I_B = 100$

(2) $I_C/I_B = 50$

(3) $I_C/I_B = 10$

Fig. 13. Collector-emitter saturation voltage as a function of collector current; typical values



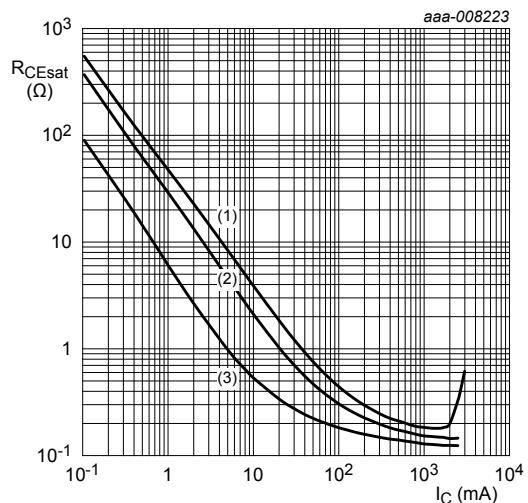
$I_C/I_B = 20$

(1) $T_{amb} = 100 \text{ } ^\circ\text{C}$

(2) $T_{amb} = 25 \text{ } ^\circ\text{C}$

(3) $T_{amb} = -55 \text{ } ^\circ\text{C}$

Fig. 14. Collector-emitter saturation resistance as a function of collector current; typical values



$T_{amb} = 25 \text{ } ^\circ\text{C}$

(1) $I_C/I_B = 100$

(2) $I_C/I_B = 50$

(3) $I_C/I_B = 10$

Fig. 15. Collector-emitter saturation resistance as a function of collector current; typical values

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11. Test information

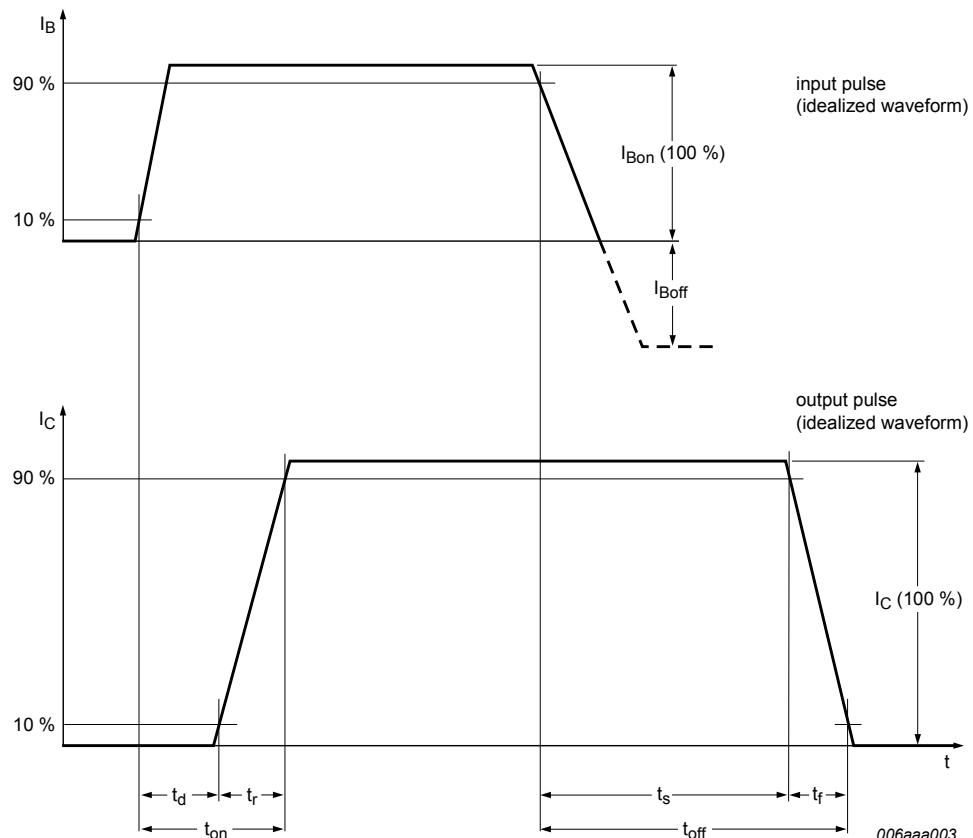


Fig. 16. BISS transistor switching time definition

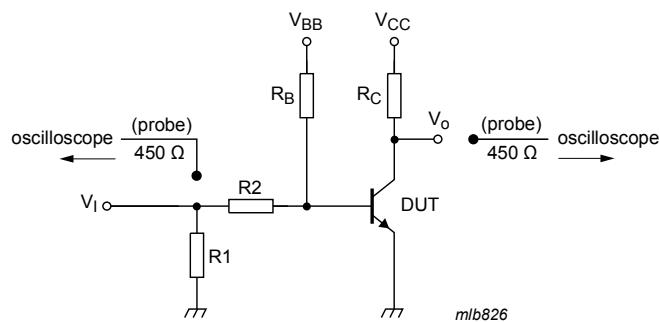
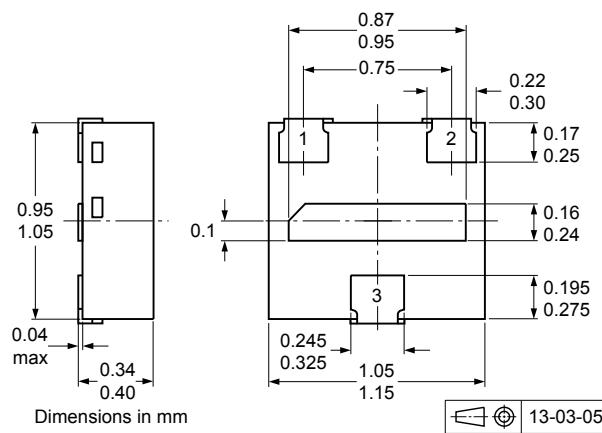


Fig. 17. Test circuit for switching times

11.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

NXP Semiconductors**PBSS4230QA****30 V, 2 A NPN low VCEsat (BISS) transistor****12. Package outline****Fig. 18. Package outline DFN1010D-3 (SOT1215)**

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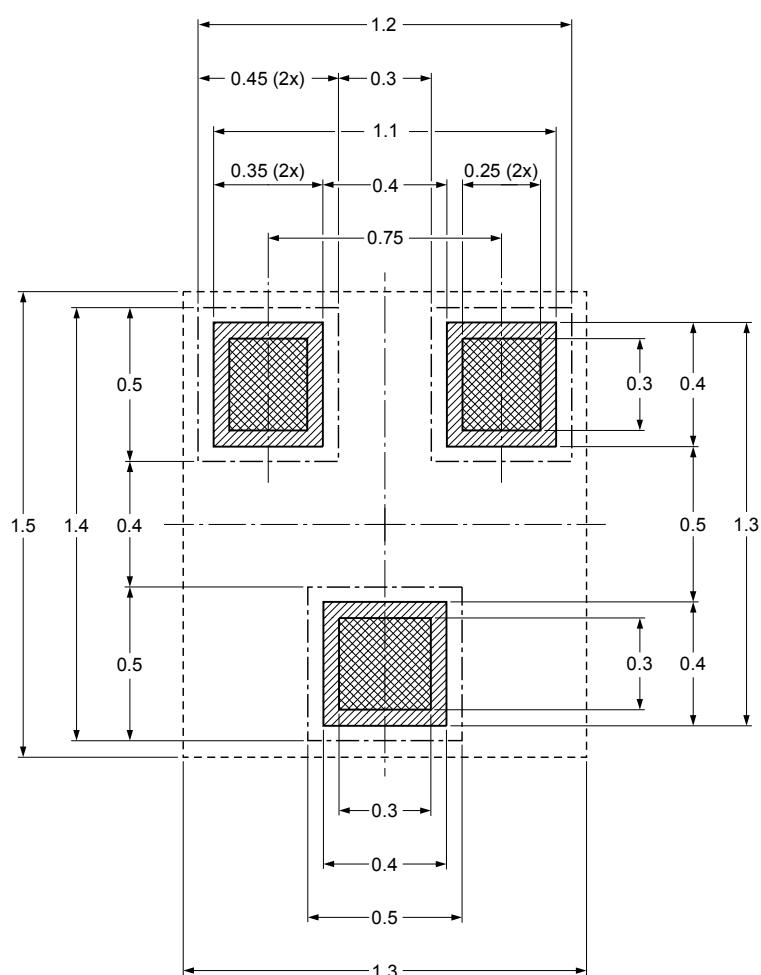
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13. Soldering

Footprint information for reflow soldering of DFN1010D-3 package

SOT1215



solder land



solder land plus solder paste



occupied area



solder resist

Dimensions in mm

Issue date 12-11-23
13-03-06

sot1215_fr

Fig. 19. Reflow soldering footprint for DFN1010D-3 (SOT1215)

NXP Semiconductors**PBSS4230QA****30 V, 2 A NPN low VCEsat (BISS) transistor****14. Revision history****Table 8. Revision history**

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PBSS4230QA v.1	20130823	Product data sheet	-	-

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15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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