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[SIHG47N65E-GE3](#)

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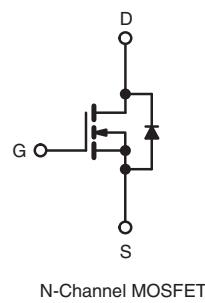
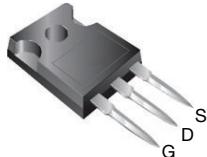
sales@integrated-circuit.com



E Series Power MOSFET

PRODUCT SUMMARY	
V_{DS} (V) at T_J max.	700
$R_{DS(on)}$ max. at 25 °C (Ω)	$V_{GS} = 10$ V 0.072
Q_g max. (nC)	273
Q_{gs} (nC)	46
Q_{gd} (nC)	79
Configuration	Single

TO-247AC



FEATURES

- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Renewable energy
 - Solar (PV inverters)

ORDERING INFORMATION

Package	TO-247AC
Lead (Pb)-free and Halogen-free	SiHG47N65E-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	650	V
Gate-Source Voltage	V_{GS}	± 30	
Continuous Drain Current ($T_J = 150$ °C)	I_D	47	A
		30	
	I_{DM}	139	
Pulsed Drain Current ^a		3.3	W/°C
Linear Derating Factor			
Single Pulse Avalanche Energy ^b	E_{AS}	1410	mJ
Maximum Power Dissipation	P_D	417	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	°C
Drain-Source Voltage Slope	dV/dt	37	V/ns
Reverse Diode dV/dt ^d		9	
Soldering Recommendations (Peak Temperature) ^c	for 10 s	300	°C

Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω, $I_{AS} = 10$ A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$, $di/dt = 100$ A/μs, starting $T_J = 25$ °C.

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	40	$^{\circ}\text{C}/\text{W}$
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.3	

SPECIFICATIONS ($T_J = 25^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$		650	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25°C , $I_D = 1 \text{ mA}$		-	0.70	-	$^{\circ}\text{C}/\text{C}$
Gate-Source Threshold Voltage (N)	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$		2	-	4	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA
		$V_{GS} = \pm 30 \text{ V}$		-	-	± 1	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 650 \text{ V}$, $V_{GS} = 0 \text{ V}$		-	-	1	μA
		$V_{DS} = 520 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 125^{\circ}\text{C}$		-	-	25	
Drain-Source On-State Resistance	$R_{DS(\text{on})}$	$V_{GS} = 10 \text{ V}$	$I_D = 24 \text{ A}$	-	0.060	0.072	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 30 \text{ V}$	$I_D = 24 \text{ A}$	-	16.7	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0 \text{ V}$, $V_{DS} = 100 \text{ V}$, $f = 1 \text{ MHz}$		-	5682	-	pF
Output Capacitance	C_{oss}			-	251	-	
Reverse Transfer Capacitance	C_{rss}			-	1	-	
Effective Output Capacitance, Energy Related ^a	$C_{o(er)}$	$V_{DS} = 0 \text{ V}$ to 520 V , $V_{GS} = 0 \text{ V}$		-	192	-	
Effective Output Capacitance, Time Related ^b	$C_{o(tr)}$			-	665	-	
Total Gate Charge	Q_g			-	182	273	nC
Gate-Source Charge	Q_{gs}	$V_{GS} = 10 \text{ V}$	$I_D = 24 \text{ A}$, $V_{DS} = 520 \text{ V}$	-	46	-	
Gate-Drain Charge	Q_{gd}			-	79	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 520 \text{ V}$, $I_D = 6 \text{ A}$, $V_{GS} = 10 \text{ V}$, $R_g = 9.1 \Omega$		-	47	94	ns
Rise Time	t_r			-	87	131	
Turn-Off Delay Time	$t_{d(off)}$			-	156	234	
Fall Time	t_f			-	103	206	
Gate Input Resistance	R_g	$f = 1 \text{ MHz}$, open drain		-	0.64	-	Ω
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	47	A
Pulsed Diode Forward Current	I_{SM}			-	-	139	
Diode Forward Voltage	V_{SD}	$T_J = 25^{\circ}\text{C}$, $I_S = 24 \text{ A}$, $V_{GS} = 0 \text{ V}$		-	0.9	1.2	V
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}\text{C}$, $I_F = I_S = 24 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_R = 25 \text{ V}$		-	753	1506	ns
Reverse Recovery Charge	Q_{rr}			-	14	28	μC
Reverse Recovery Current	I_{RRM}			-	28	-	A

Notes

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .
 b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

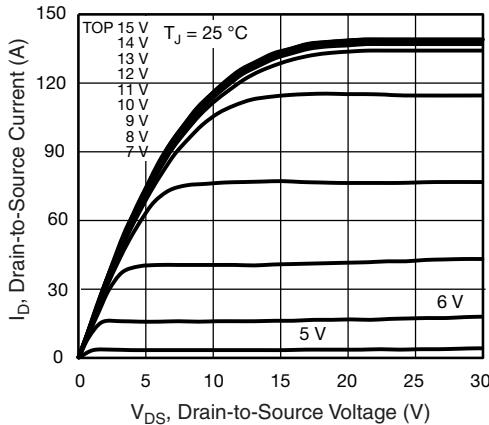


Fig. 1 - Typical Output Characteristics

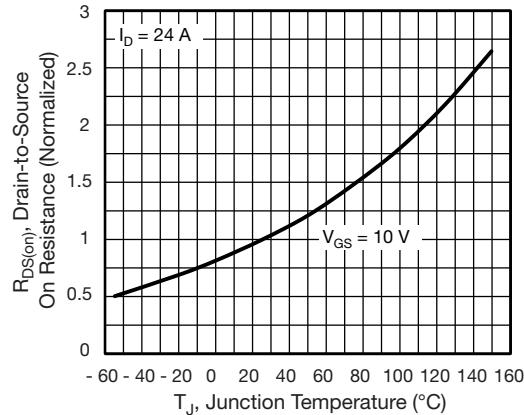


Fig. 4 - Normalized On-Resistance vs. Temperature

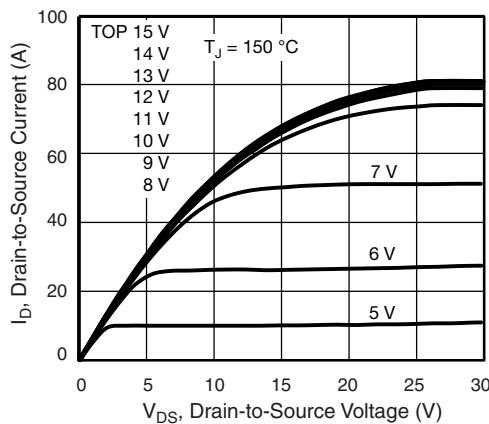


Fig. 2 - Typical Output Characteristics

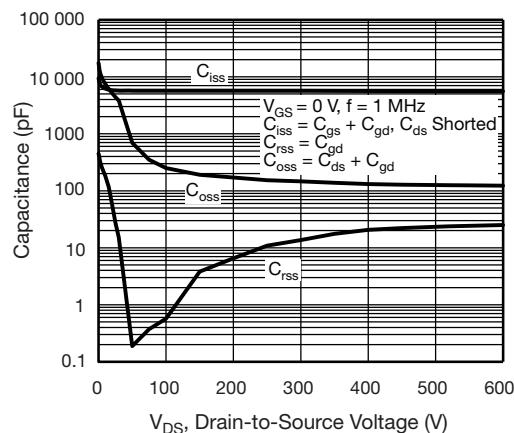


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

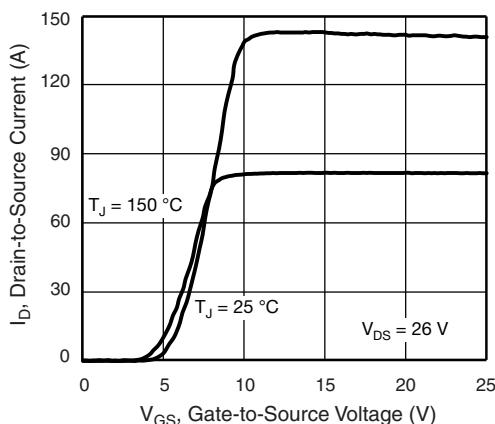


Fig. 3 - Typical Transfer Characteristics

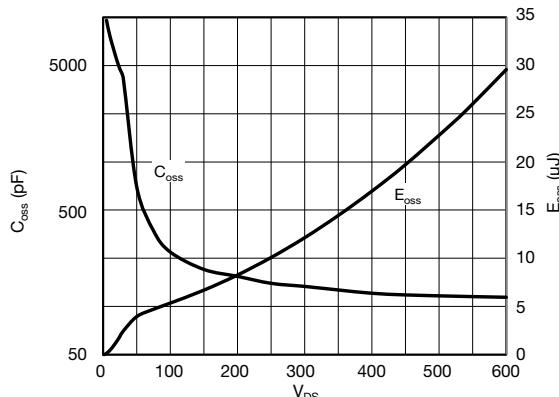


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}

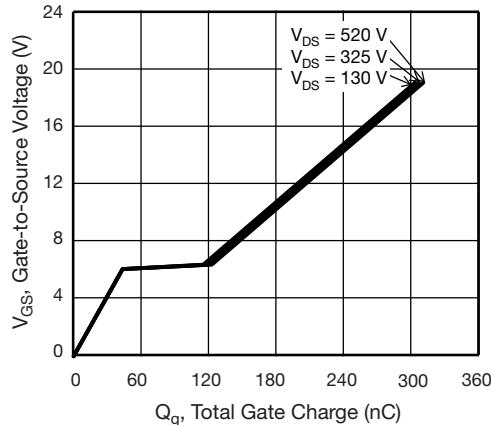


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

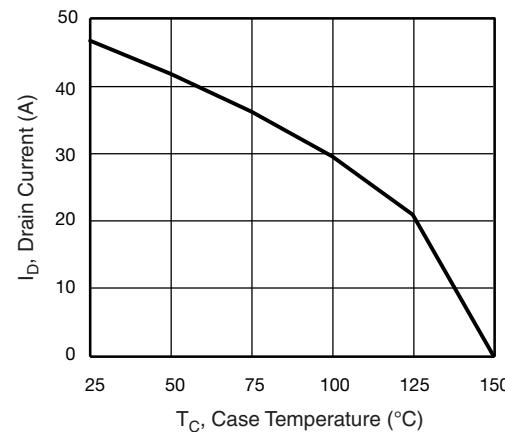


Fig. 10 - Maximum Drain Current vs. Case Temperature

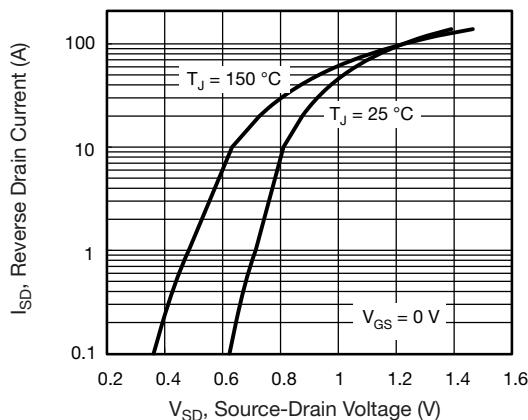


Fig. 8 - Typical Source-Drain Diode Forward Voltage

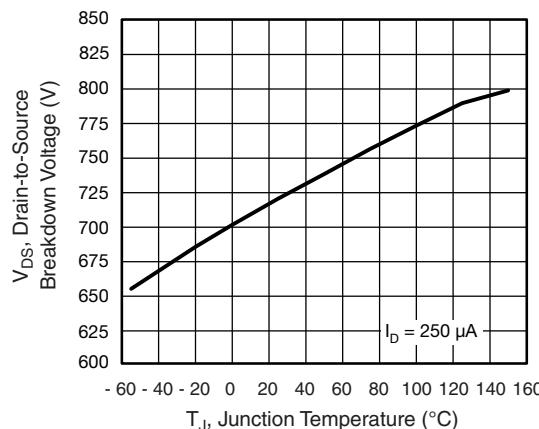


Fig. 11 - Temperature vs. Drain-to-Source Voltage

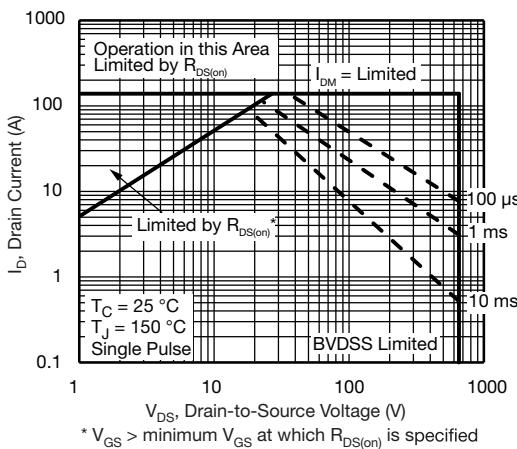


Fig. 9 - Maximum Safe Operating Area

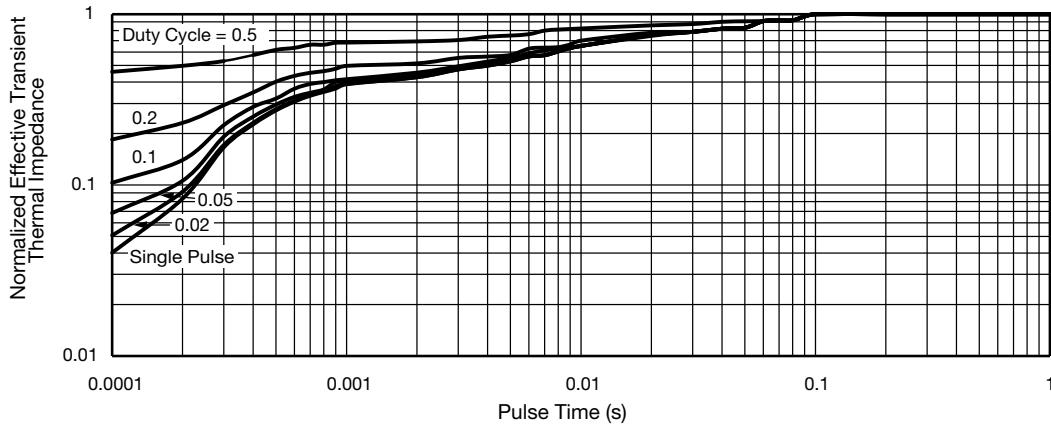


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

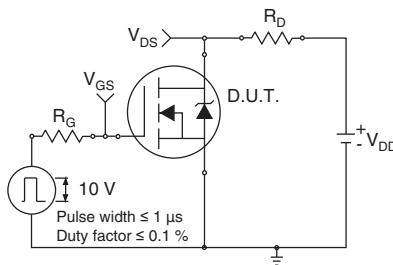


Fig. 13 - Switching Time Test Circuit

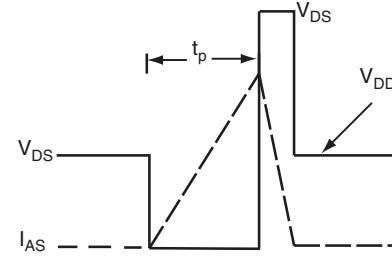


Fig. 16 - Unclamped Inductive Waveforms

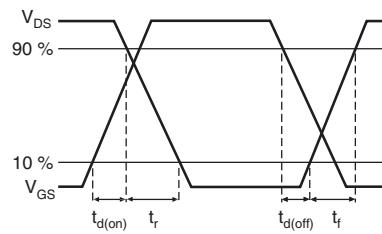


Fig. 14 - Switching Time Waveforms

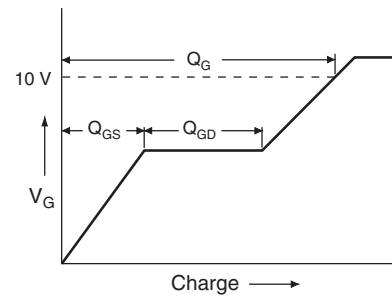


Fig. 17 - Basic Gate Charge Waveform

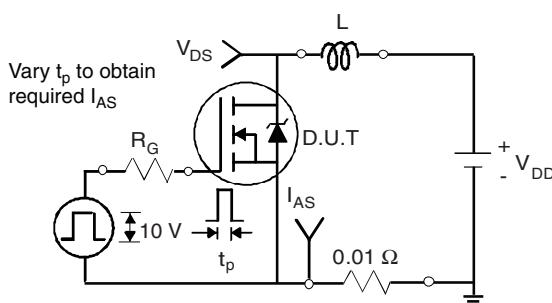


Fig. 15 - Unclamped Inductive Test Circuit

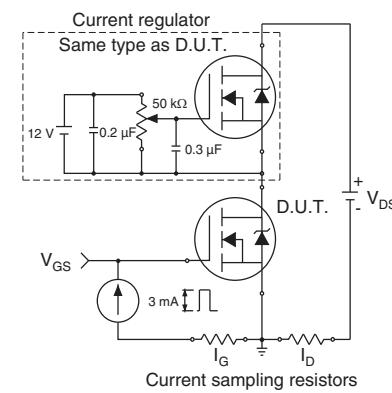


Fig. 18 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

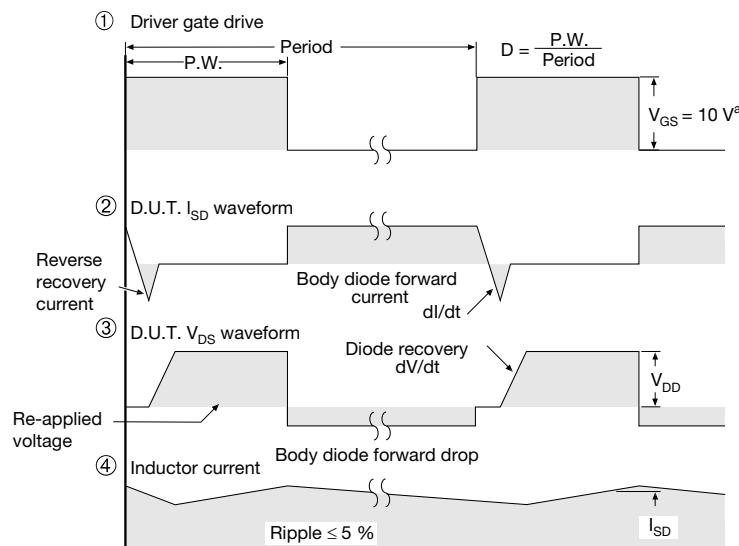
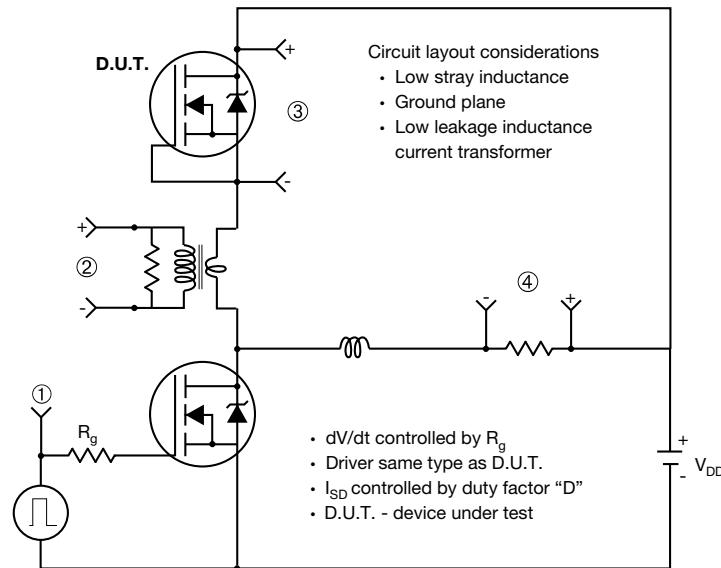


Fig. 19 - For N-Channel

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