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[SIHW73N60E-GE3](#)

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www.vishay.com
SiHW73N60E

Vishay Siliconix

E Series Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	650	
$R_{DS(on)}$ max. at 25 °C (Ω)	$V_{GS} = 10$ V	0.039
Q_g max. (nC)	362	
Q_{gs} (nC)	48	
Q_{gd} (nC)	98	
Configuration	Single	

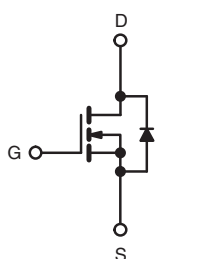
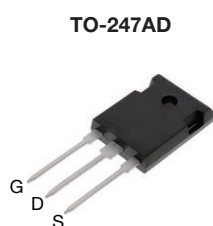
FEATURES

- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
 COMPLIANT
 HALOGEN
FREE

APPLICATIONS

- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Renewable energy
 - Solar (PV inverters)



N-Channel MOSFET

ORDERING INFORMATION	
Package	TO-247AD
Lead (Pb)-free and Halogen-free	SiHW73N60E-GE3


ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	600	V
Gate-Source Voltage	V_{GS}	± 20	
Gate-Source Voltage AC ($f > 1$ Hz)		30	
Continuous Drain Current ($T_J = 150$ °C)	V_{GS} at 10 V	$T_C = 25$ °C	73
		$T_C = 100$ °C	46
Pulsed Drain Current ^a	I_{DM}	236	A
Linear Derating Factor		4.2	W/°C
Single Pulse Avalanche Energy ^b	E_{AS}	2030	mJ
Maximum Power Dissipation	P_D	520	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	°C
Drain-Source Voltage Slope	$V_{DS} = 0$ V to 80 % V_{DS}	60	V/ns
Reverse Diode dV/dt ^d		8.4	
Soldering Recommendations (Peak Temperature)	for 10 s	300°	°C

Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 12$ A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$, $dI/dt = 30$ A/ μ s, starting $T_J = 25$ °C.



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	40	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.24	

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		600	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}, I_D = 250\text{ }\mu\text{A}$		-	0.65	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2	-	4	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$		-	-	1	μA
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	10	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 36\text{ A}$	-	0.032	0.039	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 40\text{ V}, I_D = 10\text{ A}$		-	12	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 100\text{ V}, f = 1\text{ MHz}$		-	7700	-	pF
Output Capacitance	C_{oss}			-	320	-	
Reverse Transfer Capacitance	C_{rss}			-	5	-	
Effective Output Capacitance, Energy Related ^a	$C_{o(er)}$	$V_{DS} = 0\text{ V to } 480\text{ V}, V_{GS} = 0\text{ V}$		-	259	-	pF
Effective Output Capacitance, Time Related ^b	$C_{o(tr)}$			-	907	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 24\text{ A}, V_{DS} = 480\text{ V}$	-	241	362	nC
Gate-Source Charge	Q_{gs}			-	48	-	
Gate-Drain Charge	Q_{gd}			-	98	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 480\text{ V}, I_D = 24\text{ A}, V_{GS} = 10\text{ V}, R_g = 10\text{ }\Omega$		-	63	95	ns
Rise Time	t_r			-	105	158	
Turn-Off Delay Time	$t_{d(off)}$			-	290	435	
Fall Time	t_f			-	120	180	
Gate Input Resistance	R_g	$f = 1\text{ MHz}, \text{open drain}$		-	1.52	-	Ω
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	73	A
Pulsed Diode Forward Current	I_{SM}			-	-	200	
Diode Forward Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 36\text{ A}, V_{GS} = 0\text{ V}$		-	0.9	1.2	V
Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = I_S = 24\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}, V_R = 25\text{ V}$		-	657	1314	ns
Reverse Recovery Charge	Q_{rr}			-	14.6	29.2	μC
Reverse Recovery Current	I_{RRM}			-	34.7	-	A

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .
 b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .



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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

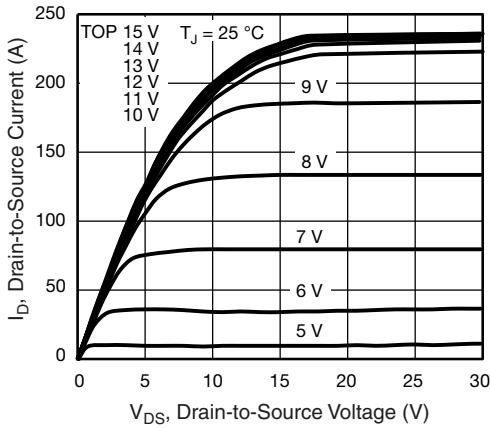


Fig. 1 - Typical Output Characteristics

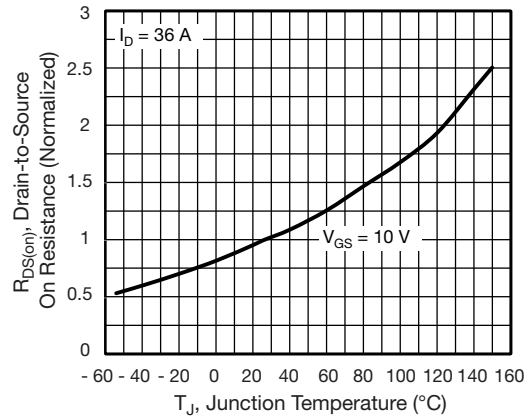


Fig. 3 - Normalized On-Resistance vs. Temperature

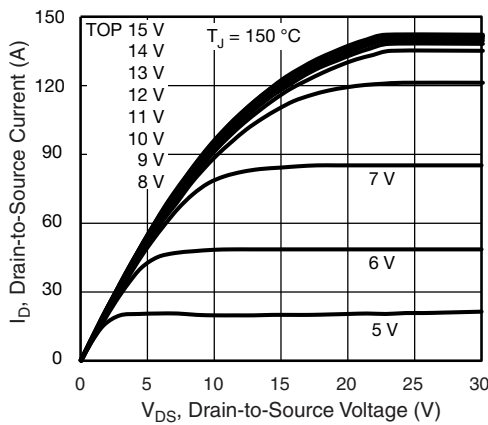


Fig. 1 - Typical Output Characteristics

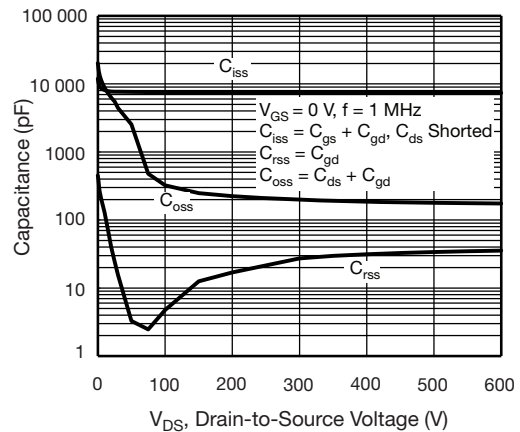


Fig. 4 - Typical Capacitance vs. Drain-to-Source Voltage

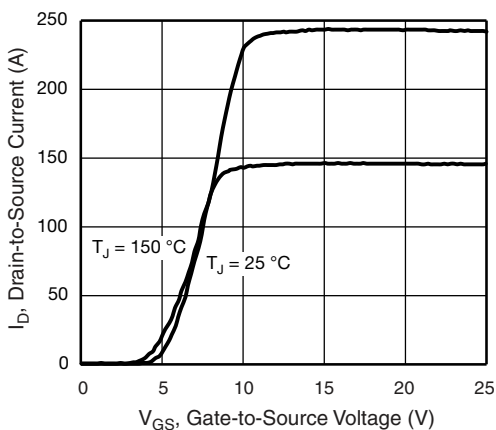


Fig. 2 - Typical Transfer Characteristics

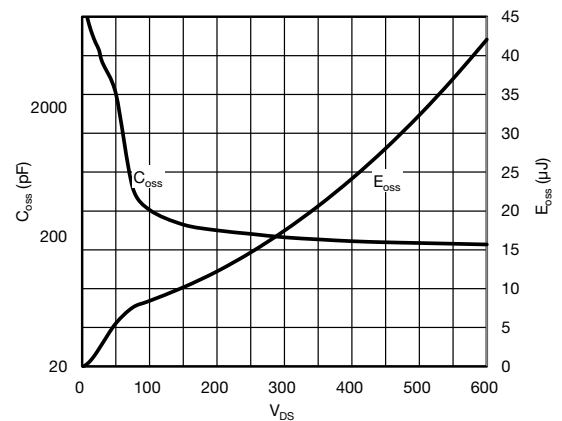


Fig. 5 - C_{oss} and E_{oss} vs. V_{DS}



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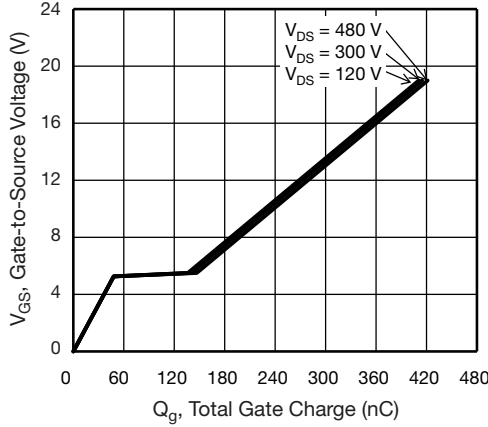


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

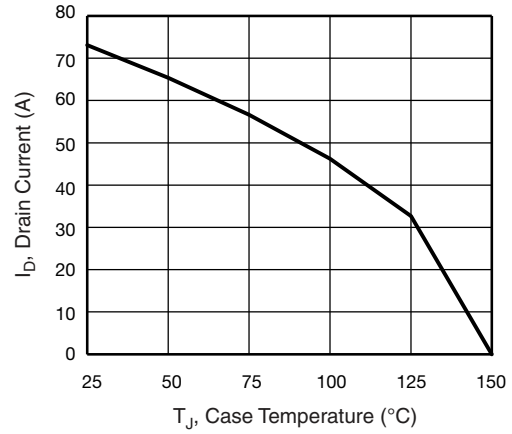


Fig. 9 - Maximum Drain Current vs. Case Temperature

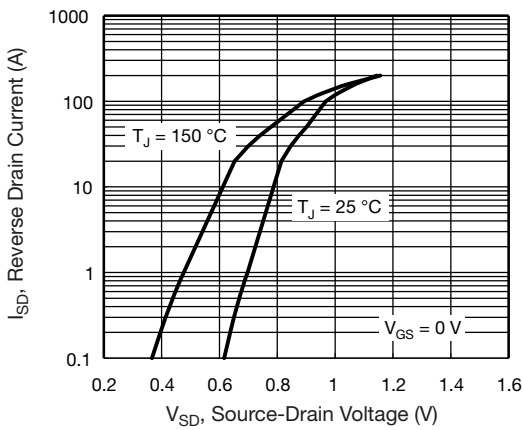


Fig. 7 - Typical Source-Drain Diode Forward Voltage

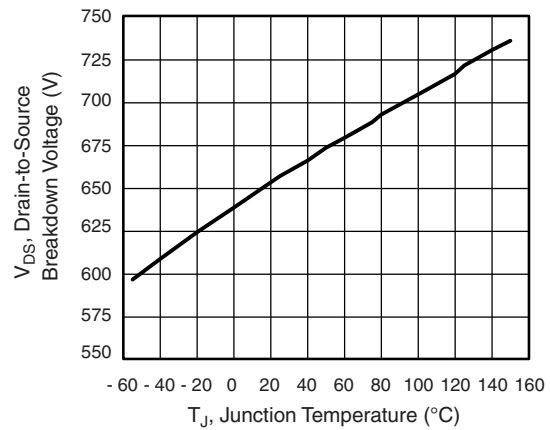


Fig. 10 - Temperature vs. Drain-to-Source Voltage

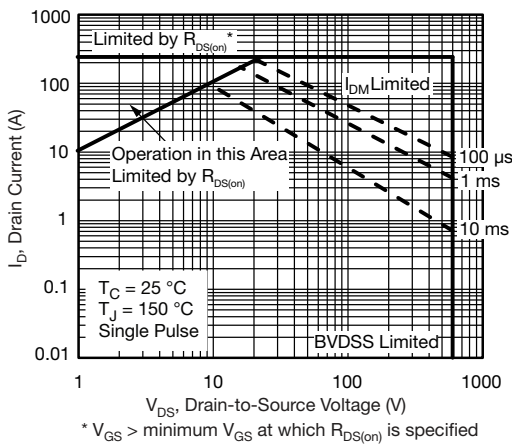


Fig. 8 - Maximum Safe Operating Area



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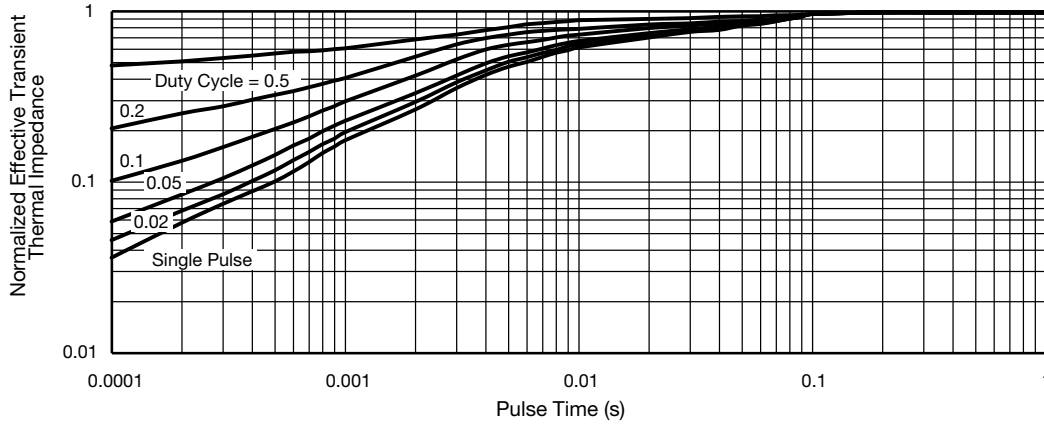


Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case

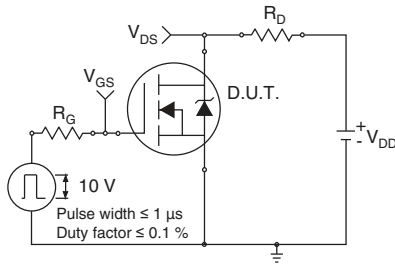


Fig. 12 - Switching Time Test Circuit

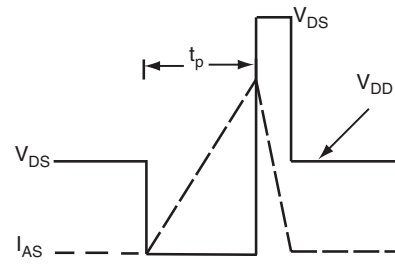


Fig. 15 - Unclamped Inductive Waveforms

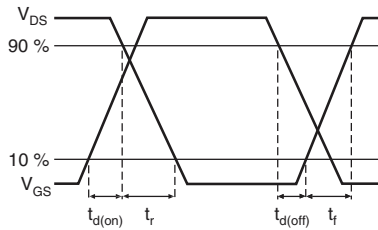


Fig. 13 - Switching Time Waveforms

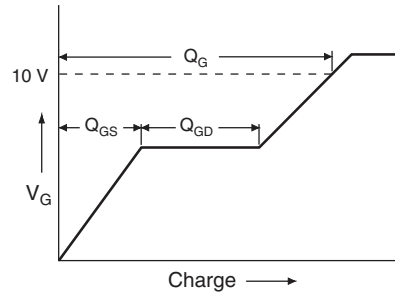


Fig. 16 - Basic Gate Charge Waveform

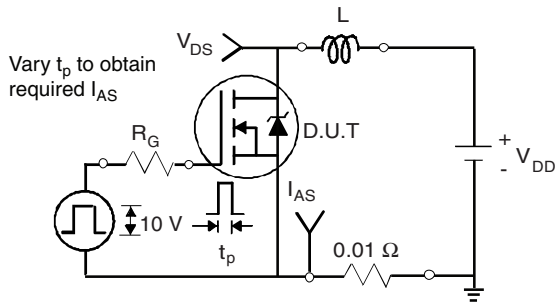


Fig. 14 - Unclamped Inductive Test Circuit

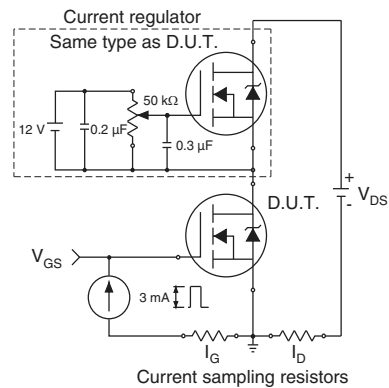
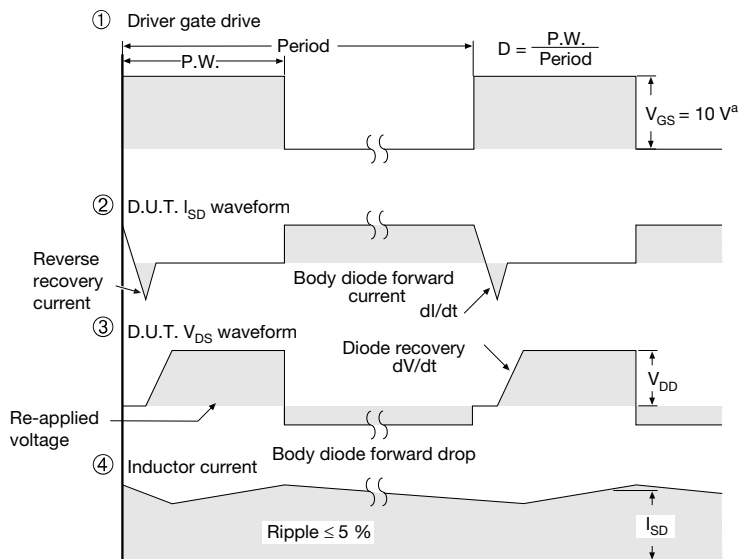
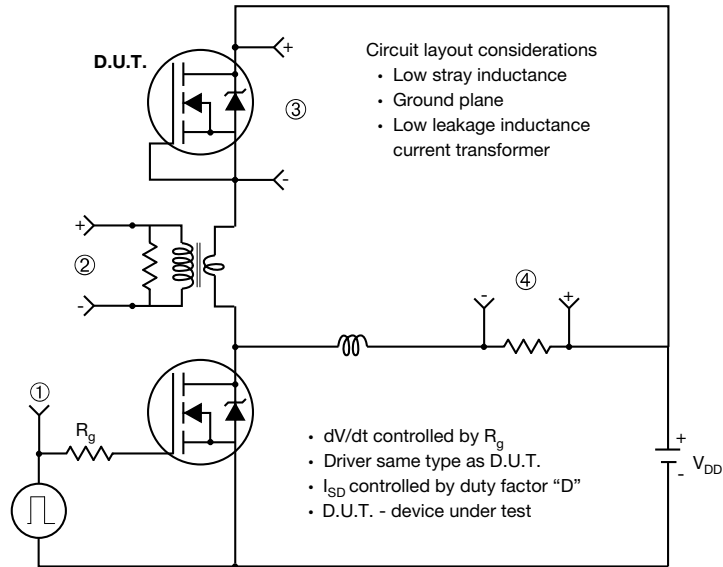


Fig. 17 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 18 - For N-Channel

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