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Integrated Transceiver Modules for ZigBee / 802.15.4 (900 MHz) Development Kit Available

FEATURES

- 250mW output power
- Long range: 2 miles
- Up to 1Mbps RF data rate
- Miniature footprint: 0.9" x 1.63"
- Multiple antenna options
- Agency Approvals: FCC and IC
- Powerful Atmel 256k ATXMEGA256A3U with 802.15.4 MAC or ZigBee Stack
- LSR serial interface based on 802.15.4 MAC
- Low power operation
- RoHS compliant
- Streamlined development with LSR design services.
- License options available to purchase design or integrate design.

APPLICATIONS

- Security
- Lighting Control
- HVAC Control
- Sensor Networks
- Medical
- Industrial Automation

ORDERING INFORMATION

DESCRIPTION

The SiFLEX02-R2 module is a high performance 900MHz IEEE 802.15.4 radio

(AT86RF212B & RF amplifier circuit) and microcontroller (ATXMEGA256A3U) in a cost effective, precertified footprint.



The module comes preloaded with the LSR host serial interface running on top of the Atmel 802.15.4 MAC.

Full debug and programming capabilities are included to develop custom applications. Easily load the ZigBee stack or 802.15.4 MAC onto the module and create your own network.

Need to get to market quickly? Not an expert in 802.15.4 or ZigBee? Need a custom antenna? Would you like to own the design? Would you like a custom design? Not quite sure what you need? Do you need help with your host board? LSR Design Services will be happy to develop custom hardware or software, integrate the design, or license the design so you can manufacture yourself. Contact us at sales@lsr.com or call us at 262-375-4400.

| Order Number | Description |
|--------------|--|
| 450-0123 | SiFLEX02-R2 Module with U.FL connector for external antenna. (Tray) SPQ = 25, MOQ = 50 |
| 450-0124 | SiFLEX02-R2 Module with wire antenna. (Tray) SPQ = 25, MOQ = 50 |
| 450-0125 | SiFLEX02-R2 Module with helical antenna. (Tray) SPQ = 25, MOQ = 50 |
| 450-0126 | SiFLEX02-R2 Module with RF castellation for off board antenna. Note: See Antenna Options section for more details. (Tray) SPQ = 25, MOQ = 50 |
| 450-0131 | SiFLEX02-R2 Development Kit with wire antenna. |

Table 1 Orderable SiFLEX02-R2 Model Numbers



MODULE ACCESSORIES

| Order Number | Description |
|--------------|---|
| 001-0002 | 900 MHz Dipole Antenna with Reverse Polarity SMA Connector |
| 080-0001 | U.FL to Reverse Polarity SMA Bulkhead Cable 105mm |

Table 2 Module Accessories





BLOCK DIAGRAM

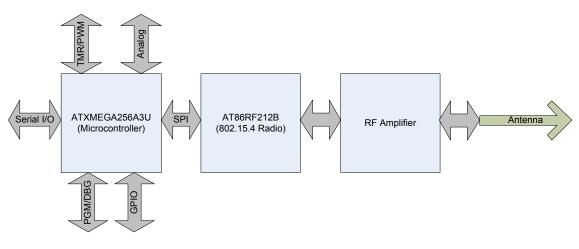


Figure 1 SiFLEX02-R2 Module Block Diagram – High-Level

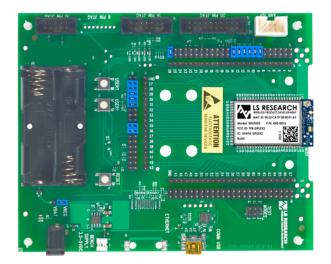
DEVELOPMENT KIT

The SiFLEX02-R2 Development Kit can be used out of the box to evaluate RF range performance with the simple press of a button.

Users interested in further investigating the performance and capabilities of the SiFLEX02-R2 Module can use the ModFLEX[™] Test Tool. This PC-based software can demonstrate just how easy it is to send & receive data, collect performance data, change channels, power levels, or addresses using the LSR Serial Host Protocol with another microcontroller.

More advanced users can use the development board to create and debug their own software for the SiFLEX02-R2 module using the 802.15.4 MAC or ZigBee stack from Atmel.

| Part Number | Description |
|-------------|-----------------------------|
| 450-0131 | SiFLEX02-R2 Development Kit |





Kit Contents

- ModFLEX[™] Development Board with SiFLEX02-R2 Module with Wire antenna (x2)
- USB Cable (x2)
- AA Batteries (x4)
- Quick Start Guide



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| |



MODULE PINOUT AND PIN DESCRIPTIONS

| - GND 2 68 GND - 67 GND - - NC 4 66 NC - 65 66 NC - - NC 5 65 NC - 66 NC - 67 - NC 6 63 NC - 63 NC - 63 - NC 7 63 NC - 63 NC - 61 - NC 8 61 PC5 24 10 JTAG TMS 9 61 PC5 24 11 JTAG TDI 10 60 PC6 22 12 JTAG TCK 11 59 PC7 23 13 JTAG TDO 12 58 PC4 20 56 JTAG/PDI/JRST 13 SiFLEX02 57 PE0 36 57 NRESET 14 (Atmel ATXMEGA256A3U) 56 PE1 37 62 PA0 15 55 NC 53 NC 53 63 PA1 18 52 NC 53 NC 54 5 PA7 19 51 | U# |
|---|----|
| - NC 4 66 NC - - NC 6 65 NC - - NC 7 63 NC - - NC 8 62 NC - 10 JTAG TMS 9 61 PC5 21 11 JTAG TCK 11 60 PC6 22 12 JTAG TCK 11 59 PC7 23 13 JTAG TDO 12 58 PC4 20 56 JTAG/PDI/JRST 13 SiFLEX02 57 PE0 36 62 PA0 15 55 NC - - - 64 PA2 17 (Atmel ATXMEGA256A3U) 56 PE1 37 63 PA1 18 52 NC - - 5 PA7 19 51 NC - - | |
| - NC 5 - NC 6 - NC 7 - NC 7 - NC 8 10 JTAG TMS 9 11 JTAG TDI 10 12 JTAG TCK 11 13 JTAG TDO 12 56 JTAG/PDI/JRST 13 SiFLEX02 57 PE0 57 nRESET 14 (Atmel ATXMEGA256A3U) 56 PE1 57 NC - 56 PB0 16 57 PA1 18 5 PA7 19 | |
| - NC 6 NC - - NC 7 63 NC - - NC 8 62 NC - 10 JTAG TMS 9 61 PC5 21 11 JTAG TDI 10 60 PC6 22 12 JTAG TCK 11 59 PC7 23 13 JTAG TDO 12 58 PC4 20 56 JTAG/PDI/JRST 13 SiFLEX02 57 PE0 36 57 nRESET 14 (Atmel ATXMEGA256A3U) 56 PE1 37 62 PA0 15 55 NC - 64 PA2 17 53 NC - 63 PA1 18 52 NC - 5 PA7 19 51 NC - | |
| - NC 7 - NC 8 10 JTAG TMS 9 11 JTAG TDI 10 12 JTAG TCK 11 13 JTAG TDO 12 56 JTAG/PDI/JRST 13 57 NRESET 14 (Atmel ATXMEGA256A3U) 56 55 NC 64 PA2 77 18 5 PA1 18 52 5 PA7 19 51 | |
| - NC 8 10 JTAG TMS 9 11 JTAG TDI 10 12 JTAG TCK 11 13 JTAG TDO 12 56 JTAG/PDI/JRST 13 SiFLEX02 57 57 nRESET 14 (Atmel ATXMEGA256A3U) 56 PE1 57 NC 64 PA2 63 PA1 5 PA1 5 PA1 | |
| 10 JTAG TMS 9 11 JTAG TDI 10 12 JTAG TCK 11 13 JTAG TDO 12 56 JTAG/PDI/JRST 13 57 nRESET 14 (Atmel ATXMEGA256A3U) 56 55 NC 64 PA2 63 PA1 5 PA7 18 51 56 PA7 56 PA7 | |
| 11 JTAG TDI 10 60 PC6 22 12 JTAG TCK 11 59 PC7 23 13 JTAG TDO 12 58 PC4 20 56 JTAG/PDI/JRST 13 SiFLEX02 57 PE0 36 57 nRESET 14 (Atmel ATXMEGA256A3U) 56 PE1 37 62 PA0 15 55 NC - 64 PA2 17 53 NC - 63 PA1 18 52 NC - 5 PA7 19 51 NC - | |
| 12 JTAG TCK 11 13 JTAG TDO 12 56 JTAG/PDI/JRST 13 57 nRESET 14 (Atmel ATXMEGA256A3U) 56 56 PB0 64 PA2 63 PA1 5 PA7 18 51 | |
| 13 JTAG TDO 12 56 JTAG/PDI/JRST 13 SiFLEX02 57 PE0 36 57 nRESET 14 (Atmel ATXMEGA256A3U) 56 PE1 37 62 PA0 15 55 NC - 64 PA2 17 53 NC - 63 PA1 18 52 NC - 5 PA7 19 51 NC - | 2 |
| 56 JTAG/PDI/JRST 13 SiFLEX02 57 PE0 36 57 nRESET 14 (Atmel ATXMEGA256A3U) 56 PE1 37 62 PA0 15 55 NC - 64 PA2 17 53 NC - 63 PA1 18 52 NC - 5 PA7 19 51 NC - | ¢. |
| 57 nRESET 14 (Atmel ATXMEGA256A3U) 56 PE1 37 62 PA0 15 55 NC - 6 PB0 16 54 NC - 64 PA2 17 53 NC - 63 PA1 18 52 NC - 5 PA7 19 51 NC - | , |
| 62 PA0 15 55 NC - 6 PB0 16 54 NC - 64 PA2 17 53 NC - 63 PA1 18 52 NC - 5 PA7 19 51 NC - | ; |
| 6 PB0 16 64 PA2 17 63 PA1 18 5 PA7 19 | |
| 64 PA2 17 63 PA1 18 5 PA7 19 | |
| 63 PA1 18 52 NC - 5 PA7 19 51 NC - | |
| 5 PA7 19 51 NC - | |
| | |
| | |
| 2 PA4 20 50 NC - | |
| 3 PA5 21 49 NC - | |
| 4 PA6 22 48 NC - | |
| 7 PB1 23 47 NC - | |
| 8 PB2 24 46 NC - | |
| 9 PB3 25 45 NC - | |
| - VCC - 3V3DC 26 44 GND - | |
| 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 | |
| PF3 PF3 PF3 PF5 PF5 PF5 PF3 PF3 PF3 PF3 PF3 PF3 PF3 PF3 PF3 PF3 | |
| PF3 PF4 PF4 PF5 PF5 PF5 PF5 PF6 PF6 PF6 PF7 PF6 PF7 PF7 PF7 PF7 PF7 PF7 PF7 PF7 PF7 PF7 | |
| | |
| PF3 PF3 PF4 PF4 PF5 PF5 PF3/UART TX PF3/UART TX PF3 PF5 PF5 PF5 PF5 PF5 PF5 PF5 PF5 PF5 PF5 | |
| | |
| MCU# 49 48 47 46 41 40 39 38 19 18 17 16 51 54 55 1 - MC | J# |

Figure 3 Module Pinout



| Module Pin | Name | MCU Pin | Туре | Description | |
|---------------|---------------|------------|-------|---|--|
| 1 | GND | N/A | GND | Ground | |
| 2 | GND | N/A | GND | Ground | |
| 3 | GND | N/A | GND | Ground | |
| 4 | NC | N/A | NC | No Connect | |
| 5 | NC | N/A | NC | No Connect | |
| 6 | NC | N/A | NC | No Connect | |
| 7 | NC | N/A | NC | No Connect | |
| 8 | NC | N/A | NC | No Connect | |
| 9 | JTAG TMS | 10 | I/O | General-purpose digital I/O (PB4), Analog input, JTAG TMS | |
| 10 | JTAG TDI | 11 | I/O | General-purpose digital I/O (PB5), Analog input, JTAG TDI | |
| 11 | JTAG TCK | 12 | I/O | General-purpose digital I/O (PB6), Analog input, JTAG TCK | |
| 12 | JTAG TDO | 13 | I/O | General-purpose digital I/O (PB7), Analog input, JTAG TDO | |
| 13 | JTAG/PDI/JRST | 56 | I/O | PDI/PDI_DATA | |
| 14 | nRESET | 57 | Input | RESET/PDI_CLOCK | |
| 15 | PA0 | 62 | I/O | General-purpose digital I/O, Analog input, Analog REF A | |
| 16 | PB0 | 6 | I/O | General-purpose digital I/O, Analog input, Analog REF B | |
| 17 | PA2 | 64 | I/O | General-purpose digital I/O, Analog input, Analog comparator 2 | |
| 18 | PA1 | 63 | I/O | General-purpose digital I/O, Analog input, Analog comparator 1 | |
| 19 | PA7 | 5 | I/O | General-purpose digital I/O, Analog input, Analog comparator output | |
| 20 | PA4 | 2 | I/O | General-purpose digital I/O, Analog input | |
| 21 | PA5 | 3 | I/O | General-purpose digital I/O, Analog input | |
| 22 | PA6 | 4 | I/O | General-purpose digital I/O, Analog input | |
| 23 | PB1 | 7 | I/O | General-purpose digital I/O, Analog input | |
| 24 | PB2 | 8 | I/O | General-purpose digital I/O, Analog input | |
| 25 | PB3 | 9 | I/O | General-purpose digital I/O, Analog input | |
| 26 | VCC - 3V3DC | VCC | VCC | Supply Voltage | |
| 27 | PF3 | 49 | I/O | General-purpose digital I/O, Output Compare, UART Tx | |
| 28 | PF2 | 48 | I/O | General-purpose digital I/O, Output Compare, UART Rx | |
| 29 | PF1 | 47 | I/O | General-purpose digital I/O, Output Compare, UART XCK0 | |
| 30 | PF0 | 46 | I/O | General-purpose digital I/O, Output Compare | |



| Module Pin | Name | MCU Pin | Туре | Description | |
|---------------|--------------|------------|------|---|--|
| 31 | PE5 | 41 | I/O | General-purpose digital I/O, Output Compare, UART XCK1, SPI MOSI | |
| 32 | PE4 | 40 | I/O | General-purpose digital I/O, Output Compare, SPI SS | |
| 33 | PE3 | 39 | I/O | General-purpose digital I/O, Output Compare, UART Tx | |
| 34 | PE2 | 38 | I/O | General-purpose digital I/O, Output Compare, UART Rx | |
| 35 | PC3, UART TX | 19 | I/O | General-purpose digital I/O, Output Compare, UART Tx | |
| 36 | PC2, UART RX | 18 | I/O | General-purpose digital I/O, Output Compare, UART Rx | |
| 37 | PC1 | 17 | I/O | General-purpose digital I/O, Output Compare, IIC SCL | |
| 38 | PC0 | 16 | I/O | General-purpose digital I/O, Output Compare, IIC SDA | |
| 39 | PF5 | 51 | I/O | General-purpose digital I/O | |
| 40 | PF6 | 54 | I/O | General-purpose digital I/O | |
| 41 | PF7 | 55 | I/O | General-purpose digital I/O | |
| 42 | PA3 | 1 | I/O | General-purpose digital I/O, Analog input | |
| 43 | NC | N/A | NC | No Connect | |
| 44 | GND | N/A | GND | Ground | |
| 45 | NC | N/A | NC | No Connect | |
| 46 | NC | N/A | NC | No Connect | |
| 47 | NC | N/A | NC | No Connect | |
| 48 | NC | N/A | NC | No Connect | |
| 49 | NC | N/A | NC | No Connect | |
| 50 | NC | N/A | NC | No Connect | |
| 51 | NC | N/A | NC | No Connect | |
| 52 | NC | N/A | NC | No Connect | |
| 53 | NC | N/A | NC | No Connect | |
| 54 | NC | N/A | NC | No Connect | |
| 55 | NC | N/A | NC | No Connect | |
| 56 | PE1 | 37 | I/O | General-purpose digital I/O, Output Compare, IIC SCL | |
| 57 | PE0 | 36 | I/O | General-purpose digital I/O, Output Compare, IIC SDA | |
| 58 | PC4 | 20 | I/O | General-purpose digital I/O, Output Compare, SPI SS | |
| 59 | PC7 | 23 | I/O | General-purpose digital I/O, Output Compare, UART Tx, SPI SCK | |
| 60 | PC6 | 22 | I/O | General-purpose digital I/O, Output Compare, UART Rx, SPI MISO | |



| Module Pin | Name | MCU Pin | Туре | Description |
|---------------|------|------------|------|--|
| 61 | PC5 | 21 | I/O | General-purpose digital I/O, Output Compare, UART XCK1, SPI MOSI |
| 62 | NC | N/A | NC | No Connect |
| 63 | NC | N/A | NC | No Connect |
| 64 | NC | N/A | NC | No Connect |
| 65 | NC | N/A | NC | No Connect |
| 66 | NC | N/A | NC | No Connect |
| 67 | GND | N/A | GND | Ground |
| 68 | GND | N/A | GND | Ground |
| 69 | GND | N/A | GND | Ground |

Table 3 SiFLEX02-R2 Module Pin Descriptions

The information in this document is subject to change without notice.



MODULE OVERVIEW

Figure 4 shows the internal interconnects of the ICs on the SiFLEX02-R2 module. Consult the respective IC datasheets for details, or contact LSR sales to purchase the SiFLEX02-R2 module schematics as part of LSR's ModFLEX[™] design program. For a high-level block diagram of the SiFLEX02-R2 module, see Figure 1.

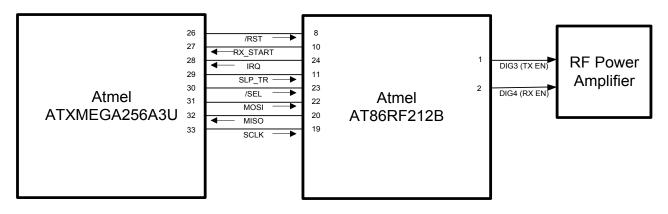


Figure 4 SiFLEX02-R2 Module Block Diagram – Internal Interconnects

Microcontroller

The AVR XMEGA A3U is a family of low power, high performance and peripheral rich CMOS 8/16-bit microcontrollers based on the AVR® enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the XMEGA A3U achieves throughputs approaching 1 Million Instructions Per Second (MIPS), thus allowing the system designer to optimize power consumption versus processing speed. Figure 5 shows a block diagram of the ATXMEGA256A3U.

The information in this document is subject to change without notice.



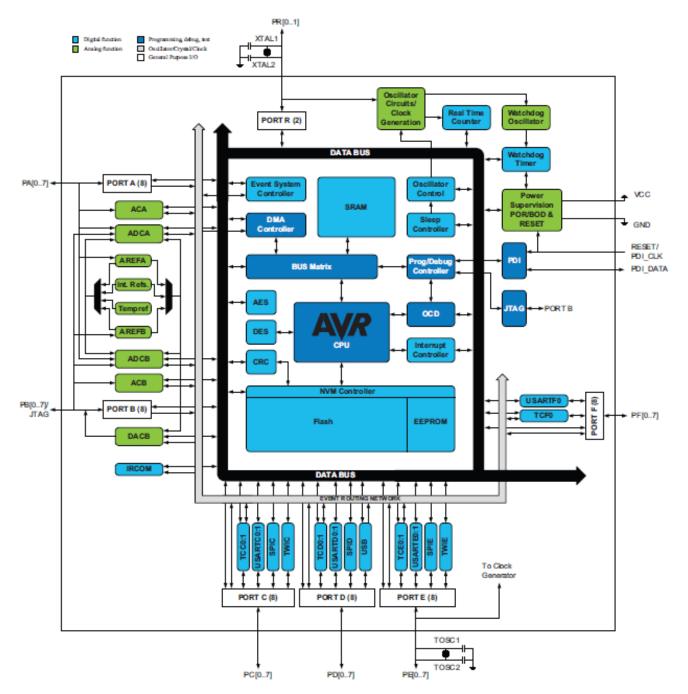


Figure 5 ATXMEGA256A3U Block Diagram

The AVR CPU combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction, executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs many times faster than conventional single-accumulator or CISC based microcontrollers.



The AVR XMEGA A3U devices have five software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, DMA Controller, Event System, Interrupt Controller and all peripherals to continue functioning. The Power-down mode saves the SRAM and register contents but stops the oscillators, disabling all other functions until the next TWI or pin-change interrupt, or Reset. In Power-save mode, the asynchronous Real Time Counter continues to run, allowing the application to maintain a timer base while the rest of the device is sleeping. In Standby mode, the Crystal/Resonator Oscillator is kept running while the rest of the device is sleeping. This allows very fast start-up from external crystal combined with low power consumption. In Extended Standby mode, both the main Oscillator and the Asynchronous Timer continue to run. To further reduce power consumption, the peripheral clock for each individual peripheral can optionally be stopped in Active mode and Idle sleep mode.

Radio

The AT86RF212B is a low-power, low-voltage 800/900 MHz transceiver specially designed for low-cost IEEE 802.15.4, ZigBee[™], and high data rate ISM applications. For the sub-1 GHz bands, it supports a low data rate of 40kbps of the IEEE 802.15.4-2003 standard [2] and provides an optional data rate 250kbps using O-QPSK, according to IEEE 802.15.4-2006. Furthermore hardware accelerators improve overall system power efficiency and timing.

The receiver path is based on a low-IF architecture. After channel filtering and down conversion the low-IF signal is sampled and applied to the digital signal processing part. Communication between transmitter and receiver is based on direct sequence spread spectrum with different modulation schemes and spreading codes. The AT86RF212B supports the IEEE 802.15.4-2006 standard mandatory BPSK modulation and optional O-QPSK modulation in the 800 and 900 MHz band. For applications not necessarily targeting IEEE compliant networks the radio transceiver supports proprietary High Data Rate Modes based on O-QPSK.

The AT86RF212B features hardware supported 128 bit security operation. The standalone AES encryption/decryption engine can be accessed in parallel to all PHY operational modes. Configuration of the AT86RF212B, reading, and writing of data memory as well as the AES hardware engine are controlled by the SPI interface and additional control signals.

The information in this document is subject to change without notice.



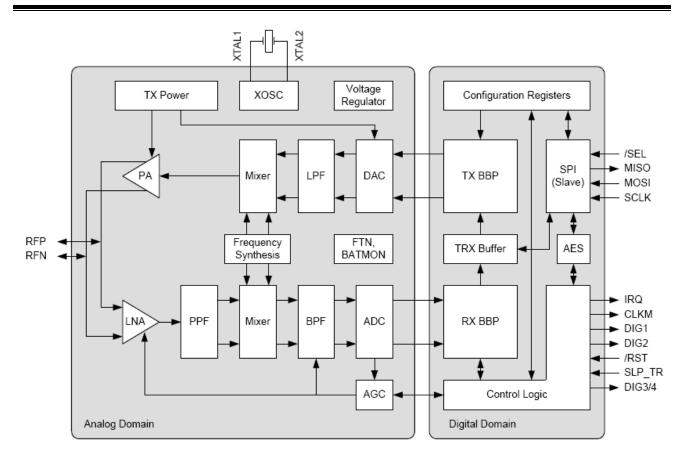


Figure 6 AT86RF212B Block Diagram

RF Power Amplifier

The SiFLEX02-R2 module contains a discrete high performance RF Front End for low-power and low-voltage 900MHz wireless applications. It is capable of 250mW output power, providing miles of range in outdoor applications.

The signals DIG3 and DIG4 from the RF212B radio are used for transmit enable (TXEN) and receive enable (RXEN) respectively. When transmitting the DIG3 signal will be high and DIG4 will be low, which is controlled by the RF212B. When receiving DIG3 will be low and DIG4 is high. In order to configure this functionality, the PA_EXT_EN bit in register TRX_CTRL_1 (0x04) of the RF212B needs to be set as a one. In addition the bits PA_LT[1] and PA_LT[0] in register RF_CTRL_0 (0x16) should both be set to one to maximize the PA lead time to 8usec.

When putting the module to sleep the PA_EXT_EN bit should be set as zero. Upon wakeup the PA_EXT_EN should be set back to one.



Antenna Options

The SiFLEX02-R2 module includes multiple antenna options. The module's regulatory certification has been completed with the following antennas:

- Integrated 3.2-inch wire monopole soldered to the board.
- Pulse W3112A helical antenna
- LSR 001-0002 900 MHz Dipole Antenna with Reverse Polarity SMA Connector and LSR 080-0001 U.FL to Reverse Polarity SMA Bulkhead Cable 105mm
- Nearson S467AH-915 dipole antenna attached to the board via 6-inch cable with connector.

The SiFLEX02-R2 RF castellation for off board antenna is not covered in the modular certification. If a host board is designed that will utilize an off board antenna via the castellated antenna connection an additional certification will be required. LSR is equipped with a certification lab and can assist in getting this done at a very reasonable cost in a short period of time.

An adequate ground plane is necessary to provide good efficiency. The ground plane of the host board on which the module is mounted increases the effective antenna ground plane size and improves the antenna performance.

The environment the module is placed in will dictate the range performance The non-ideal characteristics of the environment will result in the transmitted signal being reflected, diffracted, and scattered. All of these factors randomly combine to create extremely complex scenarios that will affect the link range in various ways.

It is also best to keep some clearance between the antenna and nearby objects. This includes how the module is mounted in the product enclosure. Unless the items on the following list of recommendations are met, the radiation pattern can be heavily distorted.

Whichever antenna is used, it is best to keep a few things in mind when determining its location.

- Never place ground plane or copper trace routing underneath the antenna.
- LSR recommends keeping metal objects as far away from the antenna as possible. At a very minimum keep the antenna at least 5 cm from any metallic objects, components, or wiring. The farther the antenna is placed from these interferers, the less the radiation pattern and gain will be perturbed.
- Do not embed the antenna in a metallic or metalized plastic enclosure.
- If located within a plastic enclosure, keep the enclosure at least 1 cm from the antenna.



MODES OF OPERATION

- With a host microcontroller
- With the Atmel 802.15.4 MAC
- With the Atmel ZigBee stack

Host Microcontroller

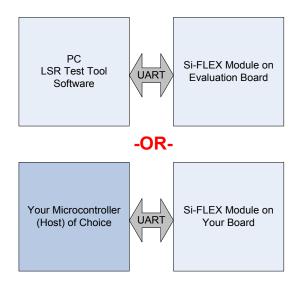


Figure 7 Host Microcontroller Modes of Operation

Out of the box the SiFLEX02-R2 module contains an 802.15.4 based application that uses a host serial processor. This allows features of the module to be explored with the LSR PC based test tool, or controlled with a host microcontroller. The advantage of this method is simplicity; all major features of using the radio are simplified into a simple serial message, taking the burden of becoming a radio expert off the developer.

Use the Communications Log in the ModFLEX[™] Test Tool software and serial host protocol documents to see the messages in action. It will help you become familiar with the serial commands and how to implement them on your own microcontroller.

| Communications Log: | 🔲 Save Log To File | | | | |
|---|--------------------|--|--|--|--|
| | Clear | | | | |
| TXCVR->Host (Query Settings Ack): 01 0E 83 02 00 02 00 01 04 0E 03 F2 9E 04 Host->TXCVR (Query Settings): 01 05 03 09 04 | | | | | |
| Figure 8 ModFLEX™ Test Tool Communications | | | | | |

Log

Some examples of serial commands that can be used with the SiFLEX02-R2 Module:

- Set/Query RF channel
- Set/Query RF power
- Set/Query device address
- Transmit RF data or notification RF data received
- Go to Sleep

Software Stacks

There are two software stacks provided by Atmel to streamline development:

| MAC (802.15.4) | |
|---|--|
| Atmel ZigBee Stack | |
| | |
| Overall Complexity and Development Effort | |
| | |

Figure 9 SiFLEX02-R2 Compatible Stacks

802.15.4 MAC

- Use for applications requiring point-topoint or star network topology.
- Advantages: Quick learning curve, minimize software development, easy to deploy in the field
- Disadvantages: No mesh networking



Distributor of LSR: Excellent Integrated System Limited Datasheet of 450-0123 - MODULE SIFLEX02-R2 U.FL Contact us: sales@integrated-circuit.com Website: www.integrated-circuit.com

SIFLEX02-R2 TRANSCEIVER MODULE DATASHEET

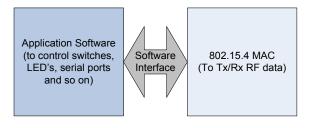


Figure 10 SiFLEX02-R2 with 802.15.4 MAC

Atmel ZigBee Stack

• Use when mesh networking is required.

- Advantages: Covers a large area with a ZigBee network.
- Disadvantages: Large learning curve, more software development, complexity

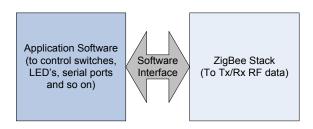


Figure 11 SiFLEX02-R2 with Atmel ZigBee Stack



DEVELOPMENT TOOLS

AVR Studio

AVR Studio[®] is an Integrated Development Environment (IDE) for writing and debugging AVR[®] applications. AVR Studio includes an assembler, simulator, and in-circuit debugger.

AVR Studio is the Integrated Development Environment (IDE) developed by Atmel for writing and debugging Atmel AVR applications.

WinAVR

WinAVR is a suite of executable, open source software development tools for the Atmel AVR series of RISC microprocessors hosted on the Windows platform. It includes the GNU GCC compiler for C/C++.

WinAVR contains all the tools for developing on AVR family microcontrollers from Atmel. This includes avr-gcc (compiler), avrdude (programmer), avr-gdb (debugger), and more.

AVR JTAGICE mkll

Custom firmware development can be done on the SiFLEX02-R2 module using development tools available through Atmel. Shown in Figure 12, a JTAGICE mkII interface is required. It plugs into the ModFLEX[™] Development Board, and can easily be adapted to other hardware. See the Atmel website for more information and ordering options.

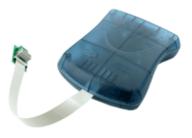


Figure 12 JTAGICE mkll

AVRISP mkll

Another option for in-circuit programming is the AVRISP mkII from Atmel, Figure 13. The AVRISP mkII combined with AVR Studio® can program new AVR 8-bit RISC microcontrollers with ISP Interface.



Figure 13 AVRISP mkll

IAR Embedded Workbench for Atmel AVR

Another option is IAR Embedded Workbench for Atmel AVR. IAR Embedded Workbench for AVR is an integrated development environment for building and debugging embedded applications. Visit the IAR Systems website for additional information.



ELECTRICAL SPECIFICATIONS

The majority of these characteristics are based on the use of the Atmel IEEE 802.15.4 MAC loaded with the generic application firmware written by LSR. Custom firmware may require these values to be re-characterized by the customer.

Absolute Maximum Ratings

| Rating | Min | Мах | Unit |
|---|------|-----------------------|------|
| Power supply voltage | 0 | 3.6 | V |
| Voltage on any pin with respect to ground | -0.3 | V _{CC} + 0.3 | V |
| RF input power | | +10 | dBm |
| Operating temperature range | -40 | +85 | °C |
| Storage temperature | -50 | +150 | °C |

Table 4 Absolute Maximum Ratings¹

Recommended Operating Conditions

| Characteristic | Min | Тур | Мах | Unit |
|---|-----|-----|------|------|
| Power supply voltage (V _{CC}) | 2.0 | 3.3 | 3.45 | Vdc |
| Ambient temperature range | -40 | 25 | 85 | °C |

Table 5 Recommended Operating Conditions

Module will NOT transmit, if $V_{cc} > 3.5V$.

¹ Under no circumstances should exceeding the maximum ratings specified in the Absolute Maximum Ratings section be allowed. Stressing the module beyond these limits may result permanent damage to the module that is not covered by the warranty.

The information in this document is subject to change without notice.



General Characteristics

| Parameter | Min | Тур | Мах | Unit |
|--------------------|-----|------|-------|--------|
| RF frequency range | 906 | | 924 | MHz |
| RF data rate | 40 | | 1000 | kbps |
| Host data rate | 1.2 | 19.2 | 921.6 | kbps |
| Flash memory | | 256 | | kBytes |
| RAM | | 16 | | kBytes |
| EEPROM | | 4 | | kBytes |

Table 6 General Characteristics

Power Consumption

$(T_A = 25^{\circ}C, V_{CC} = 3.3V, fc = 906-924MHz, Rload = 50\Omega)$

| Parameter | Test Conditions | Min | Тур | Мах | Unit |
|---------------|--------------------|-----|-----|-----|------|
| Transmit mode | Maximum power step | 270 | 285 | 300 | mA |
| Receive mode | | 27 | 30 | 33 | mA |
| Sleep mode | | | 2 | 5 | μA |

 Table 7 Power Consumption

DC Characteristics – General Purpose I/O

| Parameter | Test Conditions | Min | Тур | Мах | Unit |
|-------------------|---|-----------------------|-----|-----------------------|------|
| Logic input low | | -0.3 | | 0.2 * V _{CC} | V |
| Logic input high | | 0.8 * V _{CC} | | V _{CC} + 0.3 | V |
| Logic output low | I _{OUT} = 15mA V _{CC} = 3.3V | | 0.4 | | V |
| Logic output high | I _{OUT} = -8mA V _{CC} = 3.3V | | 2.9 | | V |

Table 8 DC Characteristics – General Purpose I/O



RF Characteristics

Transmitter Characteristics $(T_A = 25^{\circ}C, V_{CC} = 3.3V, fc = 906-924 \text{ MHz})$

| Parameter | Test Conditions | Min | Тур | Мах | Unit |
|---------------------------------|-----------------|------|------|-----|----------|
| Nominal max output power | 250mW | 22 | 24.0 | 25 | dBm |
| Programmable output power range | 22 Steps | -6.0 | | 25 | dBm |
| Harmonics (2fo) | | | -34 | | dBm |
| Harmonics (3fo) | | | -38 | | dBm |
| Error vector magnitude | | | 10 | 35 | % rms |

 Table 9 Transmitter RF Characteristics

The information in this document is subject to change without notice.



| Host Protocol | Host Protocol AT86RF212B | | BPSK into 50 ohms at U.FL | | OQPSK into 50 ohms at U.FL | | |
|-------------------|------------------------------|--------------------------|-------------------------------------|--------------------------|-------------------------------------|--|--|
| RF Power Level | PHY_TX_PWR Register Value | RF Output Power (dBm) | Typical Current Consumption (mA) | RF Output Power (dBm) | Typical Current Consumption (mA) | | |
| 21 | 0xE2 | 23.9 | 260 | 24.4 | 285 | | |
| 20 | 0xE3 | 23.8 | 255 | 24.3 | 275 | | |
| 19 | 0x83 | 23.4 | 245 | 24.0 | 270 | | |
| 18 | 0x60 | 23.0 | 235 | 23.5 | 260 | | |
| 17 | 0x61 | 21.8 | 200 | 22.0 | 220 | | |
| 16 | 0x42 | 20.7 | 185 | 20.7 | 195 | | |
| 15 | 0x63 | 20.0 | 175 | 20.0 | 185 | | |
| 14 | 0x22 | 19.5 | 165 | 19.5 | 175 | | |
| 13 | 0x64 | 18.6 | 150 | 18.5 | 160 | | |
| 12 | 0x23 | 17.6 | 140 | 17.5 | 145 | | |
| 11 | 0x45 | 16.2 | 125 | 16.0 | 130 | | |
| 10 | 0x46 | 15.6 | 120 | 15.0 | 120 | | |
| 9 | 0x47 | 14.0 | 105 | 13.0 | 105 | | |
| 8 | 0x04 | 12.0 | 95 | 10.5 | 90 | | |
| 7 | 0x05 | 9.0 | 80 | 8.0 | 80 | | |
| 6 | 0x06 | 7.0 | 75 | 5.0 | 70 | | |
| 5 | 0x07 | 4.5 | 68 | 2.5 | 65 | | |
| 4 | 0x08 | 1.0 | 62 | 0.0 | 61 | | |
| 3 | 0x09 | -1.5 | 59 | -3.0 | 57 | | |
| 2 | 0x0A | -4.0 | 57 | -5.0 | 55 | | |
| 1 | 0x0B | -6.0 | 55 | -7.0 | 54 | | |
| 0 | 0x0C | -8.0 | 54 | -9.0 | 53 | | |

Table 10 RF Power Settings

Receiver Characteristics

$(T_A = 25^{\circ}C, V_{CC} = 3.3V, fc = 906-924 \text{ MHz})$

| Parameter | Test Conditions | Min | Тур | Мах | Unit |
|----------------------------------|-----------------|-----|------|-----|------|
| Receiver Sensitivity @ 1% PER | BPSK 40kbit/s | | -102 | | dBm |
| Saturation Level @ 1% PER | BPSK 40kbit/s | | -2 | | dBm |

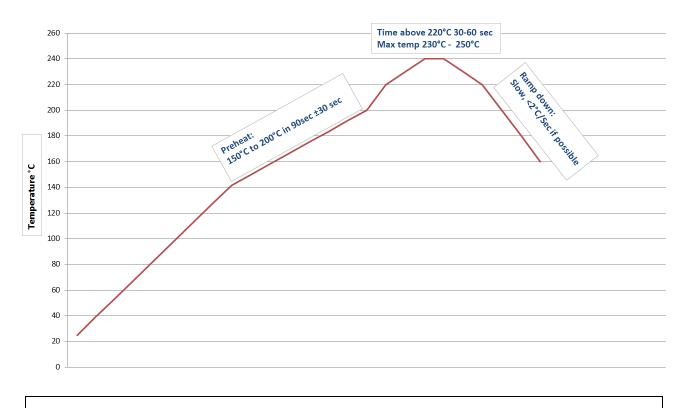
Table 11 Receiver RF Characteristics

For additional details regarding the electrical specifications, refer to the ATXMEGA256A3U and AT86RF212B datasheets on the Atmel website.



SOLDERING RECOMMENDATIONS

Recommended Reflow Profile for Lead Free Solder



Note: The quality of solder joints on the castellations ('half vias') where they contact the host board should meet the appropriate IPC Specification. See IPC-A-610-D Acceptability of Electronic Assemblies, section 8.2.4 Castellated Terminations."



CLEANING

In general, cleaning the populated modules is strongly discouraged. Residuals under the module cannot be easily removed with any cleaning process.

- Cleaning with water can lead to capillary effects where water is absorbed into the gap between the host board and the module. The combination of soldering flux residuals and encapsulated water could lead to short circuits between neighboring pads. Water could also damage any stickers or labels.
- Cleaning with alcohol or a similar organic solvent will likely flood soldering flux residuals into the RF shield, which is not accessible for post-washing inspection. The solvent could also damage any stickers or labels.
- Ultrasonic cleaning could damage the module permanently.

OPTICAL INSPECTION

After soldering the Module to the host board, consider optical inspection to check the following:

- Proper alignment and centering of the module over the pads.
- Proper solder joints on all pads.
- Excessive solder or contacts to neighboring pads, or vias.

REWORK

The module can be unsoldered from the host board if the Moisture Sensitivity Level (MSL) requirements are met as described in this datasheet.

Never attempt a rework on the module itself, e.g. replacing individual components. Such actions will terminate warranty coverage.

SHIPPING, HANDLING, AND STORAGE

Shipping

Bulk orders of the SiFLEX02-R2 modules are delivered in trays of 25.

Handling

The SiFLEX02-R2 modules contain a highly sensitive electronic circuitry. Handling without proper ESD protection may damage the module permanently.

Moisture Sensitivity Level (MSL)

Per J-STD-020, devices rated as MSL 4 and not stored in a sealed bag with desiccant pack should be baked prior to use.

Devices are packaged in a Moisture Barrier Bag with a desiccant pack and Humidity Indicator Card (HIC). Devices that will be subjected to reflow should reference the HIC and J-STD-033 to determine if baking is required.

If baking is required, refer to J-STD-033 for bake procedure.

Storage

Per J-STD-033, the shelf life of devices in a Moisture Barrier Bag is 12 months at <40°C and <90% room humidity (RH).

Do not store in salty air or in an environment with a high concentration of corrosive gas, such as Cl2, H2S, NH3, SO2, or NOX.

Do not store in direct sunlight.

The product should not be subject to excessive mechanical shock.



Repeating Reflow Soldering

Only a single reflow soldering process is encouraged for host boards.



AGENCY STATEMENTS

Federal Communication Commission Interference Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

<u>FCC CAUTION</u>: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

The information in this document is subject to change without notice.



Industry Canada Statements

Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that permitted for successful communication.

This device has been designed to operate with the antennas listed below, and having a maximum gain of 2.0 dB. Antennas not included in this list or having a gain greater than 2.0 dB are strictly prohibited for use with this device. The required antenna impedance is 50 ohms.

Wire Monopole – 3.2 inch, 22 AWG solid copper wire, pvc insulated

External Dipole – LSR 001-0002 900 MHz Dipole Antenna with Reverse Polarity SMA Connector and LSR 080-0001 U.FL to Reverse Polarity SMA Cable (105mm in length)

External Dipole – Nearson S467AH-915, RP-SMA on 6" cable

On Board Chip Helical – Pulse Engineering W3112A

The information in this document is subject to change without notice.



OEM Responsibilities to comply with FCC and Industry Canada Regulations

The SiFLEX02 Module has been certified for integration into products only by OEM integrators under the following conditions:

This device is granted for use in Mobile only configurations in which the antennas used for this transmitter must be installed to provide a separation distance of at least 20cm from all person and not be co-located with any other transmitters except in accordance with FCC and Industry Canada multi-transmitter product procedures.

As long as the two conditions above are met, further transmitter testing will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

IMPORTANT NOTE: In the event that these conditions cannot be met (for certain configurations or co-location with another transmitter), then the FCC and Industry Canada authorizations are no longer considered valid and the FCC ID and IC Certification Number cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC and Industry Canada authorization.

The information in this document is subject to change without notice.



End Product Labelling

The SiFLEX02 Module is labeled with its own FCC ID and IC Certification Number. If the FCC ID and IC Certification Number are not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. In that case, the final end product must be labeled in a visible area with the following:

"Contains Transmitter Module FCC ID: TFB-SIFLEX2"

"Contains Transmitter Module IC: 5969A-SIFLEX2"

or

"Contains FCC ID: TFB-SIFLEX2"

"Contains IC: 5969A-SIFLEX2"

The OEM of the SiFLEX02 Module must only use the approved antenna(s) listed above, which have been certified with this module.

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module or change RF related parameters in the user manual of the end product.

The user manual for the end product must include the following information in a prominent location:

This device is granted for use in Mobile only configurations in which the antennas used for this transmitter must be installed to provide a separation distance of at least 20cm from all person and not be co-located with any other transmitters except in accordance with FCC and Industry Canada multi-transmitter product procedures.

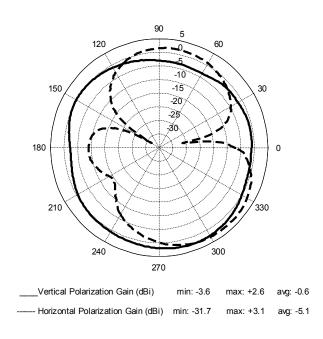
The information in this document is subject to change without notice.



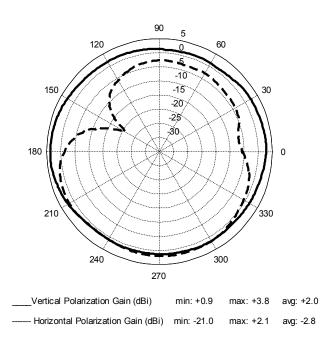
ANTENNA INFORMATION

Wire Antenna (Perpendicular to Board as in Figure 16)

Unit Flat - 914 MHz



Unit Vertical - 914 MHz

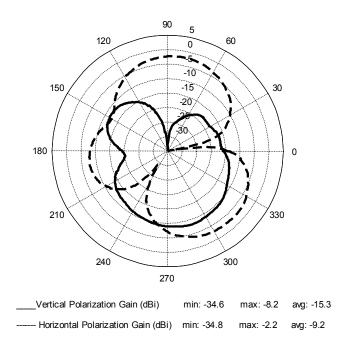




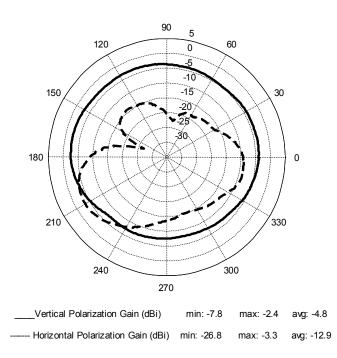


Helical Antenna

Unit Flat - 914 MHz



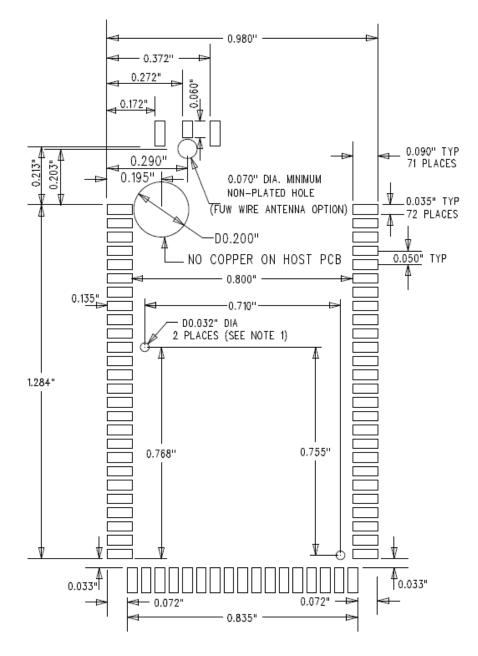
Unit Vertical - 914 MHz





MECHANICAL DATA

PCB Footprint



Notes:

1) Optional alignment holes are for use with fixture placement and hand soldering operations.

2) See http://wiki.lsr.com for additional information.





General Module Dimensions

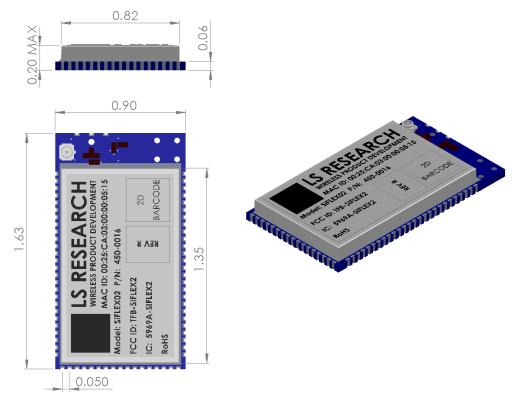


Figure 15 Basic dimensions





Module with Wire Antenna

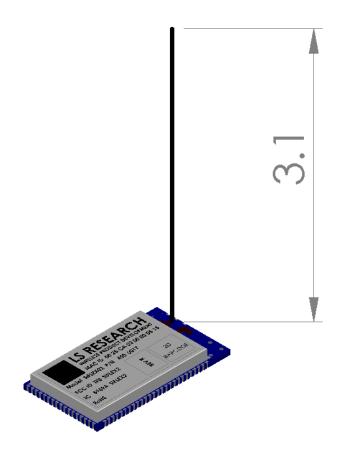


Figure 16 SiFLEX02-R2 with wire antenna



Module with Helical Antenna

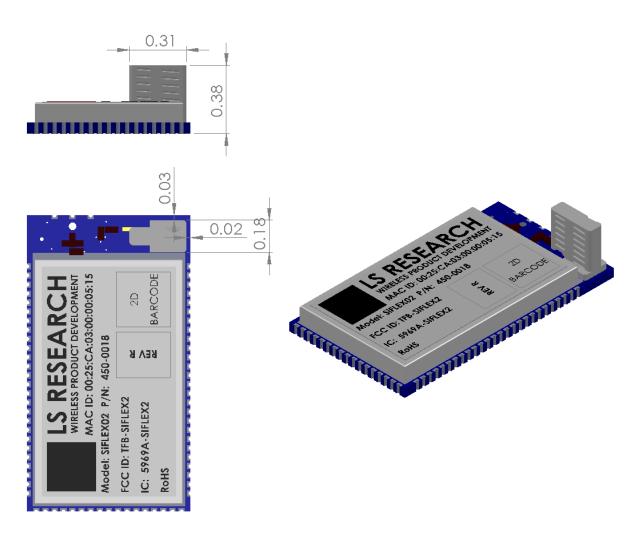


Figure 17 SiFLEX02-R2 with helical antenna



COMPATIBILITY

To maintain compatibility with other ModFLEX[™] family transceiver modules it is important to use the module pins in your application as they are designated in Figure 18. Since the available GPIO and peripherals vary per micro, not all pins may be populated. For example on SiFLEX02-R2 module pins 45-55 are not available (due to the number of GPIO available on the ATxMega256A3U).

All attempts are made to lay out modules starting with the lowest number in the peripheral (ADC, TMR/PWM, GPIO) series. For example if there are only two ADC's available they will be brought out to ADC1 and ADC2 (module pins 20 and 21).

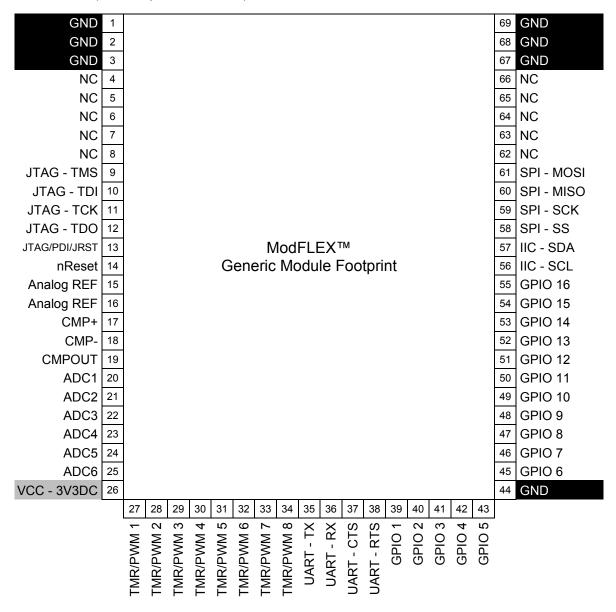


Figure 18 ModFLEX™ Generic Module Footprint

The information in this document is subject to change without notice.





MODULE REVISION HISTORY

Rev 1.0

• Initial production release.

Part Number: 450-0123 U.FL Module



00:25:CA:03:XX:XX:XX = MAC ID 2D Barcode Format is Data Matrix Standard XX:XX:XX:XX = unique portion of MAC ID that changes for each module Part Number: 450-0124 Wire Module



00:25:CA:03:XX:XX:XX = MAC ID 2D Barcode Format is Data Matrix Standard XX:XX:XX:XX = unique portion of MAC ID that changes for each module

Part Number: 450-0125 Helical Module



00:25:CA:03:XX:XX:XX = MAC ID 2D Barcode Format is Data Matrix Standard XX:XX:XX:XX = unique portion of MAC ID that changes for each module Part Number: 450-0126 RF Castellation Module



00:25:CA:03:XX:XX:XX = MAC ID 2D Barcode Format is Data Matrix Standard XX:XX:XX:XX = unique portion of MAC ID that changes for each module



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