OPA355-Q1 200-MHz CMOS Operational Amplifier With Shutdown

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- Unity-Gain Bandwidth: 450 MHz
- Wide Bandwidth: 200 MHz GBW
- High Slew Rate: 360 V/µs
- Low Noise: 5.8 nV/$\sqrt{Hz}$
- Excellent Video Performance:
  - Differential Gain: 0.02%
  - Differential Phase: 0.05° 0.1 dB
  - Gain Flatness: 75 MHz
- Input Range Includes Ground
- Rail-to-Rail Output (within 100 mV)
- Low Input Bias Current: 3 pA
- Low Shutdown Current: 3.4 µA
- Enable and Disable Time: 100 ns and 30 ns
- Thermal Shutdown
- Single-Supply Operating Range: 2.5 to 5.5 V
- *Micro*SIZE Packages

2 Applications

- Automotive
- Active Filters
- High-Speed Integrators
- Analog-to-Digital Converter (ADC) Input Buffers
- Digital-to-Analog Converter (DAC) Output Amplifiers

3 Description

The OPA355-Q1 device is a high-speed, voltage-feedback CMOS operational amplifier designed for applications requiring wide bandwidth. The OPA355-Q1 device is unity-gain stable and can drive large output currents. In addition, the OPA355-Q1 device has a digital shutdown (enable) function. This feature provides power saving during idle periods and places the output in a high-impedance state to support output multiplexing. The differential gain is 0.02% and the differential phase is 0.05°. The quiescent current is 8.3 mA per channel.

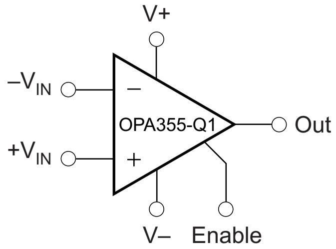
The OPA355-Q1 device is optimized for operation on single supply or dual supplies as low as 2.5 V (±1.25 V) and up to 5.5 V (±2.75 V). The common-mode input range for the OPA355-Q1 device extends 100 mV below ground and up to 1.5 V from V+. The output swing is within 100 mV of the rails, supporting wide dynamic range.

The OPA355-Q1 device is available in a single SOT23-6 package and is specified over the extended –40°C to 125°C range.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA355-Q1	SOT-23 (6)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



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4 Revision History

Changes from Revision A (December 2013) to Revision B — **Page**

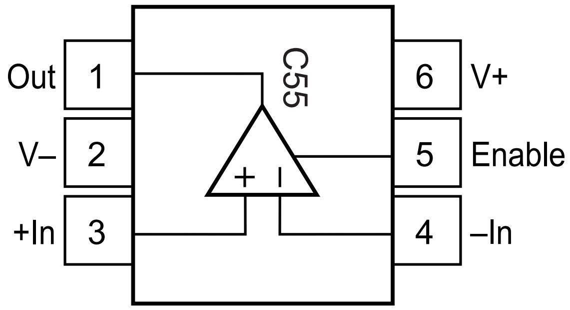
- Changed device status from *Product Preview* to *Production Data* 1

5 Device Comparison Table

OPA355-Q1 RELATED PRODUCTS	FEATURES
OPA356	200-MHz, Rail-to-Rail Output, CMOS, No Shutdown
OPAx350	38-MHz, Rail-to-Rail Input and Output, CMOS
OPAx631	75-MHz, Rail-to-Rail Output
OPAx634	150-MHz, Rail-to-Rail Output
THS412x	Differential Input and Output, 3.3-V Supply

6 Pin Configuration and Functions

6-Pin SOT-23
DBV Package
Top View



(1) Pin 1 of the SOT23-6 is determined by orienting the package marking as indicated in the diagram.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	V+ to V–		7.5	V
Signal input terminals	Voltage	(V–) – 0.5	(V+) + 0.5	V
	Current		10	mA
Output short circuit(2)		Continuous		
Operating temperature		–55	150	°C
Junction Temperature			160	°C
Lead temperature (soldering, 10 seconds)			300	°C

(1) Stresses above *absolute maximum ratings* may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Short-circuit to ground, one amplifier per package.

7.2 Handling Ratings

				MIN	MAX	UNIT
T_{stg}	Storage temperature range			–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)			2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 3, 4, and 6)		750	
			Other pins		500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Thermal Information

THERMAL METRIC(1)		DBV 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	187.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	126.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	24.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	32.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.4 Electrical Characteristics

V_S = 2.7 V to 5.5 V single supply. At T_A = 25°C, R_F = 604 Ω, R_L = 150Ω, and connected to V_S / 2, unless otherwise noted.

PARAMETER			TEST CONDITIONS	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	T_A = –40°C to 125°C MIN	T_A = –40°C to 125°C TYP	T_A = –40°C to 125°C MAX	UNIT
OFFSET VOLTAGE										
V_{OS}	Input offset voltage		V_S = 5 V		±2	±9			±15	mV
DV_{OS}/dT	Input offset voltage versus temperature							±7		**µV/°C**
PSRR	Input offset voltage versus power supply		V_S = 2.7 to 5.5 V, V_{CM} = V_S / 2 – 0.15 V		±80	±350				µV/V
INPUT BIAS CURRENT										
I_B	Input bias current				3	±50				pA
I_{OS}	Input offset current				±1	±50				pA
NOISE										
e_n	Input noise voltage density		f = 1 MHz		5.8					nV/√Hz
i_n	Current noise density		f = 1 MHz		50					fA/√Hz
INPUT VOLTAGE RANGE										
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) – 1.5				V
CMRR	Common-mode rejection ratio		V_S = 5.5 V, –0.1 V < V_{CM} < 4 V	66	80		66			dB
INPUT IMPEDANCE										
	Differential				10^{13} || 1.5					Ω || pF
	Common-mode				10^{13} || 1.5					Ω || pF
OPEN-LOOP GAIN										
	Open-loop gain		V_S = 5 V, 0.3 V < V_O < 4.7 V	84	92		80			dB
FREQUENCY RESPONSE										
f_{-3dB}	Small-signal bandwidth		G = 1, V_O = 100 mVp-p, R_F = 0 Ω		450					MHz
			G = 2, V_O = 100 mVp-p, R_L = 50 Ω		100					MHz
			G = 2, V_O = 100 mVp-p, R_L = 150 Ω		170					MHz
			G = 2, V_O = 100 mVp-p, R_L = 1 kΩ		200					MHz
GBW	Gain-bandwidth product		G = 10, R_L = 1 kΩ		200					MHz
$f_{0.1dB}$	Bandwidth for 0.1-db gain flatness		G = 2, V_O = 100 mVp-p, R_F = 560 Ω		75					MHz
SR	Slew rate		V_S = 5 V, G = 2, 4-V output step		300 / –360					V/µs
	Rise and fall time		G = 2, V_O = 200 mVp-p, 10% to 90%		2.4					ns
			G = 2, V_O = 2 Vp-p, 10% to 90%		8					ns
	Settling time	0.1%	V_S = 5 V, G = 2, 2-V output step		30					ns
		0.01%	V_S = 5 V, G = 2, 2-V output step		120					ns
	Overload recovery time		V_I × G = V_S		8					ns
	Harmonic distortion	Second harmonic	G = 2, f = 1 MHz, V_O = 2 Vp-p, R_L = 200 Ω		–81					dBc
		Third harmonic	G = 2, f = 1 MHz, V_O = 2 Vp-p, R_L = 200 Ω		–93					dBc
	Differential gain error		NTSC, R_L = 150 Ω		0.02%					
	Differential phase error		NTSC, R_L = 150 Ω		0.05					degrees (°)

Electrical Characteristics (continued)

V_S = 2.7 V to 5.5 V single supply. At T_A = 25°C, R_F = 604 Ω, R_L = 150Ω, and connected to V_S / 2, unless otherwise noted.

PARAMETER			TEST CONDITIONS	T_A = 25°C			T_A = –40°C to 125°C			
				MIN	TYP	MAX	MIN	TYP	MAX	UNIT
OUTPUT										
	Voltage output swing from rail		V_S = 5 V, R_L = 150 Ω, A_{OL} > 84 dB		0.2	0.3				V
			V_S = 5 V, R_L = 1 kΩ		0.1					V
I_O	Output current(1)	Continuous			±60					mA
		Peak	V_S = 5 V		±100					mA
			V_S = 3 V		±80					mA
	Closed-loop output impedance		f < 100 kHz		0.02					Ω
POWER SUPPLY										
V_S	Specified voltage range			2.7		5.5				V
	Operating voltage range				2.5 to 5.5					V
I_Q	Quiescent current (per amplifier)		V_S = 5 V, enabled; I_O = 0		8.3	11			14	mA
SHUTDOWN										
	Disabled	Logic-LOW threshold(2)				0.8				V
	Enabled	Logic-HIGH threshold(2)		2						V
	Enable time				100					ns
	Disable time				30					ns
	Shutdown current (per amplifier)		V_S = 5 V, disabled		3.4					µA
THERMAL SHUTDOWN										
	Junction Temperature	Shutdown			160					°C
		Reset from Shutdown			140					°C
TEMPERATURE RANGE										
	Specified Range			–40		125				°C
	Operating Range			–55		150				°C
	Storage Range			–65		150				°C

(1) See the *Output Voltage Swing vs Output Current* (Figure 21 and Figure 23) in the *Typical Characteristics* section.
(2) Logic LOW and HIGH levels are CMOS logic compatible. They are referenced to V–.

7.5 Typical Characteristics

At T_A = 25°C, V_S = 5 V, G = 2, R_F = 604 Ω, and R_L = 150 Ω connected to V_S / 2, unless otherwise noted.

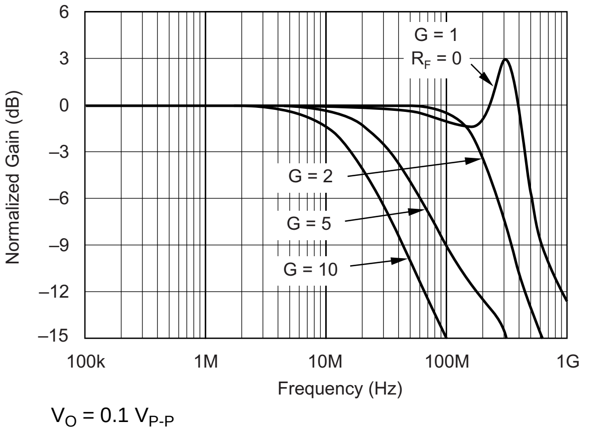


Figure 1. Non-Inverting Small-Signal Frequency Response

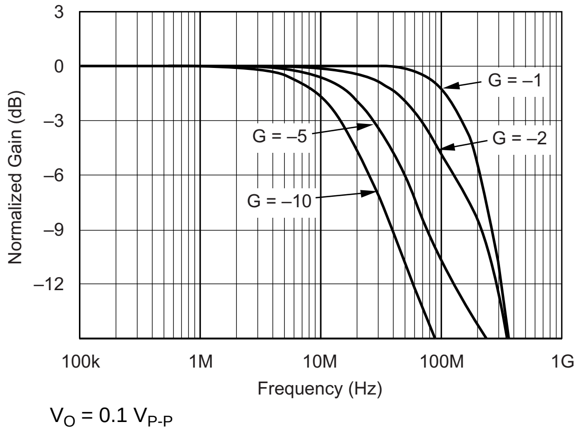


Figure 2. Inverting Small-Signal Frequency Response

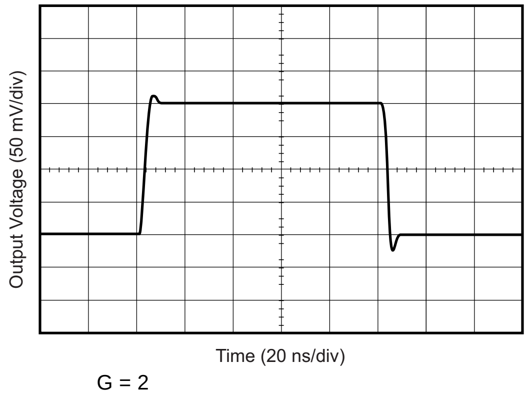


Figure 3. Non-Inverting Small-Signal Step Response

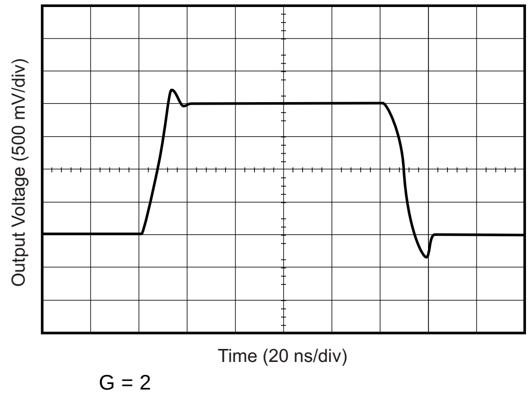


Figure 4. Non-Inverting Large-Signal Step Response

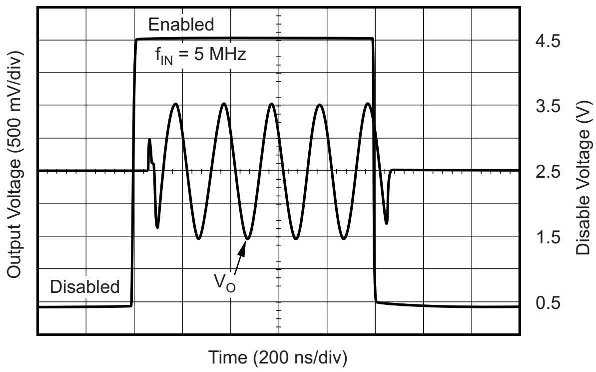


Figure 5. Large-Signal Disable and Enable Response

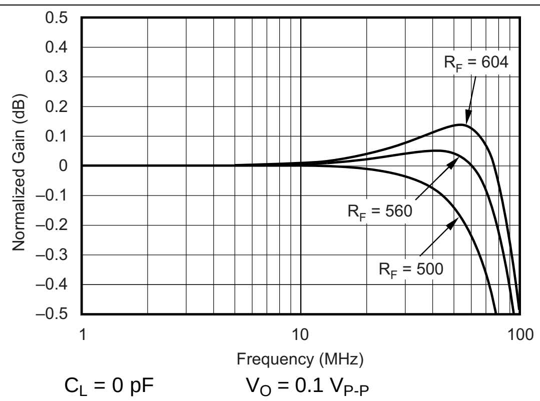


Figure 6. 0.1 dB Gain Flatness for Various R_F

Typical Characteristics (continued)

At T_A = 25°C, V_S = 5 V, G = 2, R_F = 604 Ω, and R_L = 150 Ω connected to V_S / 2, unless otherwise noted.

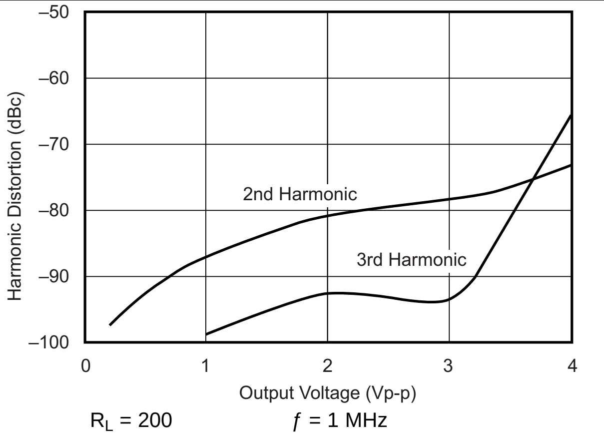


Figure 7. Harmonic Distortion vs Output Voltage

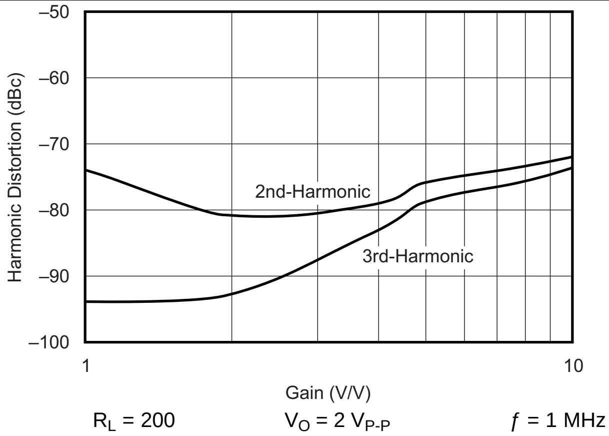


Figure 8. Harmonic Distortion vs Non-Inverting Gain

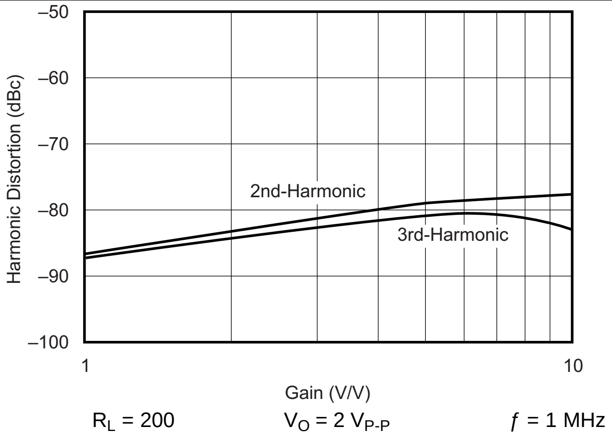


Figure 9. Harmonic Distortion vs Inverting Gain

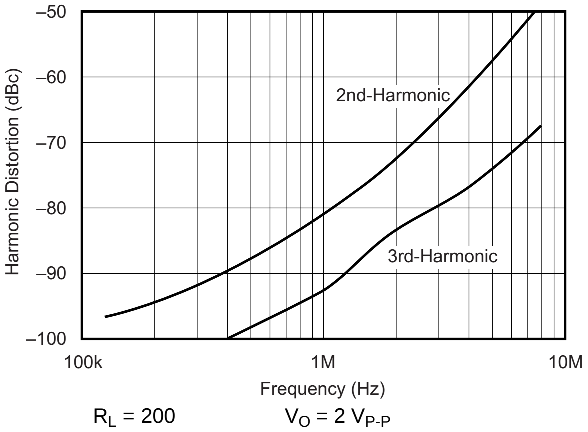


Figure 10. Harmonic Distortion vs Frequency

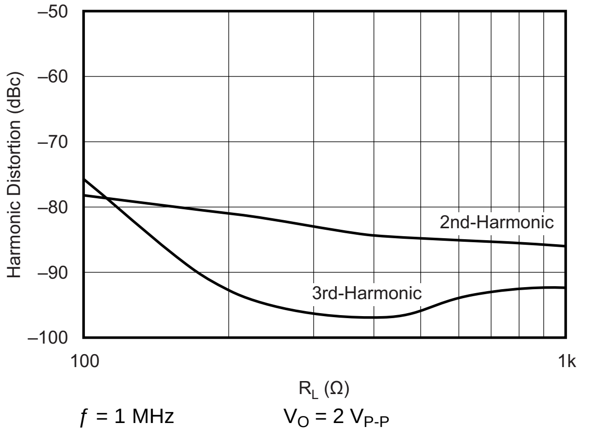


Figure 11. Harmonic Distortion vs Load Resistance

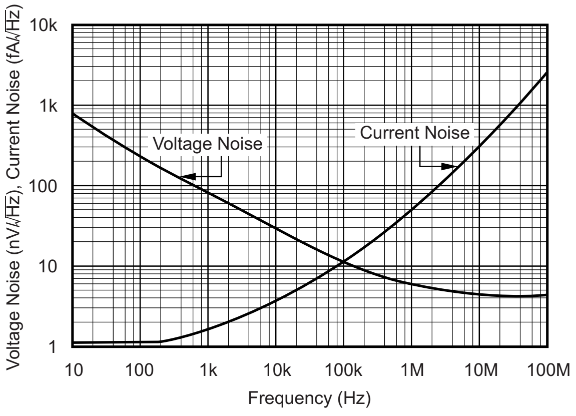


Figure 12. Input Voltage and Current Noise Spectral Density vs Frequency

Typical Characteristics (continued)

At T_A = 25°C, V_S = 5 V, G = 2, R_F = 604 Ω, and R_L = 150 Ω connected to V_S / 2, unless otherwise noted.

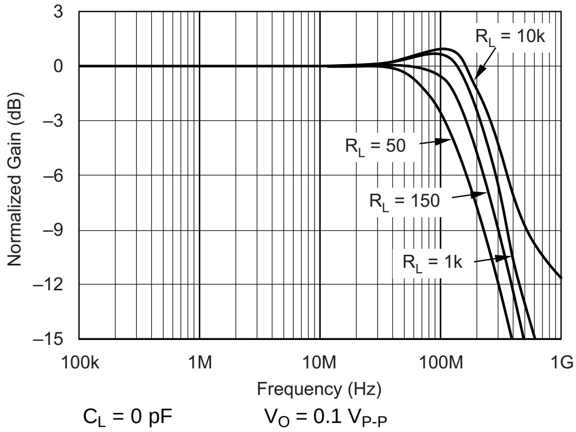


Figure 13. Frequency Response for Various R_L

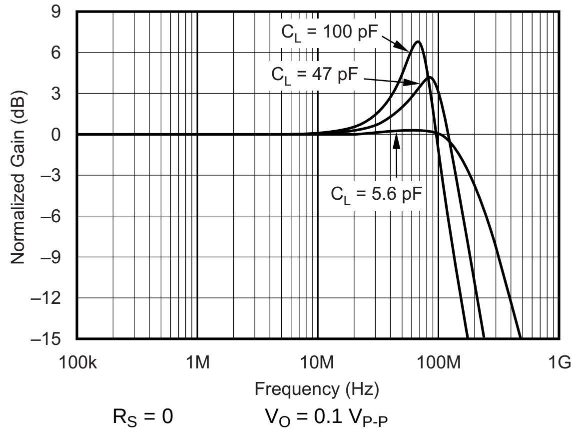


Figure 14. Frequency Response for Various C_L

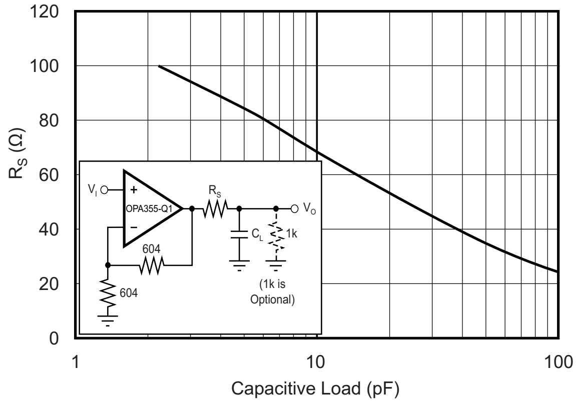


Figure 15. Recommended R_S vs Capacitive Load

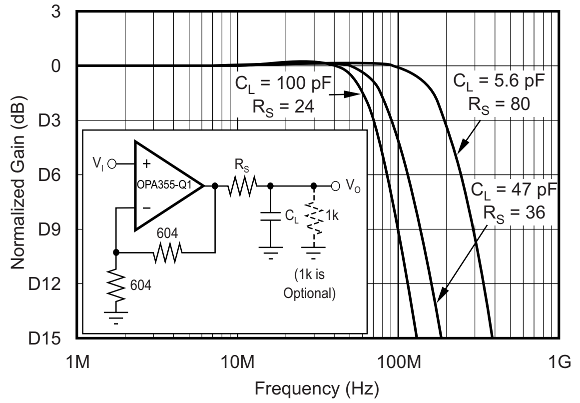


Figure 16. Frequency Response vs Capacitive Load

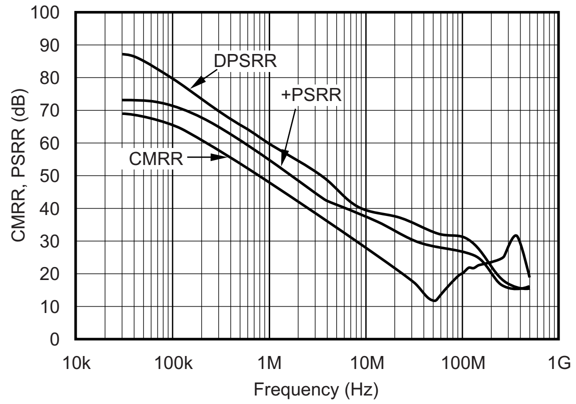


Figure 17. Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Frequency

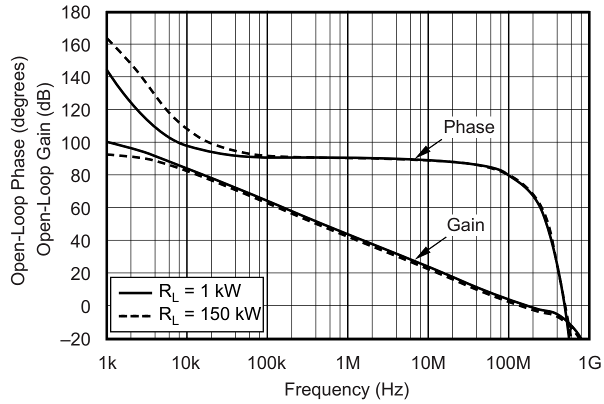


Figure 18. Open-Loop Gain and Phase

Typical Characteristics (continued)

At T_A = 25°C, V_S = 5 V, G = 2, R_F = 604 Ω, and R_L = 150 Ω connected to V_S / 2, unless otherwise noted.

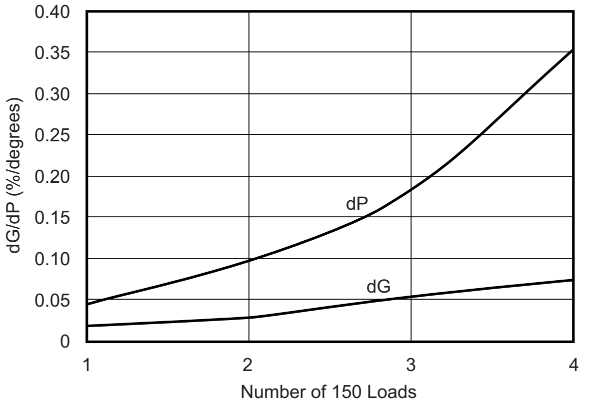


Figure 19. Composite Video Differential Gain and Phase

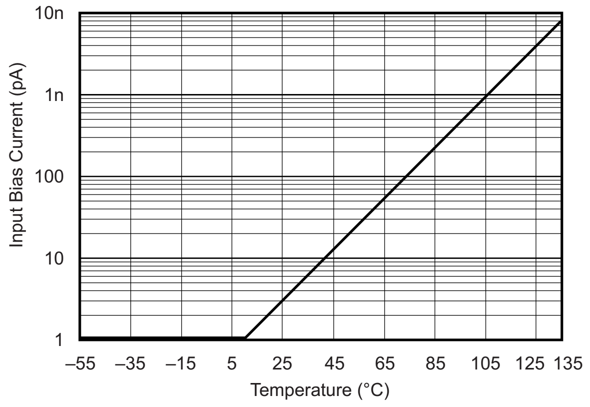


Figure 20. Input Bias Current vs Temperature

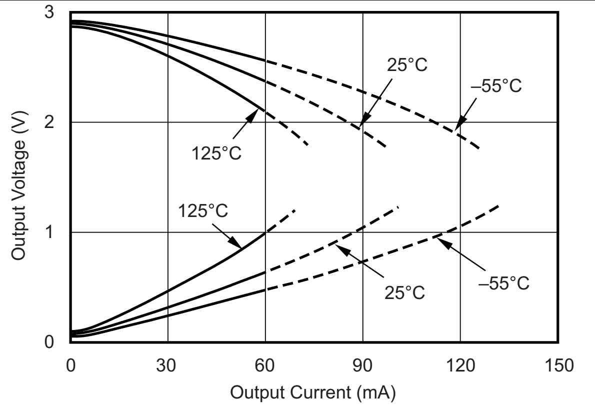


Figure 21. Output Voltage Swing vs Output Current for V_S = 3 V

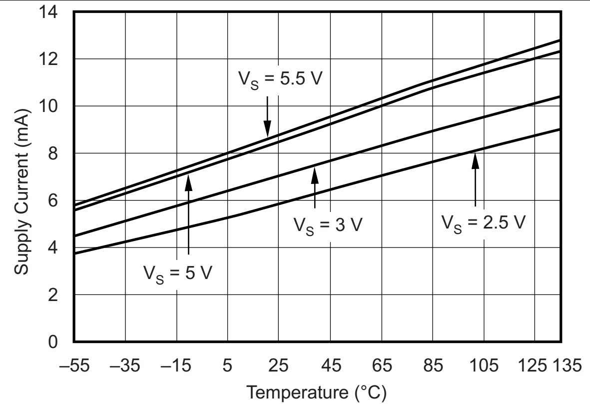


Figure 22. Supply Current vs Temperature

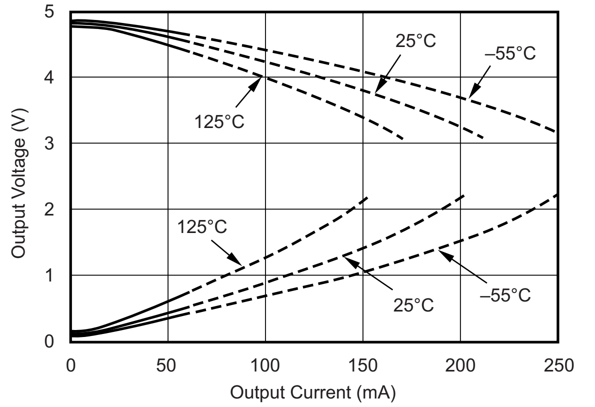


Figure 23. Output Voltage Swing vs Output Current for V_S = 5 V

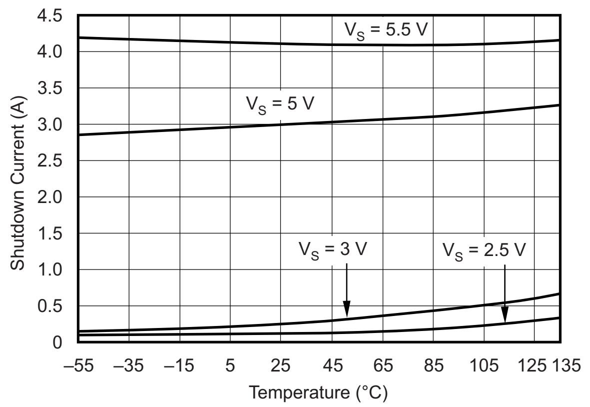


Figure 24. Shutdown Current vs Temperature

Typical Characteristics (continued)

At T_A = 25°C, V_S = 5 V, G = 2, R_F = 604 Ω, and R_L = 150 Ω connected to V_S / 2, unless otherwise noted.

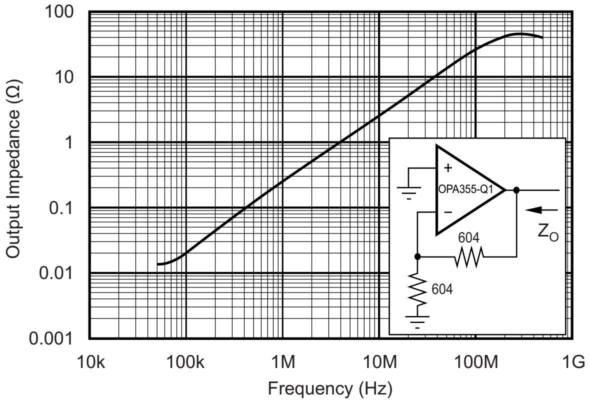
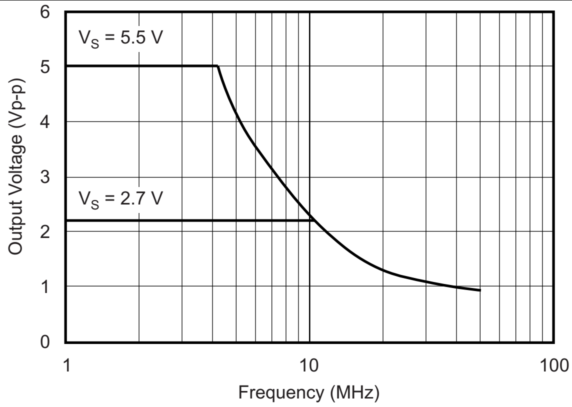
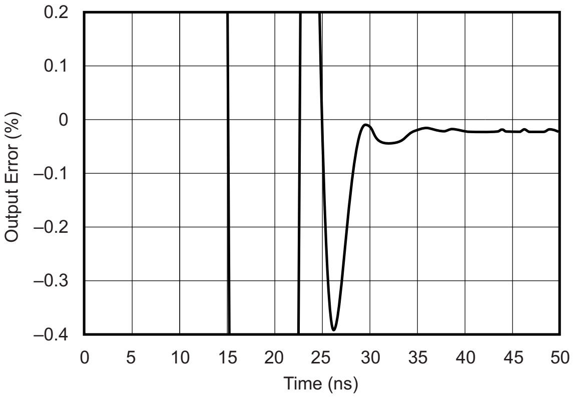


Figure 25. Closed-Loop Output Impedance vs Frequency



Maximum output voltage without slew-rate induced distortion

Figure 26. Maximum Output Voltage vs Frequency



V_O = 2 V_{P-P}

Figure 27. Output Settling Time to 0.1%

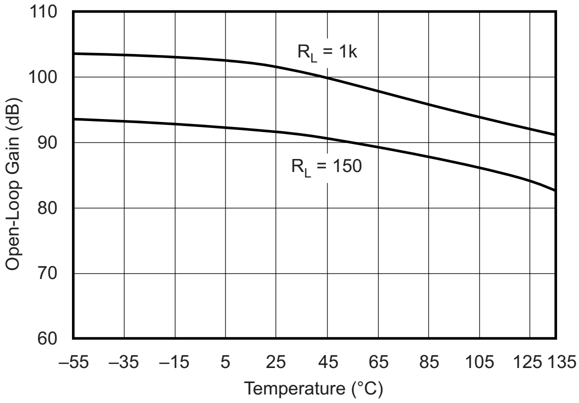


Figure 28. Open-Loop Gain vs Temperature

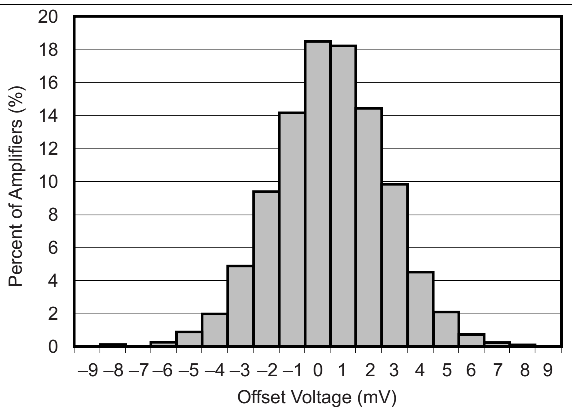


Figure 29. Offset Voltage Production Distribution

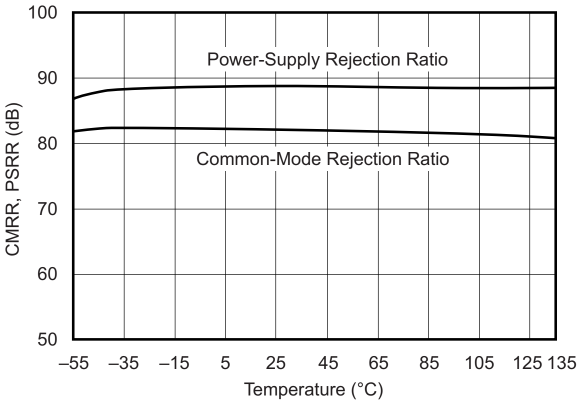


Figure 30. Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Temperature

8 Detailed Description

8.1 Feature Description

8.1.1 Operating Voltage

The OPA355-Q1 device is specified over a power-supply range of 2.7 to 5.5 V (±1.35 to ±2.75 V). However, the supply voltage can range from 2.5 to 5.5 V (±1.25 to ±2.75 V). Supply voltages higher than 7.5 V (absolute maximum) can permanently damage the amplifier.

Parameters that vary significantly over supply voltage or temperature are shown in the Typical Characteristics section of this data sheet.

8.1.2 Enable Function

The OPA355-Q1 device is enabled by applying a TTL HIGH-voltage level to the Enable pin. Conversely, a TTL LOW-voltage level disables the amplifier which reduces the supply current from 8.3 mA to only 3.4 µA per amplifier. This pin voltage is referenced to a single-supply ground. When using a split-supply, such as ±2.5 V, the enable and disable voltage levels are referenced to V–. Independent Enable pins are available for each channel, providing maximum design flexibility. For portable battery-operated applications, this feature can be used to greatly reduce the average current and thereby extend battery life.

The Enable input can be modeled as a CMOS input gate with a 100-kΩ pullup resistor to V+. Left open, the Enable pin assumes a logic HIGH, and the amplifier turns on.

The Enable time is 100 ns and the disable time is 30 ns which allows the OPA355-Q1 device to operate as a *gated* amplifier, or to have the output multiplexed onto a common output bus. When disabled, the output assumes a high-impedance state.

8.1.3 Output Drive

The output stage supplies a high short-circuit current (typically over 200 mA). Therefore, an on-chip thermal shutdown circuit is provided to protect the OPA355-Q1 device from dangerously-high junction temperatures. At 160°C, the protection circuit shuts down the amplifier. Normal operation resumes when the junction temperature cools to below 140°C.

NOTE

Running a continuous DC current in excess of ±60 mA is not recommended. Refer to the *Output Voltage Swing vs Output Current* graphs (Figure 21 and Figure 22) in the Typical Characteristics section.

8.1.4 Input and ESD Protection

All OPA355-Q1 pins are static protected with internal ESD protection diodes tied to the supplies (see Figure 31).

If the current is externally limited to 10 mA by the source or by a resistor, these diodes provide overdrive protection.

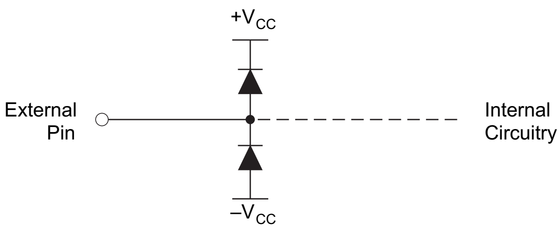


Figure 31. Internal ESD Protection

9 Application and Implementation

9.1 Application Information

The OPA355-Q1 device is a CMOS, high-speed, voltage-feedback, operational amplifier (op-amp) designed for general-purpose applications.

The amplifier features a 200-MHz gain bandwidth and 360-V/µs slew rate, but the device is unity-gain stable and can operate as a 1-V/V voltage follower.

The input common-mode voltage range of the device includes ground which allows the OPA355-Q1 to be used in virtually any single-supply application up to a supply voltage of +5.5 V.

10 Layout

10.1 Layout Guidelines

Good high-frequency printed-circuit board (PCB) layout techniques must be used for the OPA355-Q1. Generous use of ground planes, short direct-signal traces, and a suitable bypass capacitor located at the V+ pin will assure clean and stable operation. Large areas of copper also help dissipate heat generated within the amplifier in normal operation.

Sockets are not recommended for use with any high-speed amplifier.

A 10-nF ceramic bypass capacitor is the minimum recommended value; adding a 1-µF or larger tantalum capacitor in parallel can be beneficial when driving a low-resistance load. Providing adequate bypass capacitance is essential to achieving very low harmonic and intermodulation distortion.

11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA355QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SLN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

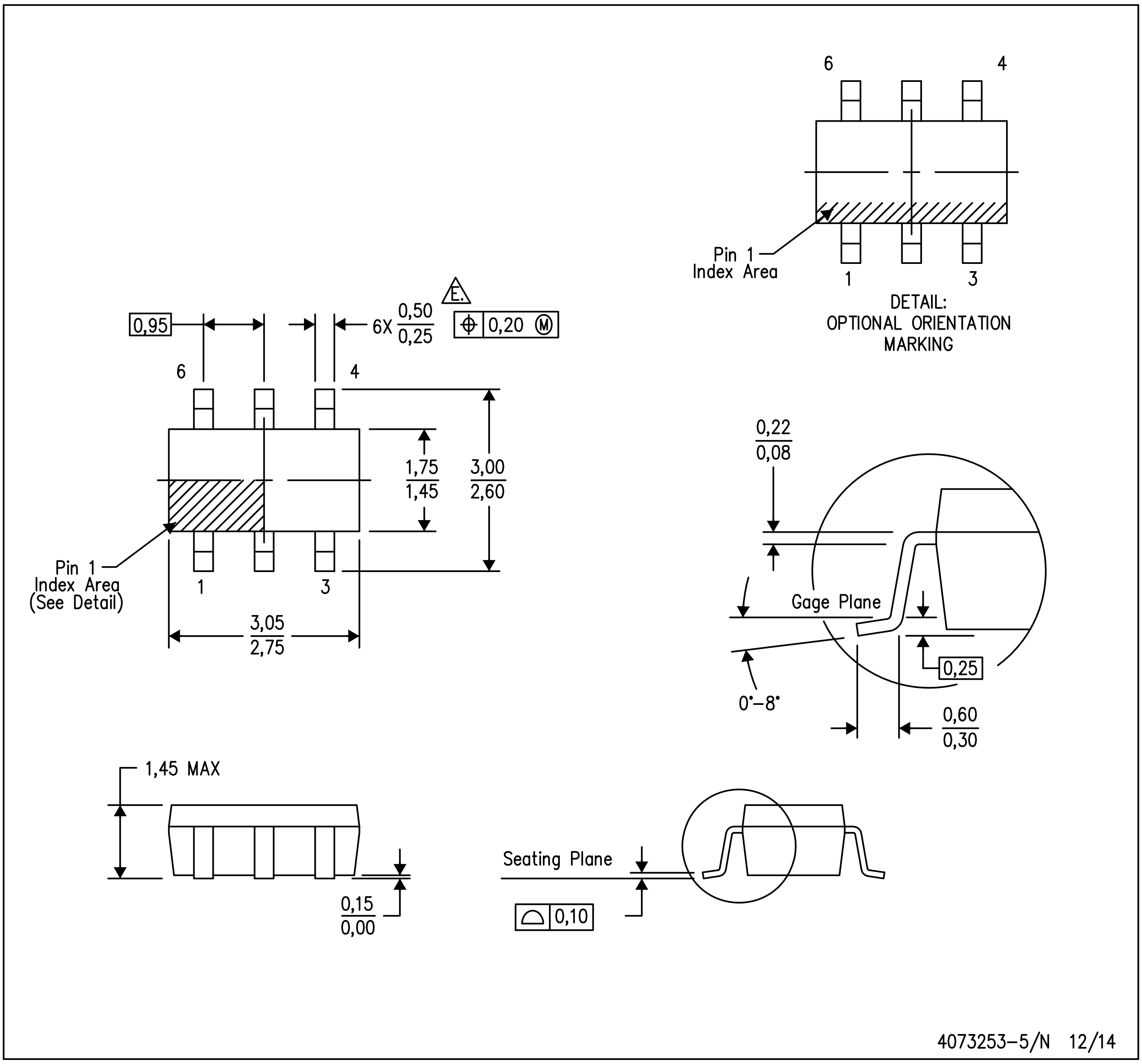
OTHER QUALIFIED VERSIONS OF OPA355-Q1 :

- Catalog: OPA355

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

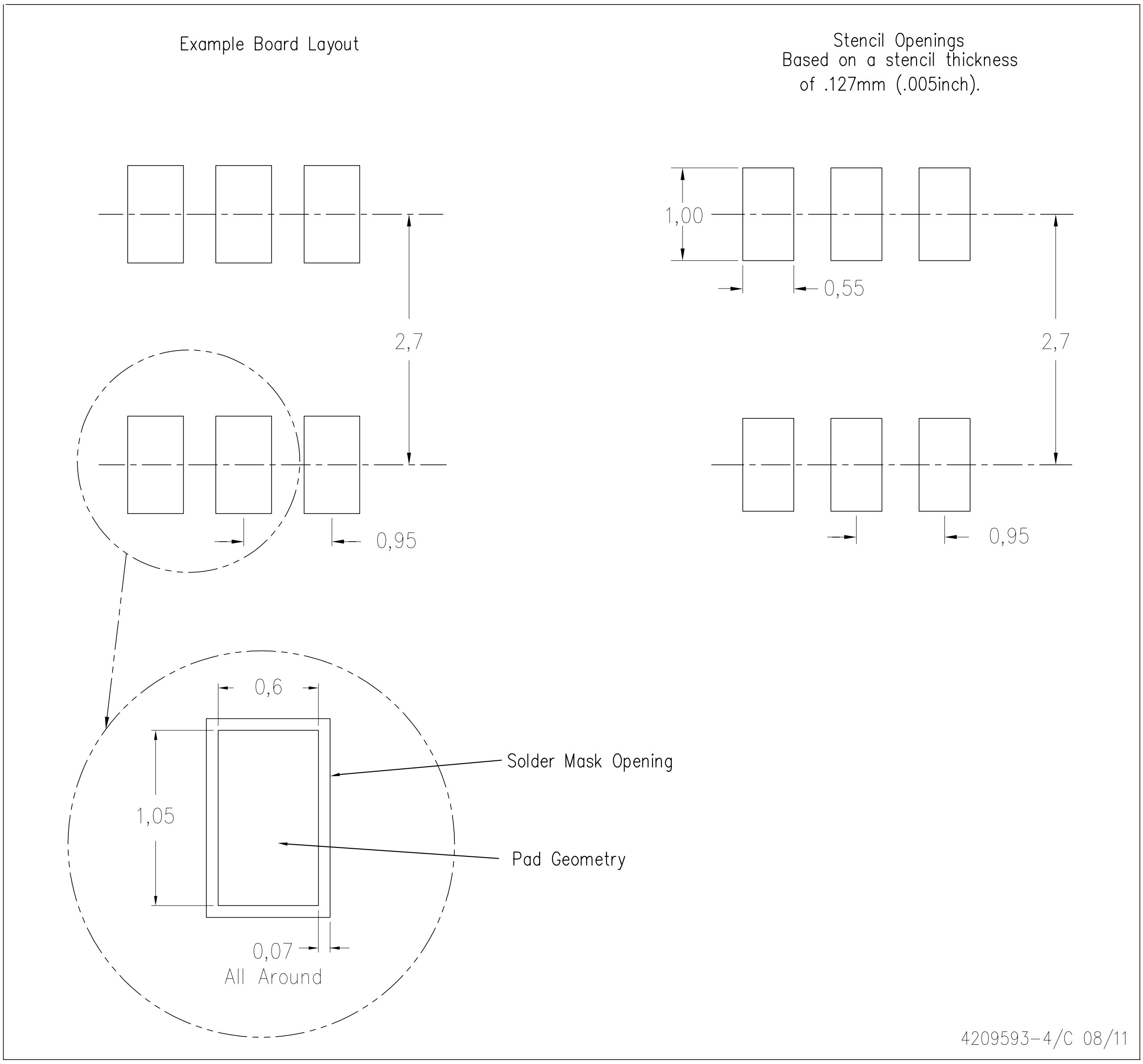
DBV (R-PDSO-G6) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO-178 Variation AB, except minimum lead width.

LAND PATTERN DATA

DBV (R-PDSO-G6) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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