# Excellent Integrated System Limited

Stocking Distributor

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Vishay/Siliconix
SI8851EDB-T2-E1

For any questions, you can email us directly:
sales@integrated-circuit.com

# P-Channel 20 V (D-S) MOSFET

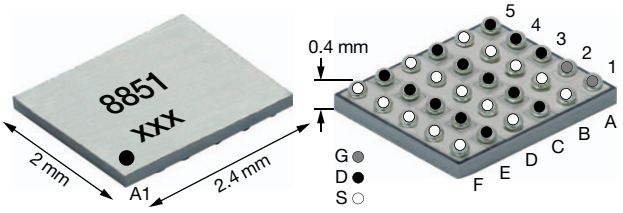
| PRODUCT SUMMARY | | | |
|---|---|---|---|
| $V_{DS}$ (V) | $R_{DS(on)}$ (Ω) Max. | $I_D$ (A) [a, d] | $Q_g$ (Typ.) |
| -20 | 0.0080 at $V_{GS}$ = -4.5 V | -16.7 | 70 nC |
| | 0.0086 at $V_{GS}$ = -3.7 V | -16.1 | |
| | 0.0110 at $V_{GS}$ = -2.5 V | -14.2 | |
| | 0.0185 at $V_{GS}$ = -1.8 V | -11 | |

## FEATURES

- TrenchFET® power MOSFET
- Small 2.4 mm x 2 mm outline area
- Low 0.4 mm max. profile
- Typical ESD protection 6000 V HBM
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free
RoHS COMPLIANT
HALOGEN FREE

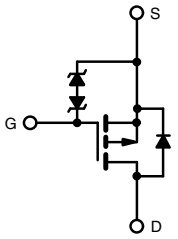
**Power MICRO FOOT® 2.4 x 2**




Backside View  Bump Side View

## APPLICATIONS

- Battery switch / load switch
- Power management
- For smart phones, tablet PCs, and mobile computing




P-Channel MOSFET

**Ordering Information:**
Si8851EDB-T2-E1 (Lead (Pb)-free and halogen-free)

| ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25 °C, unless otherwise noted) | | | | |
|---|---|---|---|---|
| PARAMETER | | SYMBOL | LIMIT | UNIT |
| Drain-Source Voltage | | $V_{DS}$ | -20 | V |
| Gate-Source Voltage | | $V_{GS}$ | ± 8 | |
| Continuous Drain Current ($T_J$ = 150 °C) | $T_A$ = 25 °C | $I_D$ | -16.7 [a] | A |
| | $T_A$ = 70 °C | | -13.4 [a] | |
| | $T_A$ = 25 °C | | -7.7 [b] | |
| | $T_A$ = 70 °C | | -6.2 [b] | |
| Pulsed Drain Current (t = 100 µs) | | $I_{DM}$ | -80 | |
| Continuous Source-Drain Diode Current | $T_C$ = 25 °C | $I_S$ | -2.6 [a] | |
| | $T_A$ = 25 °C | | -0.55 [b] | |
| Maximum Power Dissipation | $T_A$ = 25 °C | $P_D$ | 3.1 [a] | W |
| | $T_A$ = 70 °C | | 2 [a] | |
| | $T_A$ = 25 °C | | 0.66 [b] | |
| | $T_A$ = 70 °C | | 0.43 [b] | |
| Operating Junction and Storage Temperature Range | | $T_J$, $T_{stg}$ | -55 to +150 | °C |
| Package Reflow Conditions [c] | VPR | | 260 | |
| | IR/Convection | | 260 | |

**Notes**
a. Surface mounted on 1" x 1" FR4 board with full copper, t = 5 s.
b. Surface mounted on 1" x 1" FR4 board with minimum copper, t = 5 s.
c. Refer to IPC/JEDEC® (J-STD-020), no manual or hand soldering.
d. Based on $T_A$ = 25 °C.

| THERMAL RESISTANCE RATINGS | | | | | |
|---|---|---|---|---|---|
| PARAMETER | | SYMBOL | Typical | Maximum | Unit |
| Maximum Junction-to-Ambient [a, b] | t = 5 s | $R_{thJA}$ | 30 | 40 | °C/W |
| Maximum Junction-to-Ambient [c, d] | t = 5 s | | 145 | 188 | |

**Notes**
a. Surface mounted on 1" x 1" FR4 board with full copper.
b. Maximum under steady state conditions is 85 °C/W.
c. Surface mounted on 1" x 1" FR4 board with minimum copper.
d. Maximum under steady state conditions is 330 °C/W.

**SPECIFICATIONS** ($T_J$ = 25 °C, unless otherwise noted)

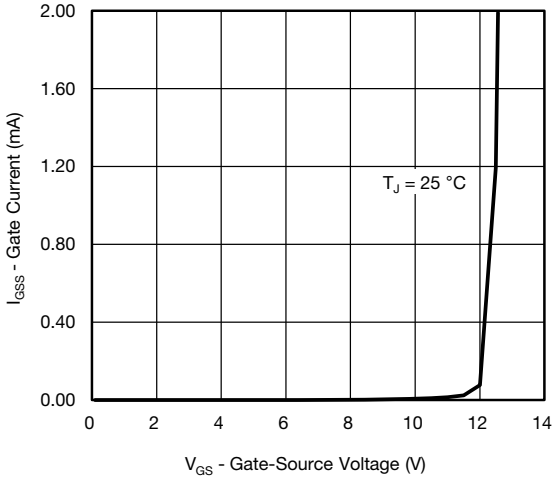
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $V_{DS}$ | $V_{GS}$ = 0 V, $I_D$ = -250 µA | -20 | - | - | V |
| $V_{DS}$ Temperature Coefficient | $\Delta V_{DS}/T_J$ | $I_D$ = -250 µA | - | -11 | - | mV/°C |
| $V_{GS(th)}$ Temperature Coefficient | $\Delta V_{GS(th)}/T_J$ | | - | 3 | - | |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = -250 µA | -0.45 | - | -1 | V |
| Gate-Source Leakage | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ± 4.5 V | - | - | ± 0.5 | µA |
| | | $V_{DS}$ = 0 V, $V_{GS}$ = ± 8 V | - | - | ± 10 | |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = -20 V, $V_{GS}$ = 0 V | - | - | -1 | |
| | | $V_{DS}$ = -20 V, $V_{GS}$ = 0 V, $T_J$ = 70 °C | - | - | -10 | |
| On-State Drain Current [a] | $I_{D(on)}$ | $V_{DS} \leq$ -5 V, $V_{GS}$ = -4.5 V | -5 | - | - | A |
| Drain-Source On-State Resistance [a] | $R_{DS(on)}$ | $V_{GS}$ = -4.5 V, $I_D$ = -7 A | - | 0.0060 | 0.0080 | Ω |
| | | $V_{GS}$ = -3.7 V, $I_D$ = -7 A | - | 0.0065 | 0.0086 | |
| | | $V_{GS}$ = -2.5 V, $I_D$ = -5 A | - | 0.0081 | 0.0110 | |
| | | $V_{GS}$ = -1.8 V, $I_D$ = -3 A | - | 0.0130 | 0.0185 | |
| Forward Transconductance [a] | $g_{fs}$ | $V_{DS}$ = -10 V, $I_D$ = -7 A | - | 50 | - | S |
| **Dynamic [b]** | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = -10 V, $V_{GS}$ = 0 V, f = 1 MHz | - | 6900 | - | pF |
| Output Capacitance | $C_{oss}$ | | - | 640 | - | |
| Reverse Transfer Capacitance | $C_{rss}$ | | - | 715 | - | |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = -10 V, $V_{GS}$ = -8 V, $I_D$ = -5 A | - | 120 | 180 | nC |
| | | $V_{DS}$ = -10 V, $V_{GS}$ = -4.5 V, $I_D$ = -5 A | - | 70 | 105 | |
| Gate-Source Charge | $Q_{gs}$ | | - | 8 | - | |
| Gate-Drain Charge | $Q_{gd}$ | | - | 14 | - | |
| Gate Resistance | $R_g$ | $V_{GS}$ = -0.1 V, f = 1 MHz | - | 2.3 | - | Ω |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = -10 V, $R_L$ = 2 Ω<br>$I_D \cong$ -5 A, $V_{GEN}$ = -4.5 V, $R_g$ = 1 Ω | - | 35 | 70 | ns |
| Rise Time | $t_r$ | | - | 40 | 80 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 115 | 230 | |
| Fall Time | $t_f$ | | - | 35 | 70 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = -10 V, $R_L$ = 2 Ω<br>$I_D \cong$ -5 A, $V_{GEN}$ = -8 V, $R_g$ = 1 Ω | - | 15 | 30 | |
| Rise Time | $t_r$ | | - | 10 | 20 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 110 | 220 | |
| Fall Time | $t_f$ | | - | 25 | 50 | |
| **Drain-Source Body Diode Characteristics** | | | | | | |
| Continuous Source-Drain Diode Current | $I_S$ | $T_A$ = 25 °C | - | - | -2.6 | A |
| Pulse Diode Forward Current (t = 100 µs) | $I_{SM}$ | | - | - | -80 | |
| Body Diode Voltage | $V_{SD}$ | $I_S$ = -5 A, $V_{GS}$ = 0 V | - | -0.8 | -1.2 | V |
| Body Diode Reverse Recovery Time | $t_{rr}$ | $I_F$ = -5 A, dI/dt = 100 A/µs,<br>$T_J$ = 25 °C | - | 40 | 80 | ns |
| Body Diode Reverse Recovery Charge | $Q_{rr}$ | | - | 30 | 60 | nC |
| Reverse Recovery Fall Time | $t_a$ | | - | 16 | - | ns |
| Reverse Recovery Rise Time | $t_b$ | | - | 24 | - | |

**Notes**

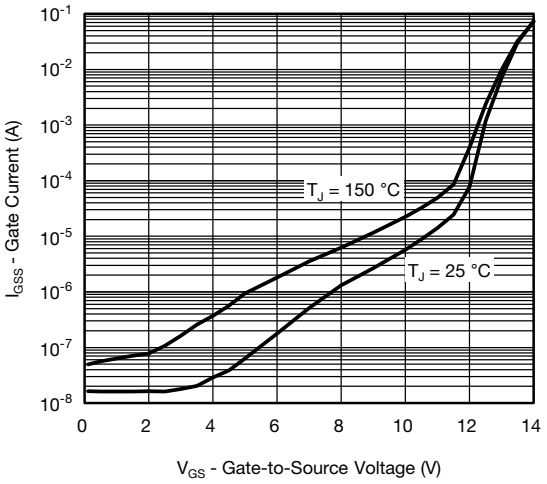
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

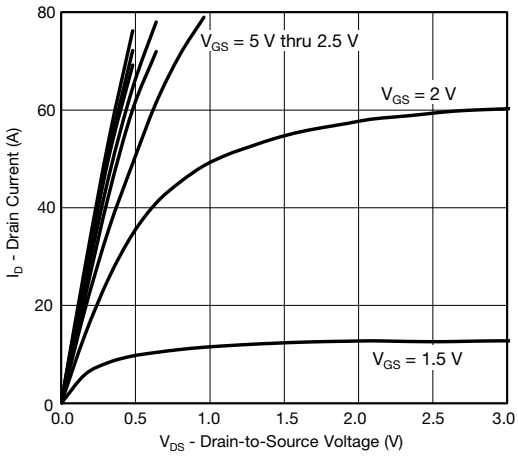
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



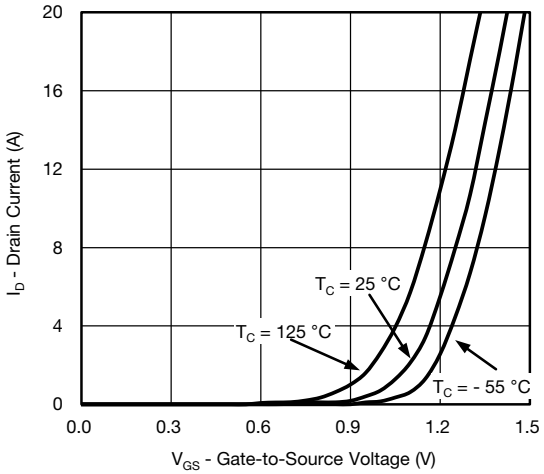

**Gate Current vs. Gate-Source Voltage**



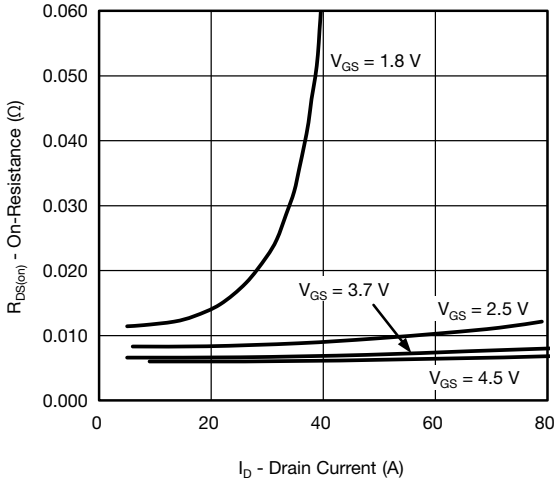

**Gate Current vs. Gate-Source Voltage**



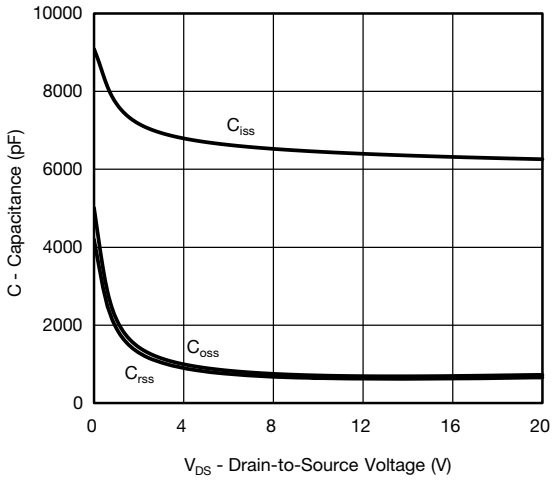

**Output Characteristics**




**Transfer Characteristics**

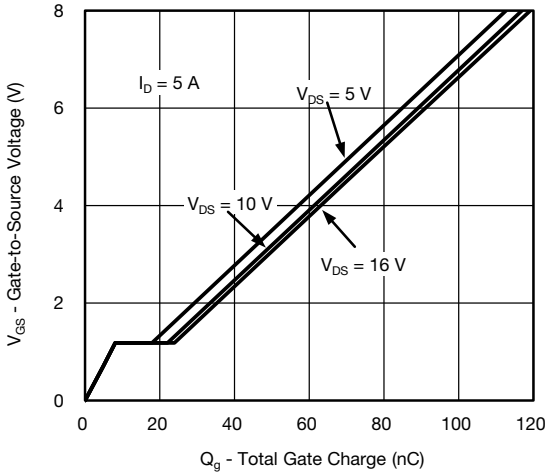



**On-Resistance vs. Drain Current and Gate Voltage**

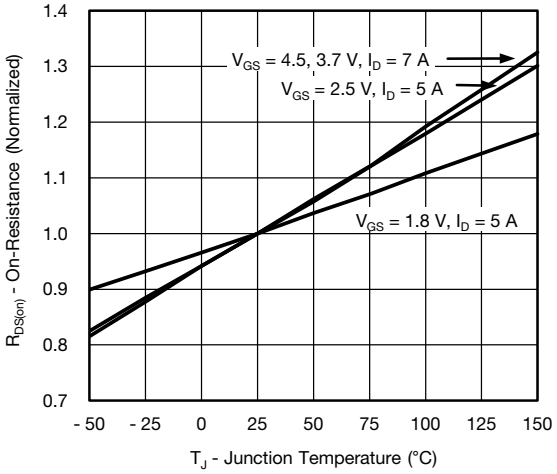



**Capacitance**

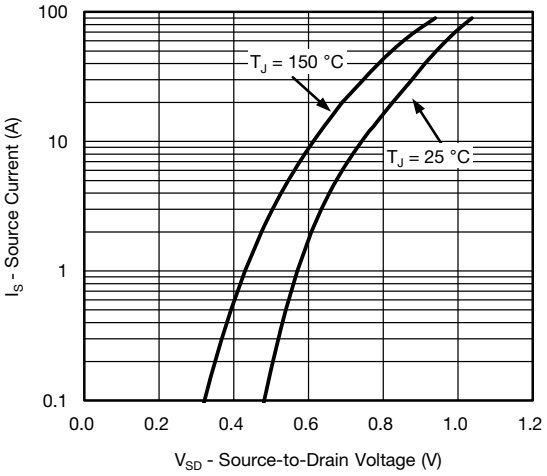
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



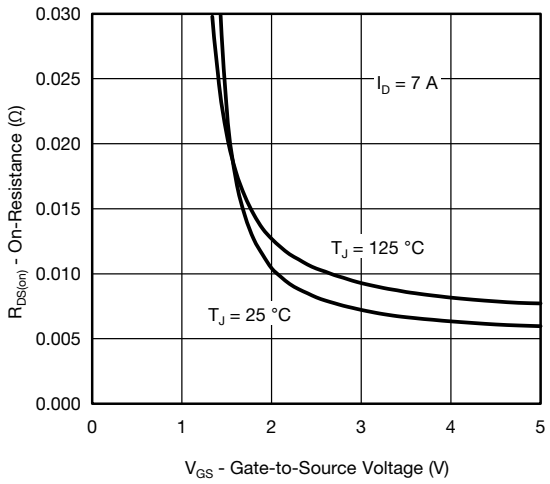

**Gate Charge**



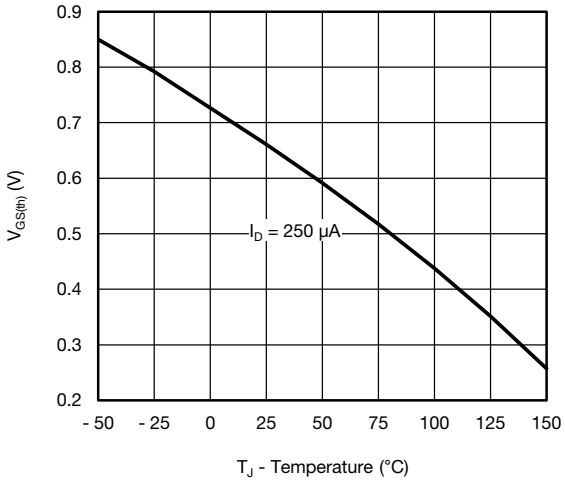

**On-Resistance vs. Junction Temperature**



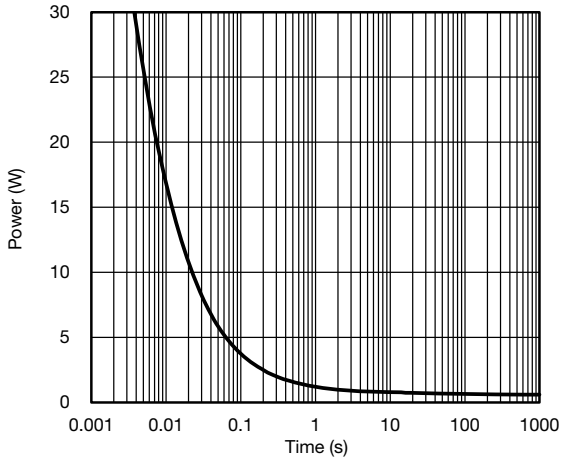

**Source-Drain Diode Forward Voltage**




**On-Resistance vs. Gate-to-Source Voltage**

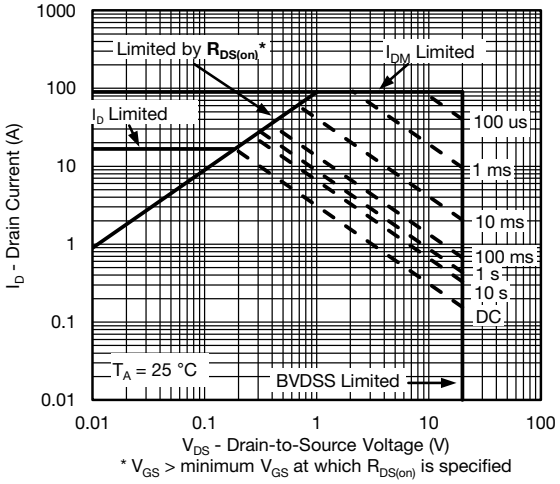



**Threshold Voltage**

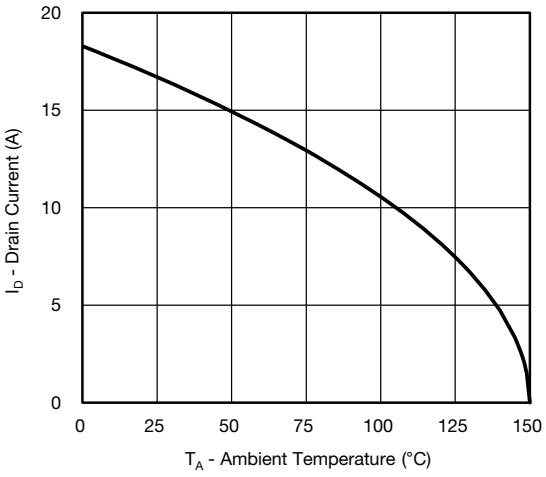



**Single Pulse Power, Junction-to-Ambient**

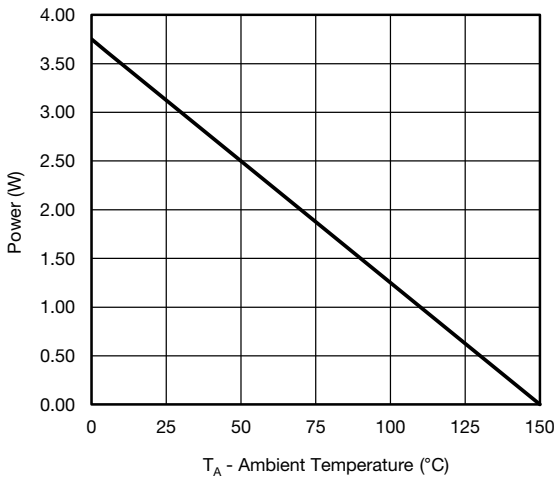
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)




**Safe Operating Area, Junction-to-Ambient[a]**




**Current Derating [a]**

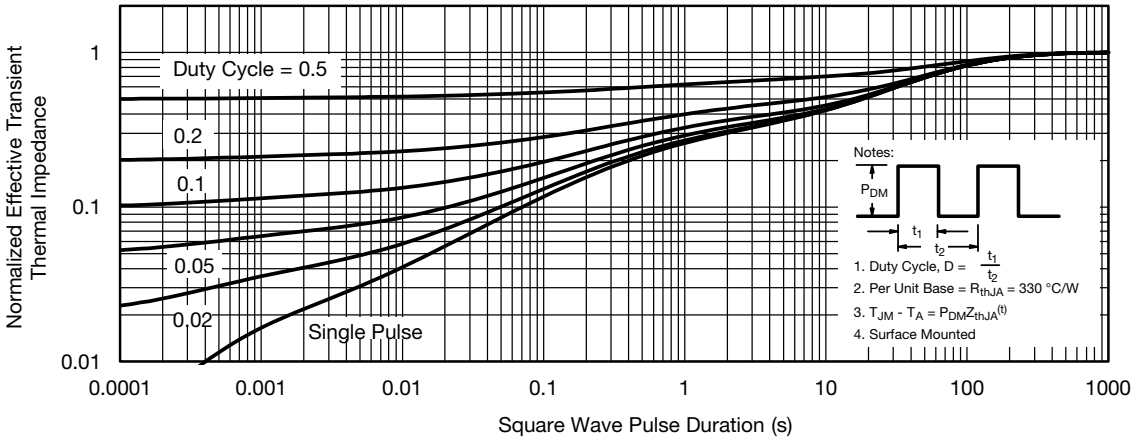



**Power Derating[a]**

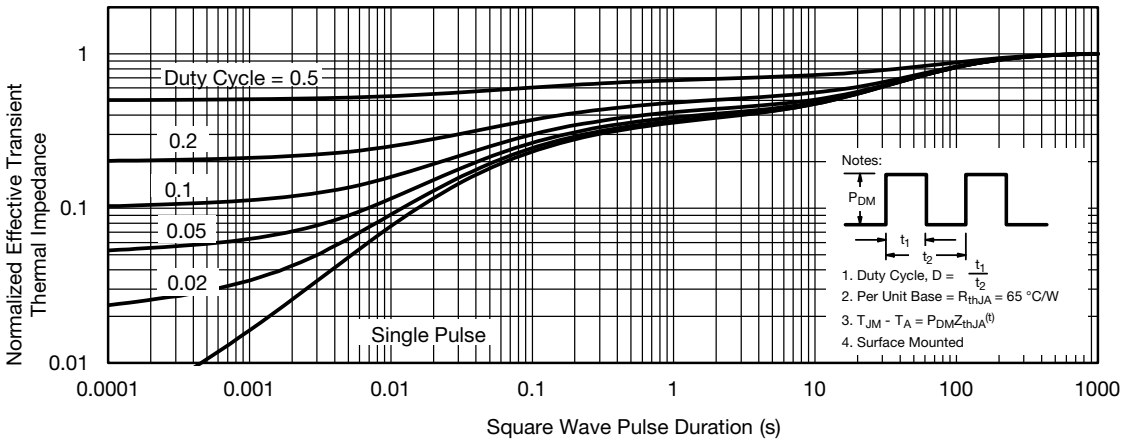
**Note**

a. When mounted on 1" x 1" FR4 with full copper and t = 5 s

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



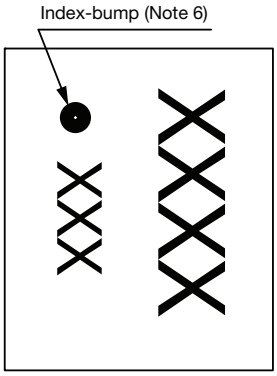

**Normalized Thermal Transient Impedance, Junction-to-Ambient (on 1" x 1" FR4 Board with minimum Copper)**



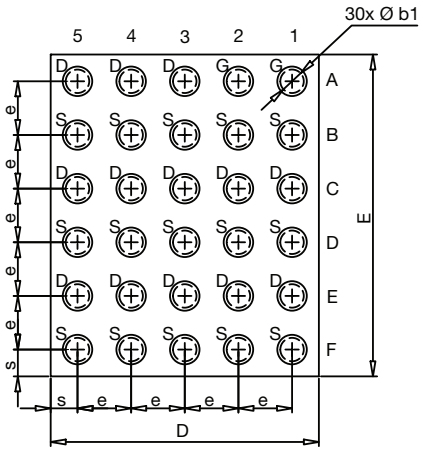

**Normalized Thermal Transient Impedance, Junction-to-Ambient (on 1" x 1" FR4 Board with maximum Copper)**

*Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?64197.*

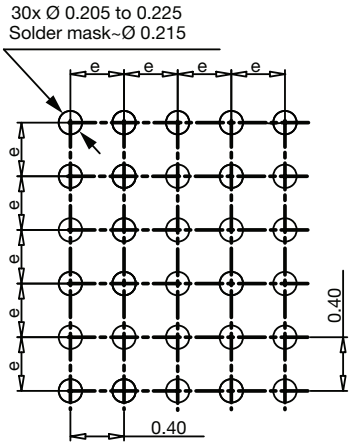
# MICRO FOOT®: 30-Bumps
# (2.4 mm x 2 mm, 0.4 mm Pitch, 0.184 mm Bump Height)



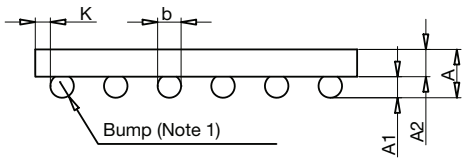

Top side (die back)

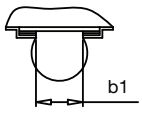



Bump side view




Recommended land pattern




**Notes**

1. Bumps are 95.5/3.8/0.7 Sn/Ag/Cu.
2. Backside surface is coated with a Ti/Ni/Ag layer.
3. Non-solder mask defined copper landing pad.
4. Laser marks on the silicon die back.
5. “b1” is the diameter of the solderable substrate surface, defined by an opening in the solder resist layer solder mask defined.
6. • is the location of pin 1

| DIM. | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.328 | 0.365 | 0.402 | 0.0129 | 0.0144 | 0.0158 |
| A1 | 0.136 | 0.160 | 0.184 | 0.0054 | 0.0063 | 0.0072 |
| A2 | 0.192 | 0.205 | 0.218 | 0.0076 | 0.0081 | 0.0086 |
| b | 0.200 | 0.220 | 0.240 | 0.0079 | 0.0087 | 0.0094 |
| b1 | | 0.175 | | | 0.0069 | |
| e | | 0.400 | | | 0.0157 | |
| s | 0.160 | 0.180 | 0.200 | 0.0063 | 0.0071 | 0.0079 |
| D | 1.920 | 1.960 | 2.000 | 0.0756 | 0.0772 | 0.0787 |
| E | 2.320 | 2.360 | 2.400 | 0.0913 | 0.0929 | 0.0945 |
| K | 0.040 | 0.070 | 0.100 | 0.0016 | 0.0028 | 0.0039 |

**Note**

- Use millimeters as the primary measurement.

ECN: T15-0177-Rev. A, 27-Apr-15
DWG: 6040

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