Excellent Integrated System Limited

Stocking Distributor

Click to view price, real time Inventory, Delivery & Lifecycle Information:

Texas Instruments
LMV934MT/NOPB

For any questions, you can email us directly:
sales@integrated-circuit.com

LMV93x-N/-N-Q1 Single, Dual, Quad 1.8-V, RRIO Operational Amplifiers

1 Features

- Typical 1.8-V Supply Values; Unless Otherwise Noted
- Available in Automotive AEC-Q100 Grade 1
- Specified at 1.8-V, 2.7-V and 5-V
- Output Swing
  - With 600-Ω Load 80 mV from Rail
  - With 2-kΩ Load 30 mV from Rail
- V_{CM} 200 mV Beyond Rails
- Supply Current (per Channel) 100 µA
- Gain Bandwidth Product 1.4 MHz
- Maximum V_{OS} 4.0 mV
- Ultra Tiny Packages
- Temperature Range −40°C to 125°C

2 Applications

- Mobile Phones
- Tablets
- Wearables
- Health Monitoring
- Portable and Battery-Powered Electronic Equipment
- Battery Monitoring

3 Description

The LMV93x-N family (LMV931-N single, LMV932-N dual and LMV934-N quad) are low-voltage, low-power operational amplifiers. The LMV93x-N family operates from 1.8-V to 5.5-V supply voltages and have rail-to-rail input and output. The input common-mode voltage extends 200 mV beyond the supplies which enables user enhanced functionality beyond the supply voltage range. The output can swing rail-to-rail unloaded and within 105 mV from the rail with 600-Ω load at 1.8-V supply. The LMV93x-N devices are optimized to work at 1.8 V, which make them ideal for portable two-cell, battery-powered systems and single-cell Li-Ion systems.

LMV93x-N devices exhibit an excellent speed-power ratio, achieving 1.4-MHz gain bandwidth product at 1.8-V supply voltage with very low supply current. The LMV93x-N devices can drive a 600-Ω load and up to 1000-pF capacitive load with minimal ringing. These devices also have a high DC gain of 101 dB, making them suitable for low-frequency applications.

The single LMV93x-N is offered in space-saving 5-pin SC70 and SOT-23 packages. The dual LMV932-N are in 8-pin VSSOP and SOIC packages and the quad LMV934-N are in 14-pin TSSOP and SOIC packages. These small packages are ideal solutions for area constrained PC boards and portable electronics such as mobile phones and tablets.

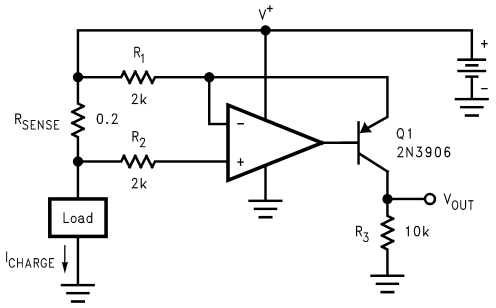
The LMV93x-N-Q1 family retains all the LMV93x-N family features while adding AEC-Q100 Grade 1 qualification for automotive applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMV931-N	SOT-23 (5)	2.90 mm × 1.60 mm
LMV931-N-Q1	SC-70 (5)	2.00 mm × 1.25 mm
LMV932-N	VSSOP (8)	3.00 mm × 3.00 mm
LMV932-N-Q1	SOIC (8)	4.90 mm × 3.91 mm
LMV934-N	TSSOP (8)	5.00 mm × 4.40 mm
LMV934-N-Q1	SOIC (14)	8.60 mm × 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

High-Side Current Sense Amplifier



$$V_{OUT} = \frac{R_{SENSE} \bullet R_3}{R_1} \bullet I_{Charge} = 1\,\Omega \bullet I_{Charge}$$

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 Handling Ratings - Commercial ... 4
6.3 Handling Ratings - Automotive ... 4
6.4 Recommended Operating Ratings ... 4
6.5 Thermal Information ... 4
6.6 DC Electrical Characteristics 1.8 V ... 5
6.7 AC Electrical Characteristics 1.8 V ... 6
6.8 DC Electrical Characteristics 2.7 V ... 7
6.9 AC Electrical Characteristics 2.7 V ... 8
6.10 Electrical Characteristics 5 V DC ... 9
6.11 AC Electrical Characteristics 5 V ... 10
6.12 Typical Characteristics ... 11
7 Detailed Description ... 16
7.1 Overview ... 16
7.2 Functional Block Diagram ... 16
7.3 Feature Description ... 16
7.4 Device Functional Modes ... 16
8 Application and Implementation ... 18
8.1 Application Information ... 18
8.2 Typical Applications ... 18
8.3 Dos and Don'ts ... 21
9 Power Supply Recommendations ... 21
10 Layout ... 21
10.1 Layout Guidelines ... 21
10.2 Layout Example ... 22
11 Device and Documentation Support ... 23
11.1 Device Support ... 23
11.2 Documentation Support ... 23
11.3 Related Links ... 23
11.4 Trademarks ... 23
11.5 Electrostatic Discharge Caution ... 23
11.6 Glossary ... 23
12 Mechanical, Packaging, and Orderable Information ... 23

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision N (June 2014) to Revision O — **Page**

- Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision M (November 2013) to Revision N — **Page**

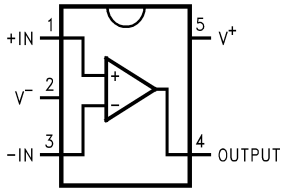
- Complete rewrite for GDS standard. ... 1
- Added LMV934-N-Q1. The other Q grades were added in previous revision. ... 1

Changes from Revision L (March 2013) to Revision M — **Page**

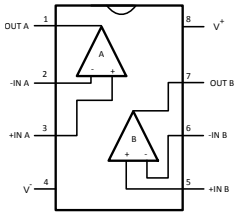
- Added Automotive Q Grade. ... 1
- Added Output Swing for Q-Grade in all Electrical Tables ... 6

5 Pin Configuration and Functions

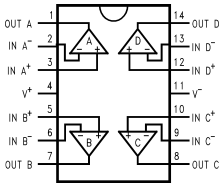
DBV and DCK Package
5-Pin SC-70 and SOT-23
LMV931-N, LMV931-N-Q1 Top View



DGK and D Package
8-Pin VSSOP and SOIC
LMV932-N, LMV932-N-Q1 Top View



DGK and D Package
14-Pin TSSOP and SOIC
LMV934-N, LMV934-N-Q1 Top View



Pin Functions: LMV931

PIN		I/O	DESCRIPTION
NAME	LMV931		
	DBV, DCK NO.		
+IN	1	I	Noninverting Input
-IN	3	I	Inverting Input
OUT	4	O	Output
V-	2	P	Negative Supply
V+	5	P	Positive Supply

Pin Functions: LMV932 and LMV934

PIN			I/O	DESCRIPTION
NAME	LMV932	LMV934		
	D, DGK NO.	D, PW NO.		
+IN A	3	3	I	Noninverting input, channel A
+IN B	5	5	I	Noninverting input, channel B
+IN C	—	10	I	Noninverting input, channel C
+IN D	—	12	I	Noninverting input, channel D
–IN A	2	2	I	Inverting input, channel A
–IN B	6	6	I	Inverting input, channel B
–IN C	—	9	I	Inverting input, channel C
–IN D	—	13	I	Inverting input, channel D
OUT A	1	1	O	Output, channel A
OUT B	7	7	O	Output, channel B
OUT C	—	8	O	Output, channel C
OUT D	—	14	O	Output, channel D
V+	8	4	P	Positive (highest) power supply
V–	4	11	P	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

See (1)(2).

	MIN	MAX	UNIT
Supply voltage ($V^+ – V^-$)	–0.3	6	V
Differential input voltage	V^-	V^+	
Voltage at input/output pins	(V^-) - 0.3	(V^+) + 0.3	
Junction temperature(3)	–40	150	°C

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Recommended Operating Conditions* indicate conditions for which the device is intended to be functional, but specific performance is not specified. For specifications and the test conditions, see the *Electrical Characteristics*.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) The maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)}–T_A)/R_{\theta JA}$. All numbers apply for packages soldered directly into a PC board.

6.2 Handling Ratings - Commercial

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) (2)	–2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(3)	–750	750	
		Machine Model (MM)(4)	–200	200	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(3) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
(4) Machine model, 200 Ω in series with 100-pF.

6.3 Handling Ratings - Automotive

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	–2000	2000	V
		Charged device model (CDM), per AEC Q100-011	–750	750	
		Machine Model (MM)(2)	–200	200	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) Machine model, 200 Ω in series with 100-pF.

6.4 Recommended Operating Ratings

See (1).

	MIN	MAX	UNIT
Supply Voltage Range ($V^+ – V^-$)	1.8	5.5	V
Temperature Range	−40	125	°C

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Recommended Operating Conditions* indicate conditions for which the device is intended to be functional, but specific performance is not specified. For specifications and the test conditions, see the *Electrical Characteristics*.

6.5 Thermal Information

THERMAL METRIC(1)		LMV921		LMV922		LMV924		UNIT
		DCK	DBV	DGK	D	DGK	D	
		5 PINS		8 PINS		14 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	414	265	235	175	155	127	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.6 DC Electrical Characteristics 1.8 V

Unless otherwise specified, all limits specified for T_J = 25°C. V^+ = 1.8 V, V^- = 0 V, $V_{CM} = V^+/2$, $V_O = V^+/2$ and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS		MIN	TYP (1)	MAX	UNIT
V_{OS}	Input Offset Voltage	LMV931 (Single)	25°C		1	4	mV
			Full Range			6	
		LMV932 (Dual), LMV934 (Quad)	25°C		1	5.5	mV
			Full Range			7.5	
TCV_{OS}	Input Offset Voltage Average Drift		Full Range		5.5		µV/°C
I_B	Input Bias Current		25°C		15	35	nA
			Full Range			50	
I_{OS}	Input Offset Current		25°C		13	25	nA
			Full Range			40	
I_S	Supply Current (per channel)		25°C		103	185	µA
			Full Range			205	
CMRR	Common-Mode Rejection Ratio	LMV931, 0 ≤ V_{CM} ≤ 0.6 V 1.4 V ≤ V_{CM} ≤ 1.8 V (2)	25°C	60	78		dB
			Full Range	55			
		LMV932 and LMV934 0 ≤ V_{CM} ≤ 0.6 V 1.4 V ≤ V_{CM} ≤ 1.8 V (2)	25°C	55	76		dB
			Full Range	50			
		−0.2 V ≤ V_{CM} ≤ 0 V 1.8 V ≤ V_{CM} ≤ 2.0 V	25°C	50	72		dB
PSRR	Power Supply Rejection Ratio	1.8 V ≤ V^+ ≤ 5 V	25°C	75	100		dB
			Full Range	70			
CMVR	Input Common-Mode Voltage Range	For CMRR Range ≥ 50dB	25°C	V^- − 0.2	−0.2 to 2.1	V^+ + 0.2	V
			−40°C to 85°C	V^-		V^+	
			125°C	V^- + 0.2		V^+ − 0.2	
A_V	Large Signal Voltage Gain LMV931-N (Single) LMV931-N-Q1 (Single)	R_L = 600 Ω to 0.9 V, V_O = 0.2 V to 1.6 V, V_{CM} = 0.5 V	25°C	77	101		dB
			Full Range	73			
		R_L = 2 kΩ to 0.9 V, V_O = 0.2 V to 1.6 V, V_{CM} = 0.5 V	25°C	80	105		dB
			Full Range	75			
	Large Signal Voltage Gain LMV932-N (Dual) LMV932-N-Q1 (Dual) LMV934-N (Quad) LMV934-N-Q1 (Quad)	R_L = 600 Ω to 0.9 V, V_O = 0.2 V to 1.6 V, V_{CM} = 0.5 V	25°C	75	90		dB
			Full Range	72			
		R_L = 2 kΩ to 0.9 V, V_O = 0.2 V to 1.6 V, V_{CM} = 0.5 V	25°C	78	100		dB
			Full Range	75			
V_O	Output Swing	R_L = 600 Ω to 0.9 V V_{IN} = ±100 mV	25°C	1.65	1.72		V
					0.077	0.105	
			Full Range	1.63		0.120	
		R_L = 2 kΩ to 0.9 V V_{IN} = ±100 mV	25°C	1.75	1.77		V
					0.024	0.035	
			Full Range	1.74		0.04	

(1) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.
(2) For specified temperature ranges, see the CMVR parameter in *DC Electrical Characteristics 1.8 V* for the input common-mode voltage specifications.

DC Electrical Characteristics 1.8 V (continued)

Unless otherwise specified, all limits specified for T_J = 25°C. V^+ = 1.8 V, V^- = 0 V, V_{CM} = $V^+/2$, V_O = $V^+/2$ and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS		MIN	TYP (1)	MAX	UNIT
V_O	Output Swing LMV932-N-Q1 (Dual) LMV934-N-Q1 (Quad)	R_L = 600 Ω to 0.9 V V_{IN} = ±100 mV	25°C	1.65	1.72		V
					0.077	0.105	
			Full Range	1.63		0.173	
		R_L = 2 kΩ to 0.9 V V_{IN} = ±100 mV	25°C	1.75	1.77		V
					0.024	0.035	
			Full Range	1.74		0.055	
I_O	Output Short Circuit Current (3)	Sourcing, V_O = 0 V V_{IN} = 100 mV	25°C	4	8		mA
			Full Range	3.3			
		Sinking, V_O = 1.8 V V_{IN} = −100 mV	25°C	7	9		mA
			Full Range	5			

(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45 mA over long term may adversely affect reliability.

6.7 AC Electrical Characteristics 1.8 V

Unless otherwise specified, all limits specified for T_J = 25°C. V^+ = 1.8 V, V^- = 0 V, V_{CM} = $V^+/2$, V_O = $V^+/2$ and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
SR	Slew Rate	See (2).		0.35		V/µs
GBW	Gain-Bandwidth Product			1.4		MHz
Φ_m	Phase Margin			67		deg
G_m	Gain Margin			7		dB
e_n	Input-Referred Voltage Noise	f = 10 kHz, V_{CM} = 0.5 V		60		nV/√Hz
i_n	Input-Referred Current Noise	f = 10 kHz		0.08		pA/√Hz
THD	Total Harmonic Distortion	f = 1 kHz, A_V = +1 R_L = 600 Ω, V_{IN} = 1 V_{PP}		0.023%		
	Amplifier-to-Amplifier Isolation	See (3)		123		dB

(1) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.
(2) Connected as voltage follower with input step from V^- to V^+. Number specified is the slower of the positive and negative slew rates.
(3) Input referred, R_L = 100 kΩ connected to $V^+/2$. Each amplifier excited in turn with 1 kHz to produce V_O = 3 V_{PP} (For Supply Voltages <3 V, V_O = V^+).

6.8 DC Electrical Characteristics 2.7 V

Unless otherwise specified, all limits specified for T_J = 25°C. V^+ = 2.7 V, V^- = 0 V, $V_{CM} = V^+/2$, $V_O = V^+/2$ and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS		MIN	TYP (1)	MAX	UNIT
V_{OS}	Input Offset Voltage	LMV931 (Single)	25°C		1	4	mV
			Full Range			6	
		LMV932 (Dual) LMV934 (Quad)	25°C		1	5.5	mV
			Full Range			7.5	
TCV_{OS}	Input Offset Voltage Average Drift		Full Range		5.5		µV/°C
I_B	Input Bias Current		25°C		15	35	nA
			Full Range			50	
I_{OS}	Input Offset Current		25°C		8	25	nA
			Full Range			40	
I_S	Supply Current (per channel)		25°C		105	190	µA
			Full Range			210	
CMRR	Common-Mode Rejection Ratio	LMV931, 0 ≤ V_{CM} ≤ 1.5 V 2.3 V ≤ V_{CM} ≤ 2.7 V (2)	25°C	60	81		dB
			Full Range	55			
		LMV932 and LMV934 0 ≤ V_{CM} ≤ 1.5 V 2.3 V ≤ V_{CM} ≤ 2.7 V (2)	25°C	55	80		dB
			Full Range	50			
		−0.2 V ≤ V_{CM} ≤ 0 V 2.7 V ≤ V_{CM} ≤ 2.9 V	25°C	50	74		dB
PSRR	Power Supply Rejection Ratio	1.8 V ≤ V^+ ≤ 5 V V_{CM} = 0.5 V	25°C	75	100		dB
			Full Range	70			
V_{CM}	Input Common-Mode Voltage Range	For CMRR Range ≥ 50 dB	25°C	V^- − 0.2	−0.2 to 3.0	V^+ + 0.2	V
			−40°C to 85°C	V^-		V^+	
			125°C	V^- + 0.2		V^+ − 0.2	
A_V	Large Signal Voltage Gain LMV931-N (Single) LMV931-N-Q1 (Single)	R_L = 600 Ω to 1.35 V, V_O = 0.2 V to 2.5 V	25°C	87	104		dB
			Full Range	86			
		R_L = 2 kΩ to 1.35 V, V_O = 0.2 V to 2.5 V	25°C	92	110		dB
			Full Range	91			
	Large Signal Voltage Gain LMV932-N (Dual) LMV932-N-Q1 (Dual) LMV934-N (Quad) LMV934-N-Q1 (Quad)	R_L = 600 Ω to 1.35 V, V_O = 0.2 V to 2.5 V	25°C	78	90		dB
			Full Range	75			
		R_L = 2 kΩ to 1.35 V, V_O = 0.2 V to 2.5 V	25°C	81	100		dB
			Full Range	78			
V_O	Output Swing	R_L = 600 Ω to 1.35 V V_{IN} = ±100 mV	25°C	2.55	2.62		V
					0.083	0.110	
			Full Range	2.53		0.130	
		R_L = 2 kΩ to 1.35 V V_{IN} = ±100 mV	25°C	2.65	2.675		V
					0.025	0.04	
			Full Range	2.64		0.045	
V_O	Output Swing LMV932-N-Q1 (Dual) LMV934-N-Q1 (Quad)	R_L = 600 Ω to 1.35 V V_{IN} = ±100 mV	25°C	2.55	2.62		V
					0.083	0.110	
			Full Range	2.53		0.187	
		R_L = 2 kΩ to 1.35 V V_{IN} = ±100 mV	25°C	2.65	2.675		V
					0.025	0.04	
			Full Range	2.64		0.059	

(1) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.
(2) For specified temperature ranges, see the CMVR parameter in *DC Electrical Characteristics 1.8 V* for the input common-mode voltage specifications.

DC Electrical Characteristics 2.7 V (continued)

Unless otherwise specified, all limits specified for T_J = 25°C. V^+ = 2.7 V, V^- = 0 V, V_{CM} = $V^+/2$, V_O = $V^+/2$ and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS		MIN	TYP (1)	MAX	UNIT
I_O	Output Short Circuit Current (3)	Sourcing, V_O = 0 V V_{IN} = +100 mV	25°C	20	30		mA
			Full Range	15			
		Sinking, V_O = 2.7 V V_{IN} = −100 mV	25°C	18	25		mA
			Full Range	12			

(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45 mA over long term may adversely affect reliability.

6.9 AC Electrical Characteristics 2.7 V

Unless otherwise specified, all limits specified for T_J = 25°C. V^+ = 2.7 V, V^- = 0 V, V_{CM} = 1.0 V, V_O = 1.35 V and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
SR	Slew Rate	See (2)		0.4		V/µs
GBW	Gain-Bandwidth Product			1.4		MHz
Φ_m	Phase Margin			70		deg
G_m	Gain Margin			7.5		dB
e_n	Input-Referred Voltage Noise	f = 10 kHz, V_{CM} = 0.5 V		57		nV/√Hz
i_n	Input-Referred Current Noise	f = 10 kHz		0.08		pA/√Hz
THD	Total Harmonic Distortion	f = 1 kHz, A_V = +1 R_L = 600 Ω, V_{IN} = 1 V_{PP}		0.022%		
	Amp-to-Amp Isolation	See (3)		123		dB

(1) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.
(2) Connected as voltage follower with input step from V^- to V^+. Number specified is the slower of the positive and negative slew rates.
(3) Input referred, R_L = 100 kΩ connected to $V^+/2$. Each amplifier excited in turn with 1 kHz to produce V_O = 3 V_{PP} (For Supply Voltages <3 V, V_O = V^+).

6.10 Electrical Characteristics 5 V DC

Unless otherwise specified, all limits specified for T_J = 25°C. V^+ = 5 V, V^- = 0 V, V_{CM} = $V^+/2$, V_O = $V^+/2$ and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS		MIN	TYP (1)	MAX	UNIT
V_{OS}	Input Offset Voltage	LMV931 (Single)	25°C		1	4	mV
			Full Range			6	
		LMV932 (Dual) LMV934 (Quad)	25°C		1	5.5	mV
			Full Range			7.5	
TCV_{OS}	Input Offset Voltage Average Drift				5.5		µV/°C
I_B	Input Bias Current		25°C		14	35	nA
			Full Range			50	
I_{OS}	Input Offset Current		25°C		9	25	nA
			Full Range			40	
I_S	Supply Current (per channel)		25°C		116	210	µA
			Full Range			230	
CMRR	Common-Mode Rejection Ratio	0 ≤ V_{CM} ≤ 3.8 V 4.6 V ≤ V_{CM} ≤ 5.0 V (2)	25°C	60	86		dB
			Full Range	55			
		−0.2 V ≤ V_{CM} ≤ 0 V 5.0 V ≤ V_{CM} ≤ 5.2 V	25°C	50	78		dB
PSRR	Power Supply Rejection Ratio	1.8 V ≤ V^+ ≤ 5 V V_{CM} = 0.5 V	25°C	75	100		dB
			Full Range	70			
CMVR	Input Common-Mode Voltage Range	For CMRR Range ≥ 50 dB	25°C	V^- − 0.2	−0.2 to 5.3	V^+ + 0.2	V
			−40°C to 85°C	V^-		V^+	
			125°C	V^- + 0.3		V^+ − 0.3	
A_V	Large Signal Voltage Gain LMV931-N (Single) LMV931-N-Q1 (Single)	R_L = 600 Ω to 2.5 V, V_O = 0.2 V to 4.8 V	25°C	88	102		dB
			Full Range	87			
		R_L = 2 kΩ to 2.5 V, V_O = 0.2 V to 4.8 V	25°C	94	113		dB
			Full Range	93			
	Large Signal Voltage Gain LMV932-N (Dual) LMV932-N-Q1 (Dual) LMV934-N (Quad) LMV934-N-Q1 (Quad)	R_L = 600 Ω to 2.5 V, V_O = 0.2 V to 4.8 V	25°C	81	90		dB
			Full Range	78			
		R_L = 2 kΩ to 2.5 V, V_O = 0.2 V to 4.8 V	25°C	85	100		dB
			Full Range	82			
V_O	Output Swing	R_L = 600 Ω to 2.5 V V_{IN} = ±100 mV	25°C	4.855	4.890		V
					0.120	0.160	
			Full Range	4.835		0.180	
		R_L = 2 kΩ to 2.5 V V_{IN} = ±100 mV	25°C	4.945	4.967		V
					0.037	0.065	
			Full Range	4.935		0.075	
V_O	Output Swing LMV932-N-Q1 (Dual) LMV934-N-Q1 (Quad)	R_L = 600 Ω to 2.5 V V_{IN} = ±100 mV	25°C	4.855	4.890		V
					0.120	0.160	
			Full Range	4.807		0.218	
		R_L = 2 kΩ to 2.5 V V_{IN} = ±100 mV	25°C	4.945	4.967		V
					0.037	0.065	
			Full Range	4.935		0.075	

(1) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.
(2) For specified temperature ranges, see the CMVR parameter in *DC Electrical Characteristics 1.8 V* for the input common-mode voltage specifications.

Electrical Characteristics 5 V DC (continued)

Unless otherwise specified, all limits specified for T_J = 25°C. V^+ = 5 V, V^- = 0 V, V_{CM} = V^+/2, V_O = V^+/2 and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS		MIN	TYP (1)	MAX	UNIT
I_O	Output Short Circuit Current (3)	LMV931, Sourcing, V_O = 0 V V_{IN} = +100 mV	25°C	80	100		mA
			Full Range	68			
		Sinking, V_O = 5 V V_{IN} = −100 mV	25°C	58	65		mA
			Full Range	45			

(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45 mA over long term may adversely affect reliability.

6.11 AC Electrical Characteristics 5 V

Unless otherwise specified, all limits specified for T_J = 25°C. V^+ = 5 V, V^- = 0 V, V_{CM} = V^+/2, V_O = 2.5 V and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
SR	Slew Rate	See . (2)		0.42		V/µs
GBW	Gain-Bandwidth Product			1.5		MHz
Φ_m	Phase Margin			71		deg
G_m	Gain Margin			8		dB
e_n	Input-Referred Voltage Noise	f = 10 kHz, V_{CM} = 1 V		50		nV/√Hz
i_n	Input-Referred Current Noise	f = 10 kHz		0.08		pA/√Hz
THD	Total Harmonic Distortion	f = 1 kHz, A_V = 1 R_L = 600 Ω, V_O = 1 V_{PP}		0.022%		
	Amplifier-to-Amplifier Isolation	See (3)		123		dB

(1) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.
(2) Connected as voltage follower with input step from V^- to V^+. Number specified is the slower of the positive and negative slew rates.
(3) Input referred, R_L = 100 kΩ connected to V^+/2. Each amplifier excited in turn with 1 kHz to produce V_O = 3 V_{PP} (For Supply Voltages <3 V, V_O = V^+).

6.12 Typical Characteristics

Unless otherwise specified, V_S = 5 V, single-supply, T_A = 25°C.

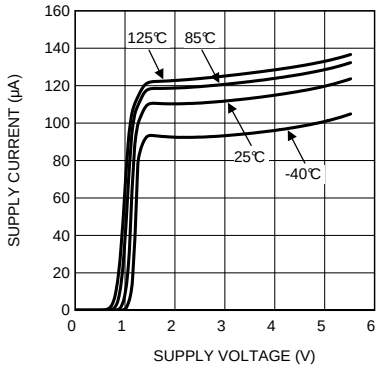


Figure 1. Supply Current vs. Supply Voltage (LMV931-N)

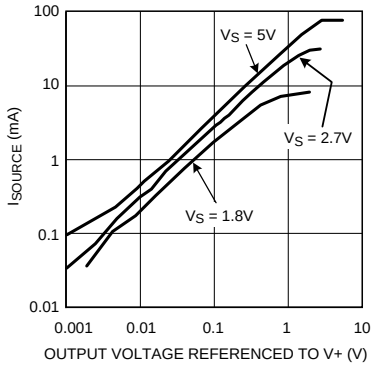


Figure 2. Sourcing Current vs. Output Voltage

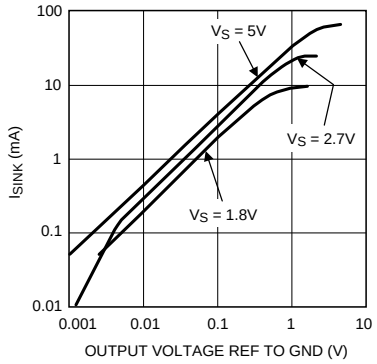


Figure 3. Sinking Current vs. Output Voltage

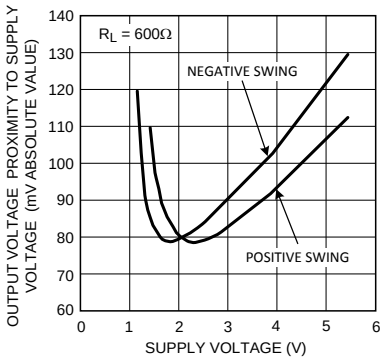


Figure 4. Output Voltage Swing vs. Supply Voltage

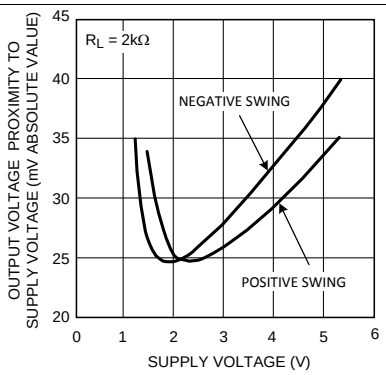


Figure 5. Output Voltage Swing vs. Supply Voltage

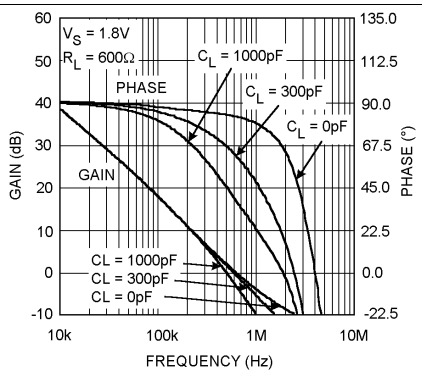


Figure 6. Gain and Phase vs. Frequency

Typical Characteristics (continued)

Unless otherwise specified, V_S = 5 V, single-supply, T_A = 25°C.

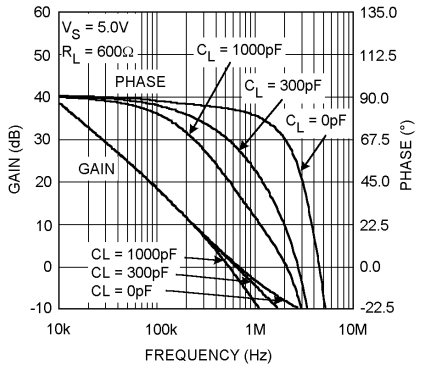


Figure 7. Gain and Phase vs. Frequency

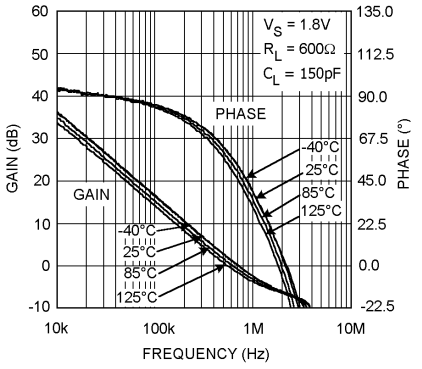


Figure 8. Gain and Phase vs. Frequency

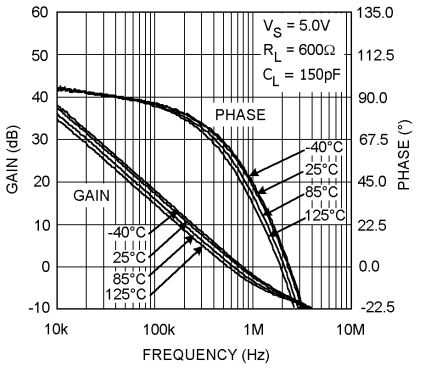


Figure 9. Gain and Phase vs. Frequency

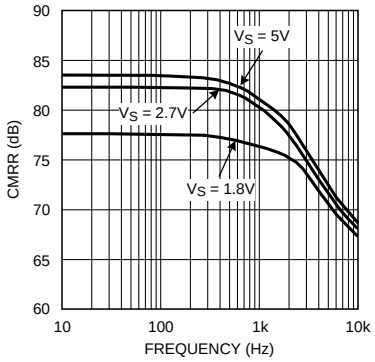


Figure 10. CMRR vs. Frequency

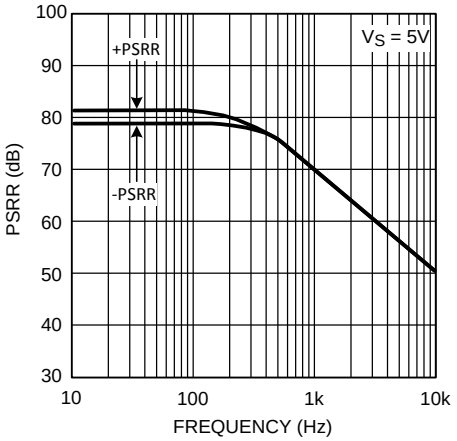


Figure 11. PSRR vs. Frequency

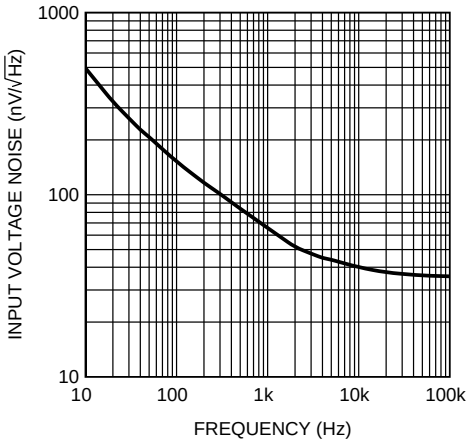


Figure 12. Input Voltage Noise vs. Frequency

Typical Characteristics (continued)

Unless otherwise specified, V_S = 5 V, single-supply, T_A = 25°C.

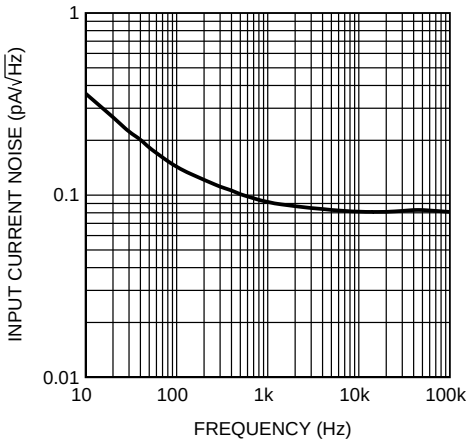


Figure 13. Input Current Noise vs. Frequency

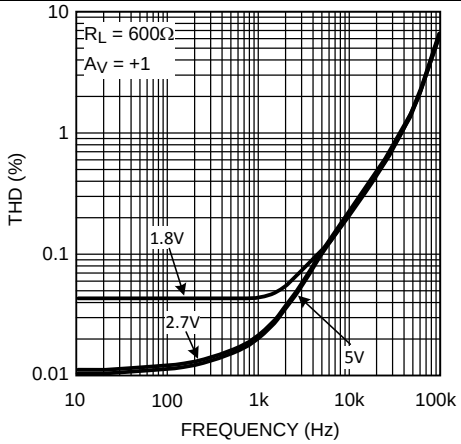


Figure 14. THD vs. Frequency

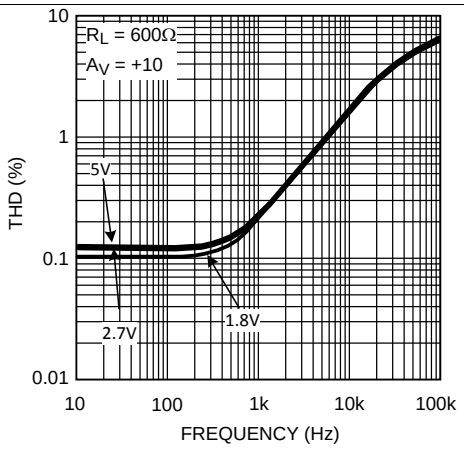


Figure 15. THD vs. Frequency

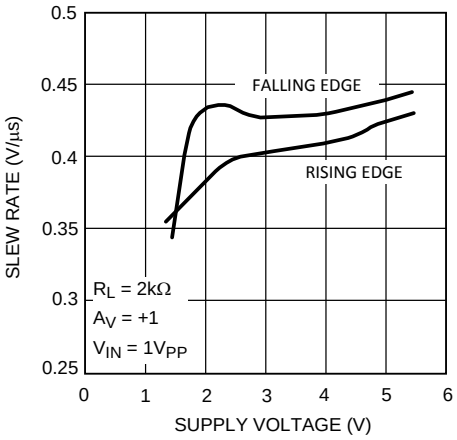


Figure 16. Slew Rate vs. Supply Voltage

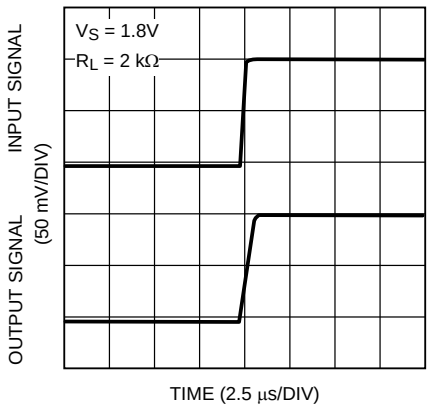


Figure 17. Small Signal Noninverting Response

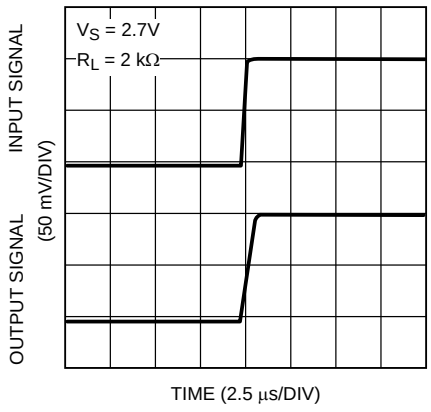


Figure 18. Small Signal Noninverting Response

Typical Characteristics (continued)

Unless otherwise specified, V_S = 5 V, single-supply, T_A = 25°C.

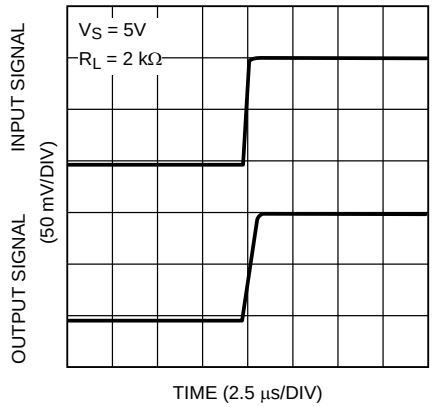


Figure 19. Small Signal Noninverting Response

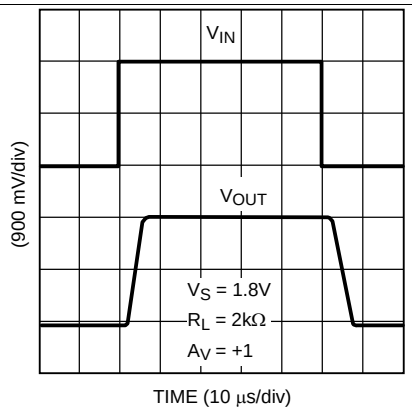


Figure 20. Large Signal Noninverting Response

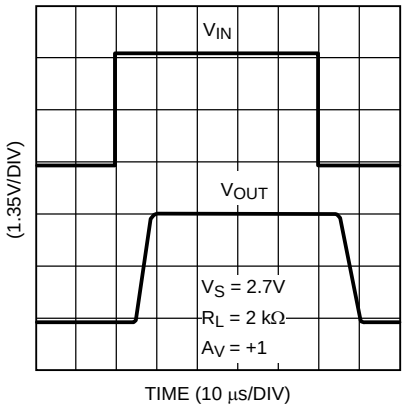


Figure 21. Large Signal Noninverting Response

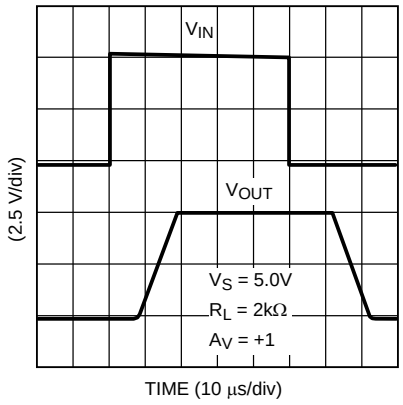


Figure 22. Large Signal Noninverting Response

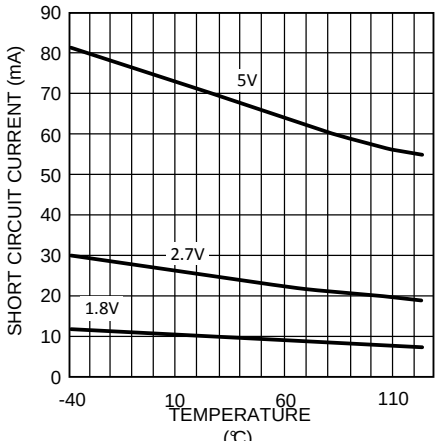


Figure 23. Short Circuit Current vs. Temperature (Sinking)

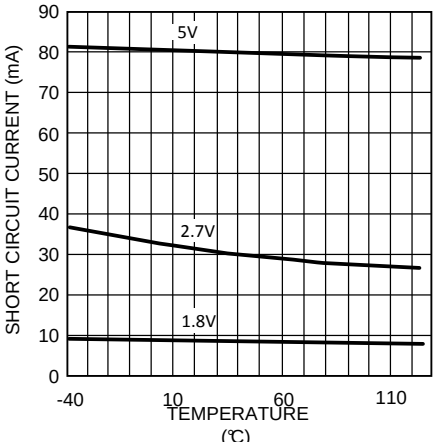


Figure 24. Short Circuit Current vs. Temperature (Sourcing)

Typical Characteristics (continued)

Unless otherwise specified, V_S = 5 V, single-supply, T_A = 25°C.

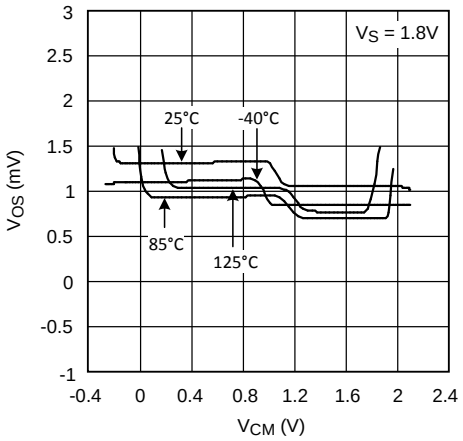


Figure 25. Offset Voltage vs. Common-Mode Range

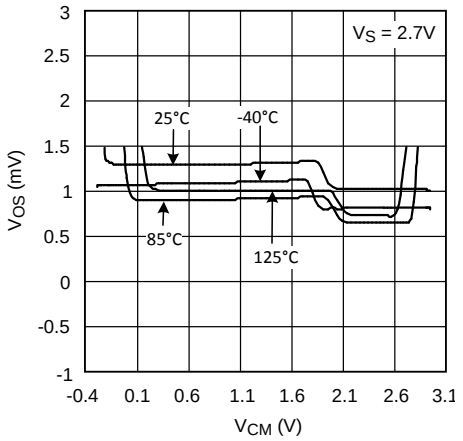


Figure 26. Offset Voltage vs. Common-Mode Range

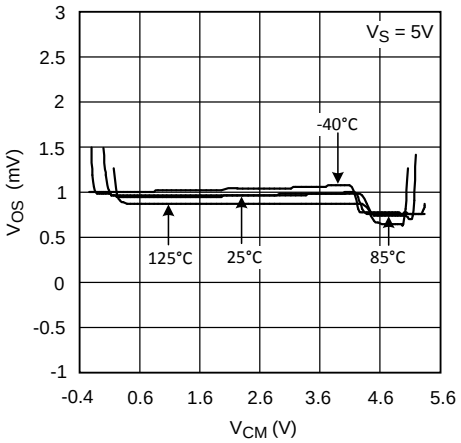


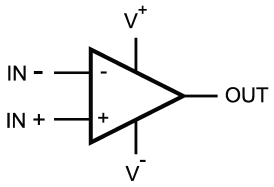
Figure 27. Offset Voltage vs. Common-Mode Range

7 Detailed Description

7.1 Overview

The LMV93x-N are low-voltage, low-power operational amplifiers (op-amp) operating from 1.8-V to 5.5-V supply voltages and have rail-to-rail input and output. LMV93x-N input common-mode voltage extends 200 mV beyond the supplies which enables user enhanced functionality beyond the supply voltage range.

7.2 Functional Block Diagram



(Each Amplifier)

7.3 Feature Description

The differential inputs of the amplifier consist of a noninverting input (+IN) and an inverting input (–IN). The amplifer amplifies only the difference in voltage between the two inputs, which is called the differential input voltage. The output voltage of the op-amp V_{OUT} is given by Equation 1:

$$V_{OUT} = A_{OL} (IN^+ - IN^-) \quad (1)$$

where

- A_{OL} is the open-loop gain of the amplifier, typically around 100 dB (100,000x, or 10 uV per volt).

7.4 Device Functional Modes

7.4.1 Input and Output Stage

The rail-to-rail input stage of this family provides more flexibility for the designer. The LMV93x-N use a complimentary PNP and NPN input stage in which the PNP stage senses common-mode voltage near V^- and the NPN stage senses common-mode voltage near V^+. The transition from the PNP stage to NPN stage occurs 1 V below V^+. Because both input stages have their own offset voltage, the offset of the amplifier becomes a function of the input common-mode voltage and has a crossover point at 1 V below V^+.

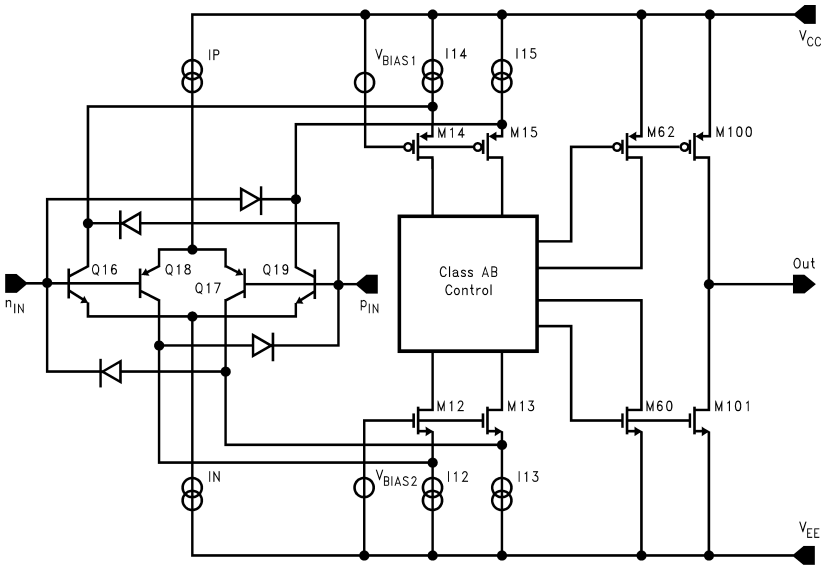


Figure 28. Simplified Schematic Diagram

Device Functional Modes (continued)

This V_{OS} crossover point can create problems for both DC− and AC-coupled signals if proper care is not taken. Large input signals that include the V_{OS} crossover point will cause distortion in the output signal. One way to avoid such distortion is to keep the signal away from the crossover. For example, in a unity gain buffer configuration with V_S = 5 V, a 5-V peak-to-peak signal will contain input-crossover distortion while a 3-V peak-to-peak signal centered at 1.5 V will not contain input-crossover distortion as it avoids the crossover point. Another way to avoid large signal distortion is to use a gain of −1 circuit which avoids any voltage excursions at the input terminals of the amplifier. In that circuit, the common-mode DC voltage can be set at a level away from the V_{OS} cross-over point. For small signals, this transition in V_{OS} shows up as a V_{CM} dependent spurious signal in series with the input signal and can effectively degrade small signal parameters such as gain and common-mode rejection ratio. To resolve this problem, the small signal should be placed such that it avoids the V_{OS} crossover point. In addition to the rail-to-rail performance, the output stage can provide enough output current to drive 600-Ω loads. Because of the high-current capability, take care not to exceed the 150°C maximum junction temperature specification.

7.4.2 Input Bias Current Consideration

The LMV93x-N family has a complementary bipolar input stage. The typical input bias current (I_B) is 15 nA. The input bias current can develop a significant offset voltage. This offset is primarily due to I_B flowing through the negative feedback resistor, R_F. For example, if I_B is 50 nA and R_F is 100 kΩ, then an offset voltage of 5 mV will develop (V_{OS} = I_B x R_F). Using a compensation resistor (R_C), as shown in Figure 29, cancels this effect. But the input offset current (I_{OS}) will still contribute to an offset voltage in the same manner.

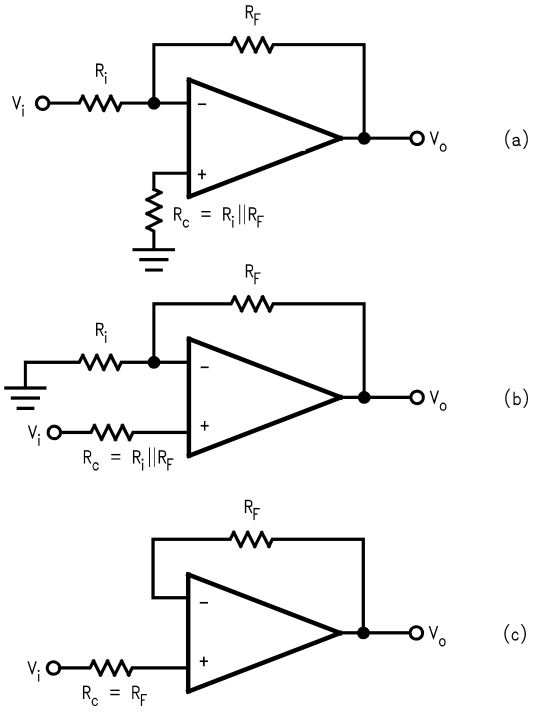


Figure 29. Canceling the Offset Voltage due to Input Bias Current

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMV93x-N devices bring performance, economy and ease-of-use to low-voltage, low-power systems. They provide rail-to-rail input and rail-to-rail output swings into heavy loads.

8.2 Typical Applications

8.2.1 High-Side Current-Sensing Application

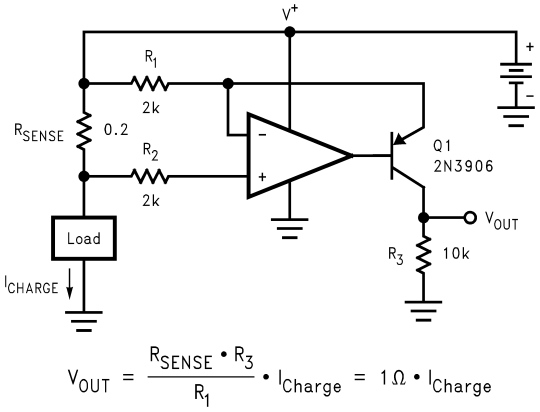


Figure 30. High-Side Current Sensing

8.2.1.1 Design Requirements

The high-side current-sensing circuit (Figure 30) is commonly used in a battery charger to monitor charging current to prevent overcharging. A sense resistor R_{SENSE} is connected to the battery directly. This system requires an op amp with rail-to-rail input. The LMV93x-N are ideal for this application because its common-mode input range extends up to the positive supply.

8.2.1.2 Detailed Design Procedure

As seen in Figure 30, the I_{CHARGE} current flowing through sense resistor R_{SENSE} develops a voltage drop equal to V_{SENSE}. The voltage at the negative sense point will now be less than the positive sense point by an amount proportional to the V_{SENSE} voltage.

The low-bias currents of the LMV93x cause little voltage drop through R_2, so the negative input of the LMV93x amplifier is at essentially the same potential as the negative sense input.

The LMV93x will detect this voltage error between its inputs and servo the transistor base to conduct more current through Q1, increasing the voltage drop across R_1 until the LMV93x inverting input matches the noninverting input. At this point, the voltage drop across R_1 now matches V_{SENSE}.

I_G, a current proportional to I_{CHARGE}, will flow according to the following relation:

$$I_G = V_{RSENSE} / R_1 = (R_{SENSE} * I_{CHARGE}) / R_1 \quad (2)$$

I_G also flows through the gain resistor R_3 developing a voltage drop equal to:

$$V_3 = I_G * R_3 = (V_{RSENSE} / R_1) * R_3 = ((R_{SENSE} * I_{CHARGE}) / R_2) * R_3 \quad (3)$$

Typical Applications (continued)

$V_{OUT} = (R_{SENSE} * I_{CHARGE}) * G$

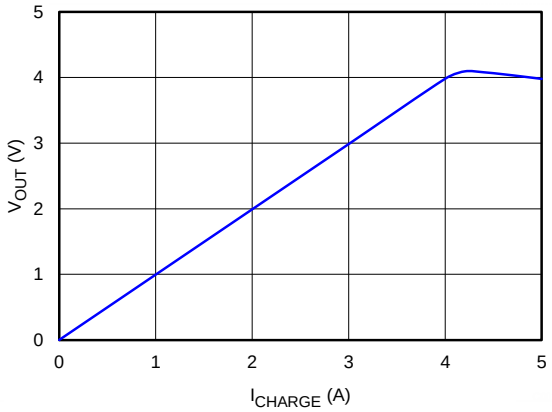
where

- $G = R_3 / R_1$ (4)

The other channel of the LMV93x may be used to buffer the voltage across R3 to drive the following stages.

8.2.1.3 Application Curve

Figure 31 shows the results of the example current sense circuit.



NOTE: the error after 4 V where transistor Q1 runs out of headroom and saturates, limiting the upper output swing.

Figure 31. Current Sense Amplifier Results

8.2.2 Half-Wave Rectifier Applications

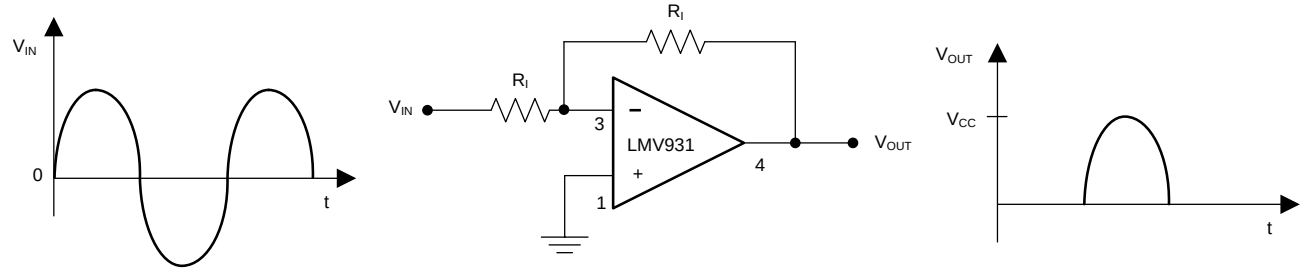


Figure 32. Half-Wave Rectifier With Rail-To-Ground Output Swing Referenced to Ground

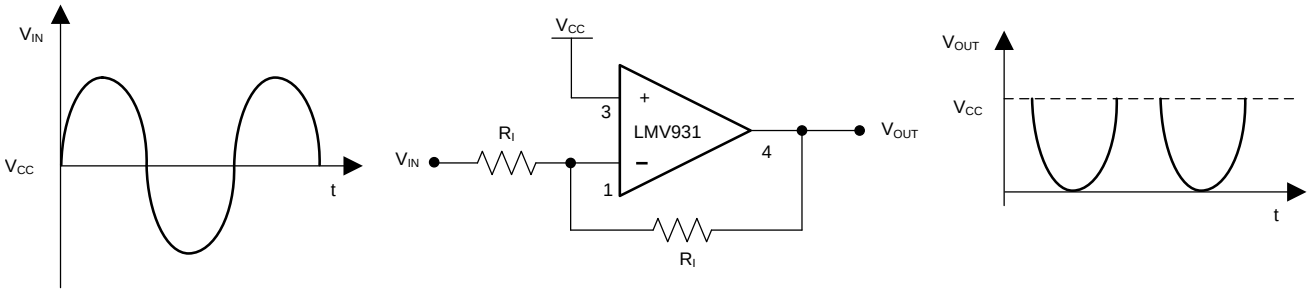


Figure 33. Half-Wave Rectifier With Negative-Going Output Referenced to V_{CC}

Typical Applications (continued)

8.2.2.1 Design Requirements

Because the LMV931-N, LMV932-N, LMV934-N input common-mode range includes both positive and negative supply rails and the output can also swing to either supply, achieving half-wave rectifier functions in either direction is an easy task. All that is needed are two external resistors; there is no need for diodes or matched resistors. The half-wave rectifier can have either positive or negative going outputs, depending on the way the circuit is arranged.

8.2.2.2 Detailed Design Procedure

In Figure 32 the circuit is referenced to ground, while in Figure 33 the circuit is biased to the positive supply. These configurations implement the half-wave rectifier because the LMV93x-N can not respond to one-half of the incoming waveform. It can not respond to one-half of the incoming because the amplifier cannot swing the output beyond either rail therefore the output disengages during this half cycle. During the other half cycle, however, the amplifier achieves a half wave that can have a peak equal to the total supply voltage. R_I should be large enough not to load the LMV93x-N.

8.2.2.3 Application Curve

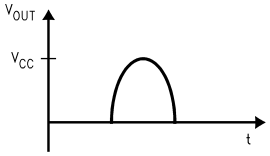


Figure 34. Output of Ground-to-Rail Circuit

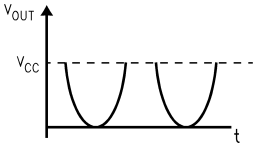


Figure 35. Output of Rail-to-Ground Circuit

8.2.3 Instrumentation Amplifier With Rail-to-Rail Input and Output Application

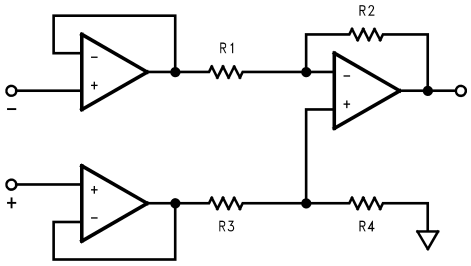


Figure 36. Rail-to-Rail Instrumentation Amplifier

8.2.3.1 Design Requirements

Using three of the LMV93x-N amplifiers, an instrumentation amplifier with rail-to-rail inputs and outputs can be made as shown in Figure 36.

8.2.3.2 Detailed Design Procedure

In this example, amplifiers on the left side act as buffers to the differential stage. These buffers assure that the input impedance is very high. They also assure that the difference amp is driven from a voltage source. This is necessary to maintain the CMRR set by the matching R_1-R_2 with R_3-R_4. The gain is set by the ratio of R_2/R_1 and R_3 should equal R_1 and R_4 equal R_2. With both rail-to-rail input and output ranges, the input and output are only limited by the supply voltages. Remember that even with rail-to-rail outputs, the output can not swing past the supplies so the combined common-mode voltages plus the signal should not be greater that the supplies or limiting will occur.

8.2.3.3 Application Curve

Figure 37 shows the results of the instrumentation amplifier with R_1 and R_3 = 1 K, and R_2 and R_4 = 100 kΩ, for a gain of 100, running on a single 5-V supply with a input of $V_{CM} = V_S/2$. The combined effects of the individual offset voltages can be seen as a shift in the offset of the curve.

Typical Applications (continued)

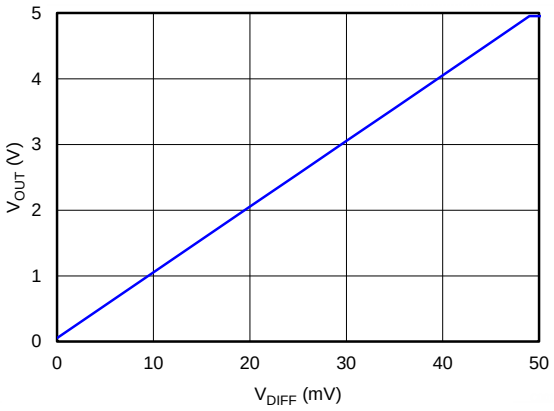


Figure 37. Instrumentation Amplifier Output Results

8.3 Dos and Don'ts

Do properly bypass the power supplies.

Do add series resistence to the output when driving capacitive loads, particularly cables, Muxes and ADC inputs.

Do add series current limiting resistors and external schottky clamp diodes if input voltage is expected to exceed the supplies. Limit the current to 1 mA or less (1 kΩ per volt).

9 Power Supply Recommendations

For proper operation, the power supplies must be properly decoupled. For decoupling the supply lines, TI recommends that 10-nF capacitors be placed as close as possible to the op amp power supply pins. For single-supply, place a capacitor between V^+ and V^- supply leads. For dual supplies, place one capacitor between V^+ and ground, and one capacitor between V^- and ground.

10 Layout

10.1 Layout Guidelines

The V^+ pin should be bypassed to ground with a low-ESR capacitor.

The optimum placement is closest to the V^+ and ground pins.

Take care to minimize the loop area formed by the bypass capacitor connection between V^+ and ground.

The ground pin should be connected to the PCB ground plane at the pin of the device.

The feedback components should be placed as close to the device as possible minimizing strays.

10.2 Layout Example

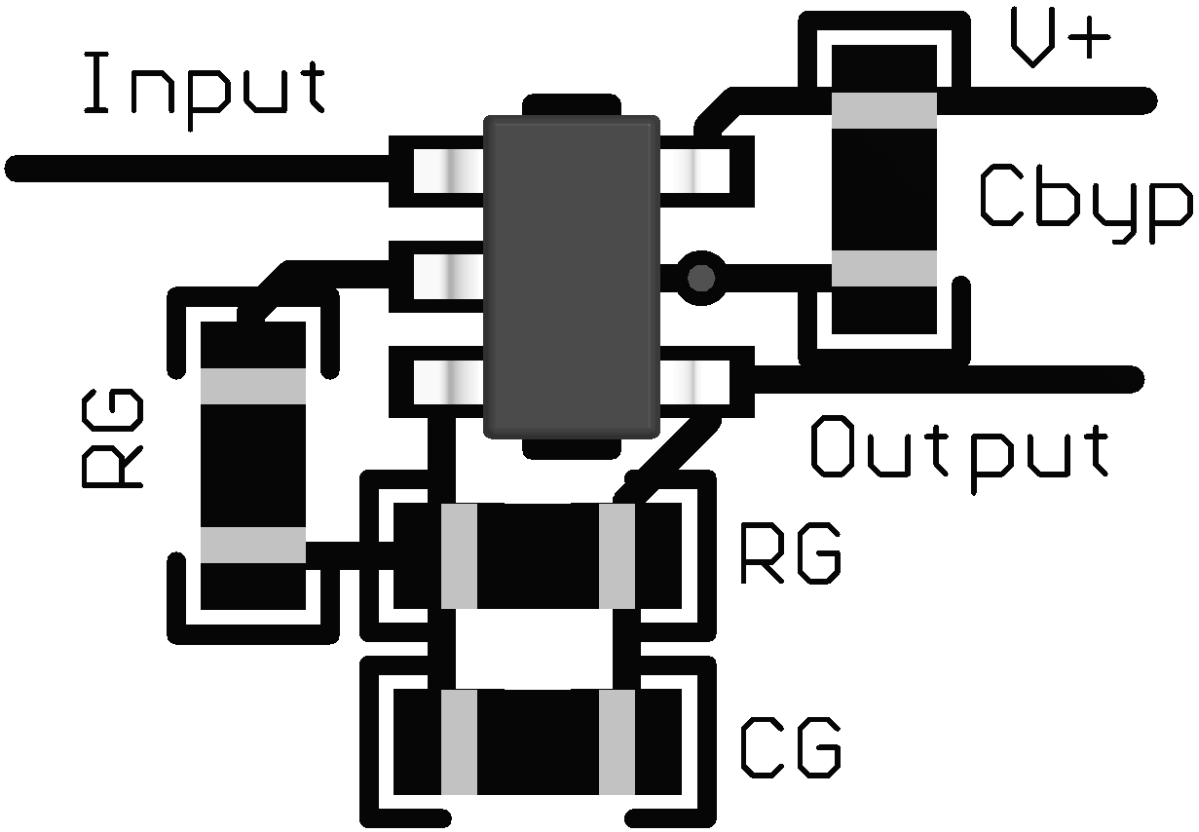


Figure 38. SOT-23 Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

LMV931 PSPICE Model (also applicable to the LMV932 and LMV934), http://www.ti.com/lit/zip/snom028

TINA-TI SPICE-Based Analog Simulation Program, http://www.ti.com/tool/tina-ti

DIP Adapter Evaluation Module, http://www.ti.com/tool/dip-adapter-evm

TI Universal Operational Amplifier Evaluation Module, http://www.ti.com/tool/opampevm

TI Filterpro Software, http://www.ti.com/tool/filterpro

11.2 Documentation Support

11.2.1 Related Documentation

For additional applications, see the following: *AN-31 Op Amp Circuit Collection*, SNLA140

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMV931-N	Click here	Click here	Click here	Click here	Click here
LMV931-N-Q1	Click here	Click here	Click here	Click here	Click here
LMV932-N	Click here	Click here	Click here	Click here	Click here
LMV932-N-Q1	Click here	Click here	Click here	Click here	Click here
LMV934-N	Click here	Click here	Click here	Click here	Click here
LMV934-N-Q1	Click here	Click here	Click here	Click here	Click here

11.4 Trademarks

All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV931MF	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	A79A	
LMV931MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	A79A	Samples
LMV931MFX	NRND	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125	A79A	
LMV931MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	A79A	Samples
LMV931MG	NRND	SC70	DCK	5	1000	TBD	Call TI	Call TI	-40 to 125	A74	
LMV931MG/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	A74	Samples
LMV931MGX/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	A74	Samples
LMV931Q1MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	ALAA	Samples
LMV931Q1MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	ALAA	Samples
LMV931Q1MG/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	BBA	Samples
LMV931Q1MGX/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	BBA	Samples
LMV932MA	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 125	LMV9 32MA	
LMV932MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMV9 32MA	Samples
LMV932MAX	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125	LMV9 32MA	
LMV932MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMV9 32MA	Samples
LMV932MM	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 125	A86A	
LMV932MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAUAG | CU SN	Level-1-260C-UNLIM	-40 to 125	A86A	Samples
LMV932MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU NIPDAUAG | CU SN	Level-1-260C-UNLIM	-40 to 125	A86A	Samples
LMV932Q1MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMV93 2Q1MA	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV932Q1MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMV93 2Q1MA	Samples
LMV934MA	NRND	SOIC	D	14	55	TBD	Call TI	Call TI	-40 to 125	LMV934MA	
LMV934MA/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMV934MA	Samples
LMV934MAX	NRND	SOIC	D	14		TBD	Call TI	Call TI	-40 to 125	LMV934MA	
LMV934MAX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMV934MA	Samples
LMV934MT/NOPB	ACTIVE	TSSOP	PW	14	94	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	LMV93 4MT	Samples
LMV934MTX	NRND	TSSOP	PW	14	2500	TBD	Call TI	Call TI	-40 to 125	LMV93 4MT	
LMV934MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	LMV93 4MT	Samples
LMV934Q1MT/NOPB	ACTIVE	TSSOP	PW	14	94	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMV934 Q1MT	Samples
LMV934Q1MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMV934 Q1MT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LMV931-N, LMV931-N-Q1, LMV932-N, LMV932-N-Q1, LMV934-N, LMV934-N-Q1 :

- Catalog: LMV931-N, LMV932-N, LMV934-N
- Automotive: LMV931-N-Q1, LMV932-N-Q1, LMV934-N-Q1

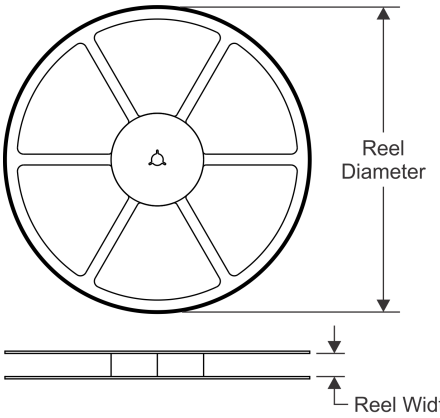
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

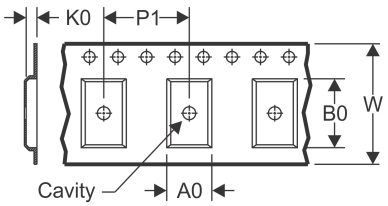
PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

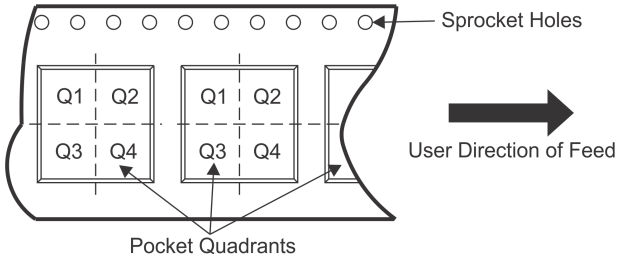


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



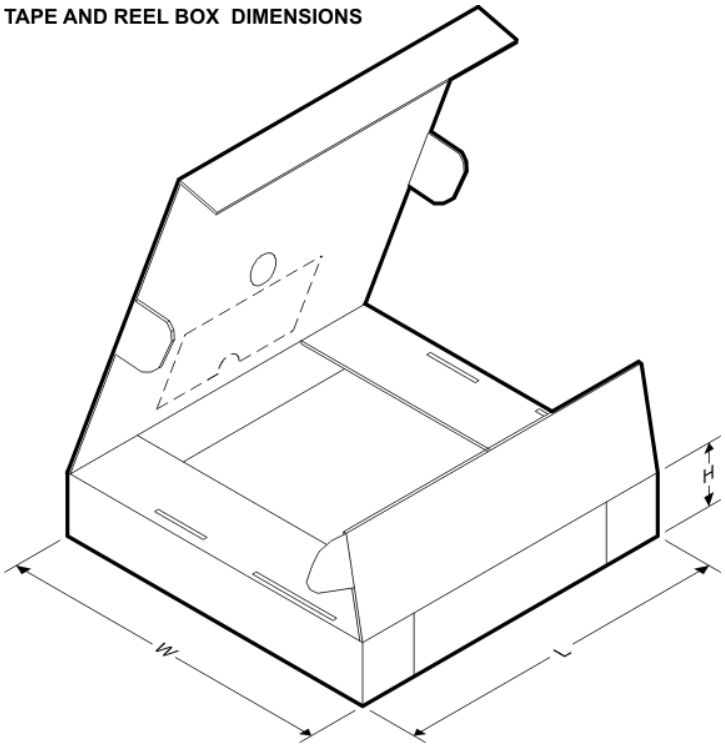
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV931MF	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV931MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV931MFX	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV931MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV931MG	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV931MG/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV931MGX/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV931Q1MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV931Q1MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV931Q1MG/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV931Q1MGX/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV932MAX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV932MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV932MM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV932MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV932MM/NOPB	VSSOP	DGK	8	1000	178.0	13.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV932MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV932MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV932Q1MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV934MAX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMV934MTX	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LMV934MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LMV934Q1MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

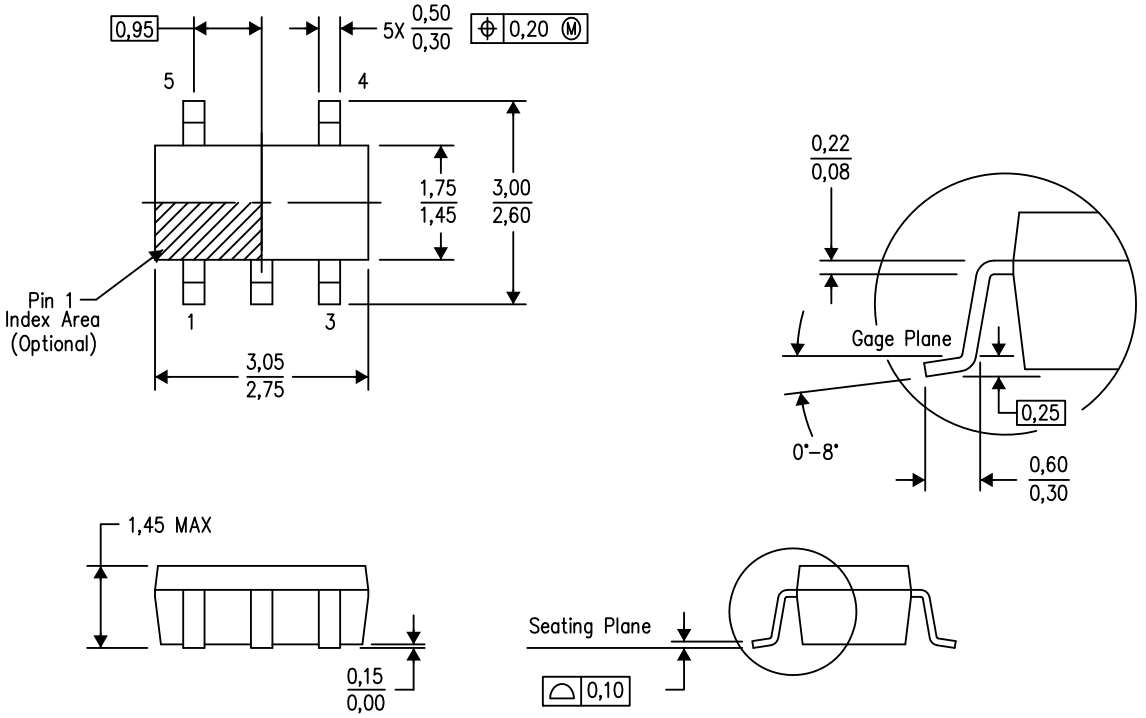
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV931MF	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV931MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV931MFX	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV931MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV931MG	SC70	DCK	5	1000	210.0	185.0	35.0
LMV931MG/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LMV931MGX/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0
LMV931Q1MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV931Q1MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV931Q1MG/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LMV931Q1MGX/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0
LMV932MAX	SOIC	D	8	2500	367.0	367.0	35.0

PACKAGE MATERIALS INFORMATION

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV932MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMV932MM	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMV932MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMV932MM/NOPB	VSSOP	DGK	8	1000	202.0	201.0	28.0
LMV932MMX/NOPB	VSSOP	DGK	8	3500	364.0	364.0	27.0
LMV932MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMV932Q1MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMV934MAX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
LMV934MTX	TSSOP	PW	14	2500	367.0	367.0	35.0
LMV934MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0
LMV934Q1MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0

MECHANICAL DATA

DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE

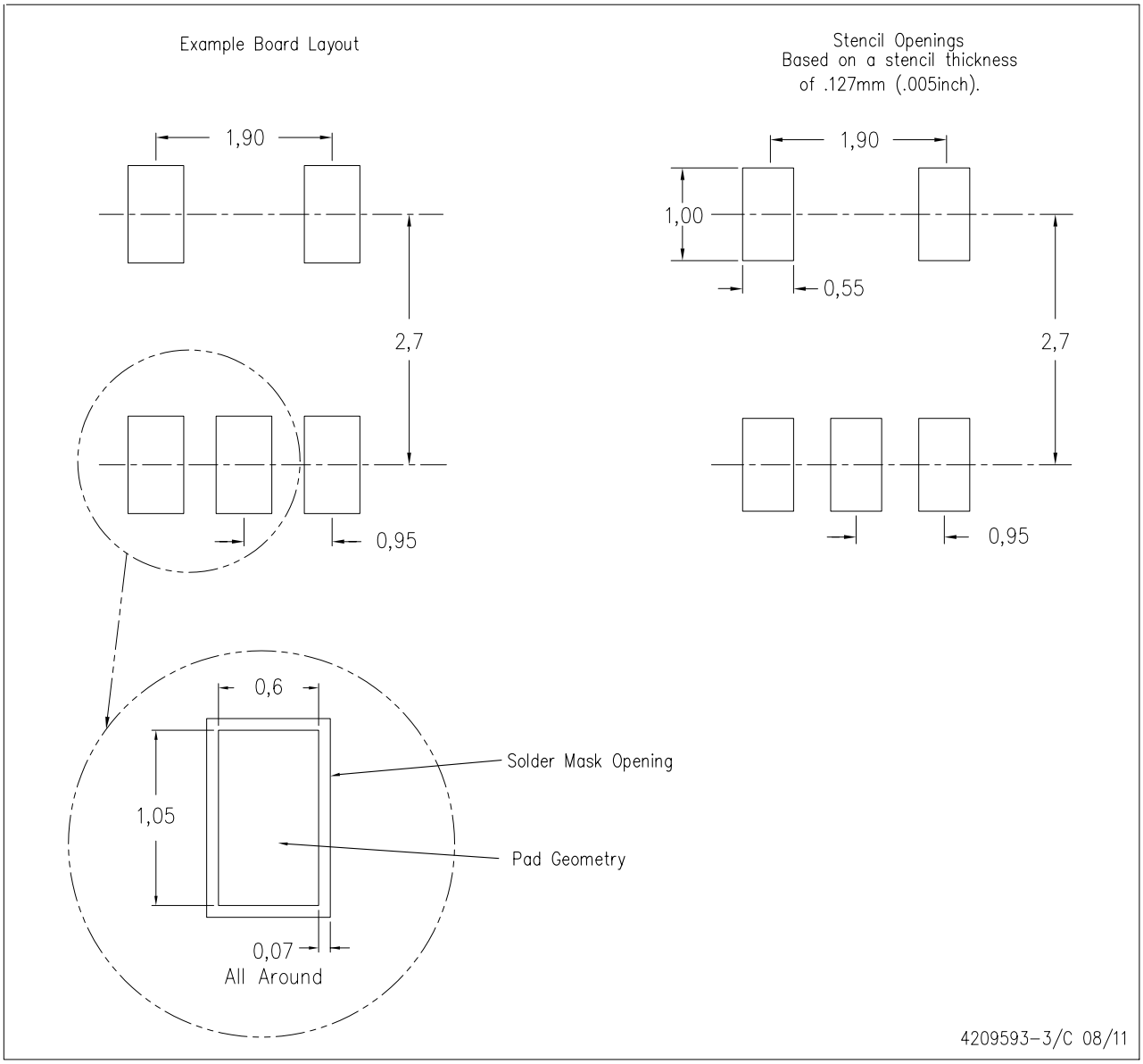


4073253–4/N 12/14

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

LAND PATTERN DATA

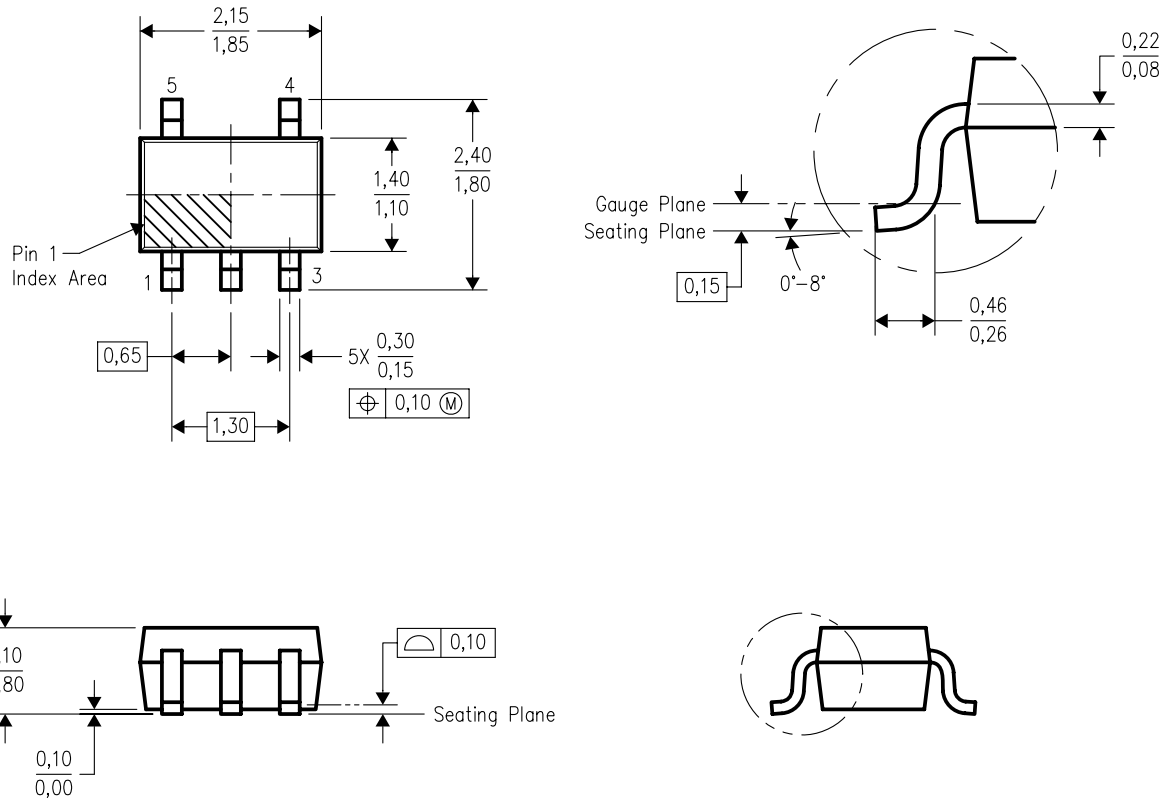
DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

MECHANICAL DATA

DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE

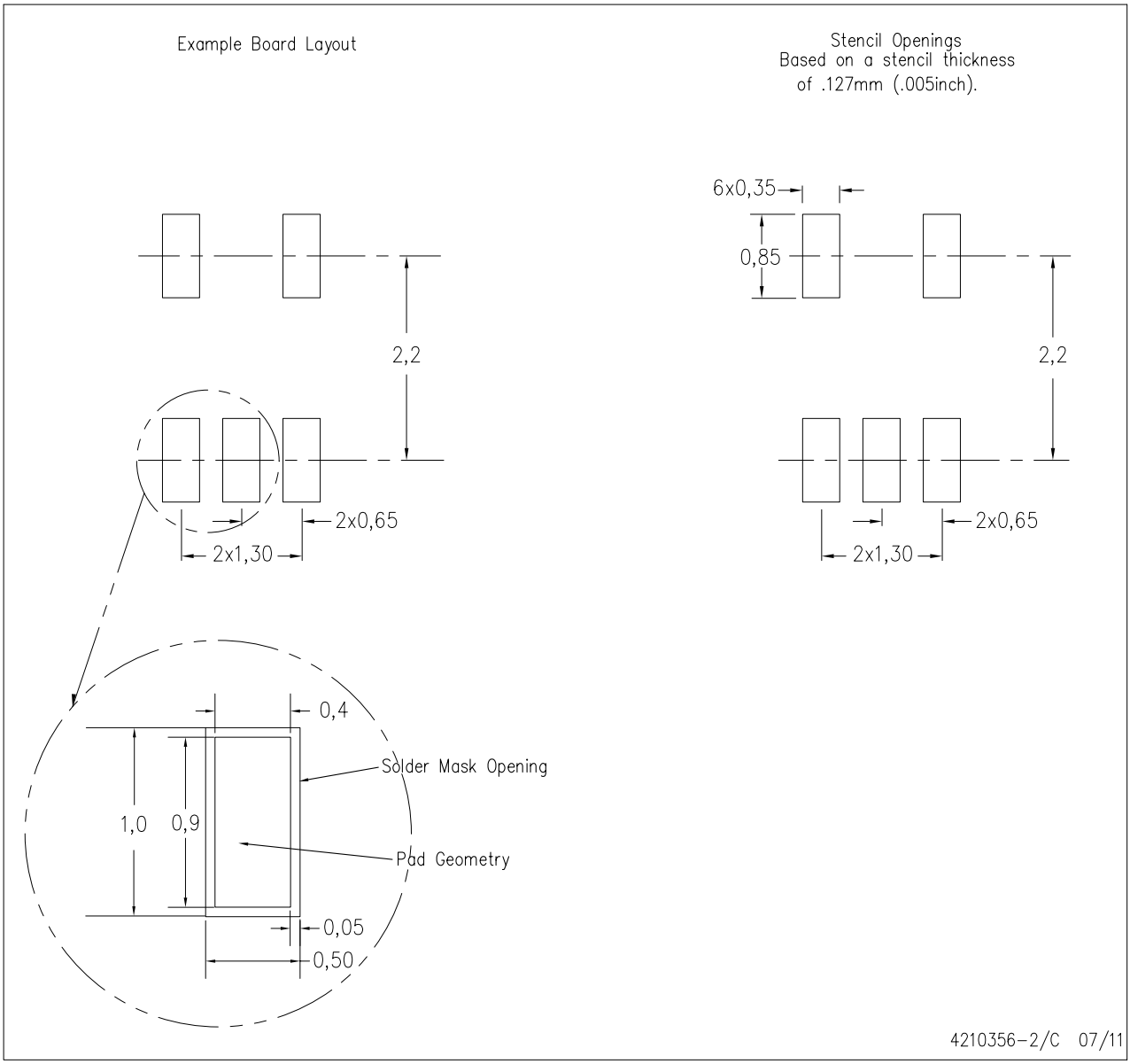


4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

LAND PATTERN DATA

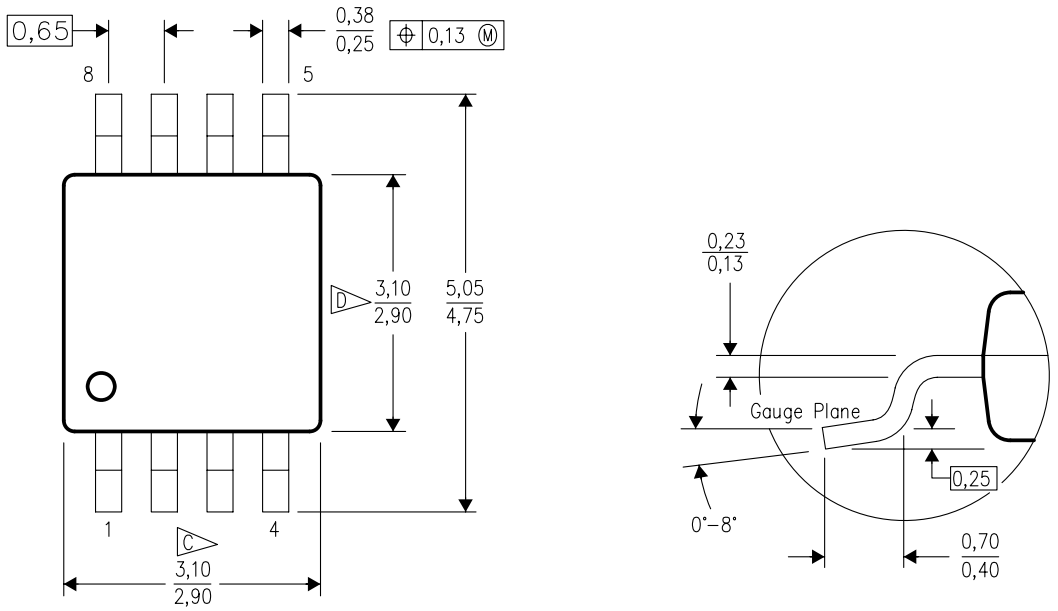
DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

MECHANICAL DATA

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE

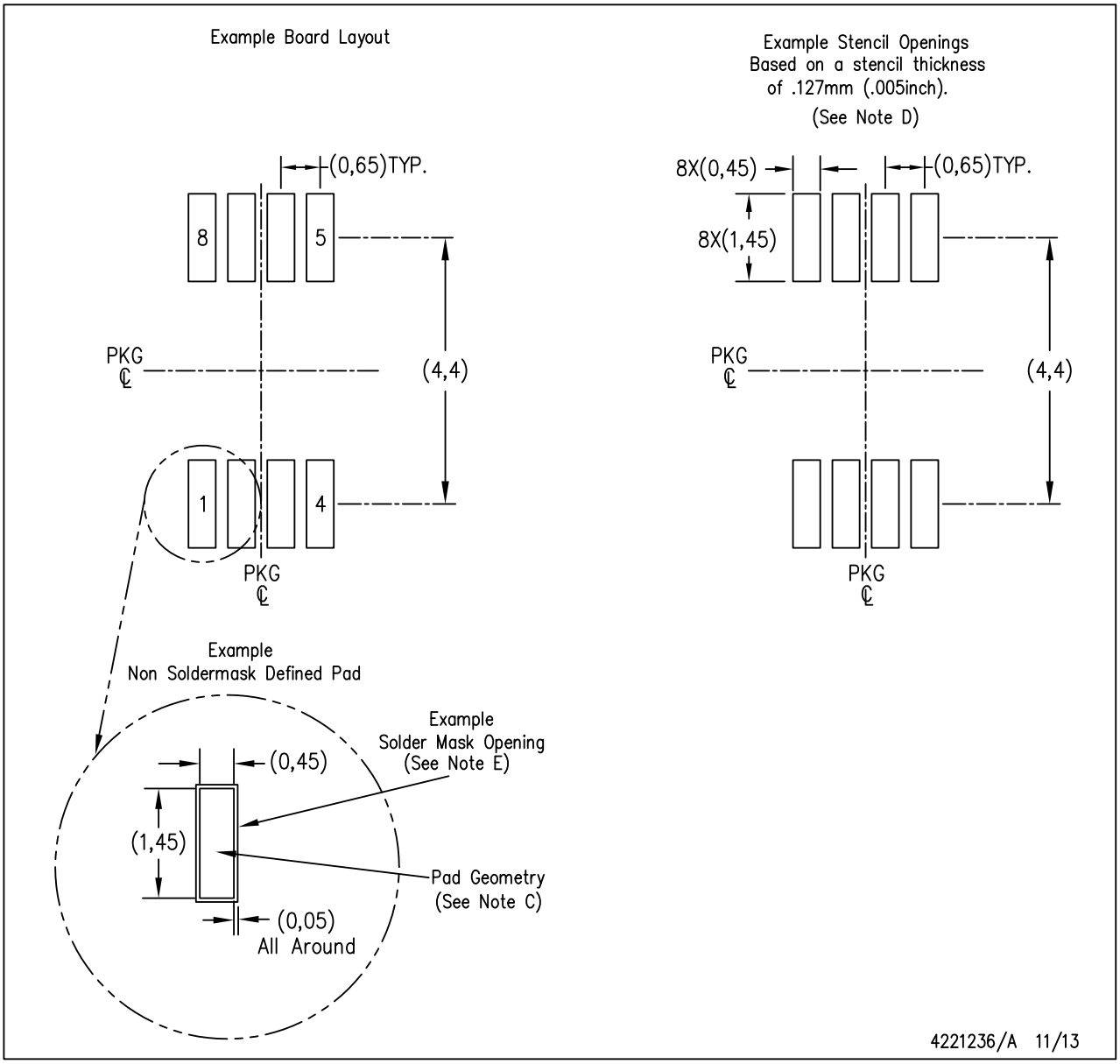


4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

LAND PATTERN DATA

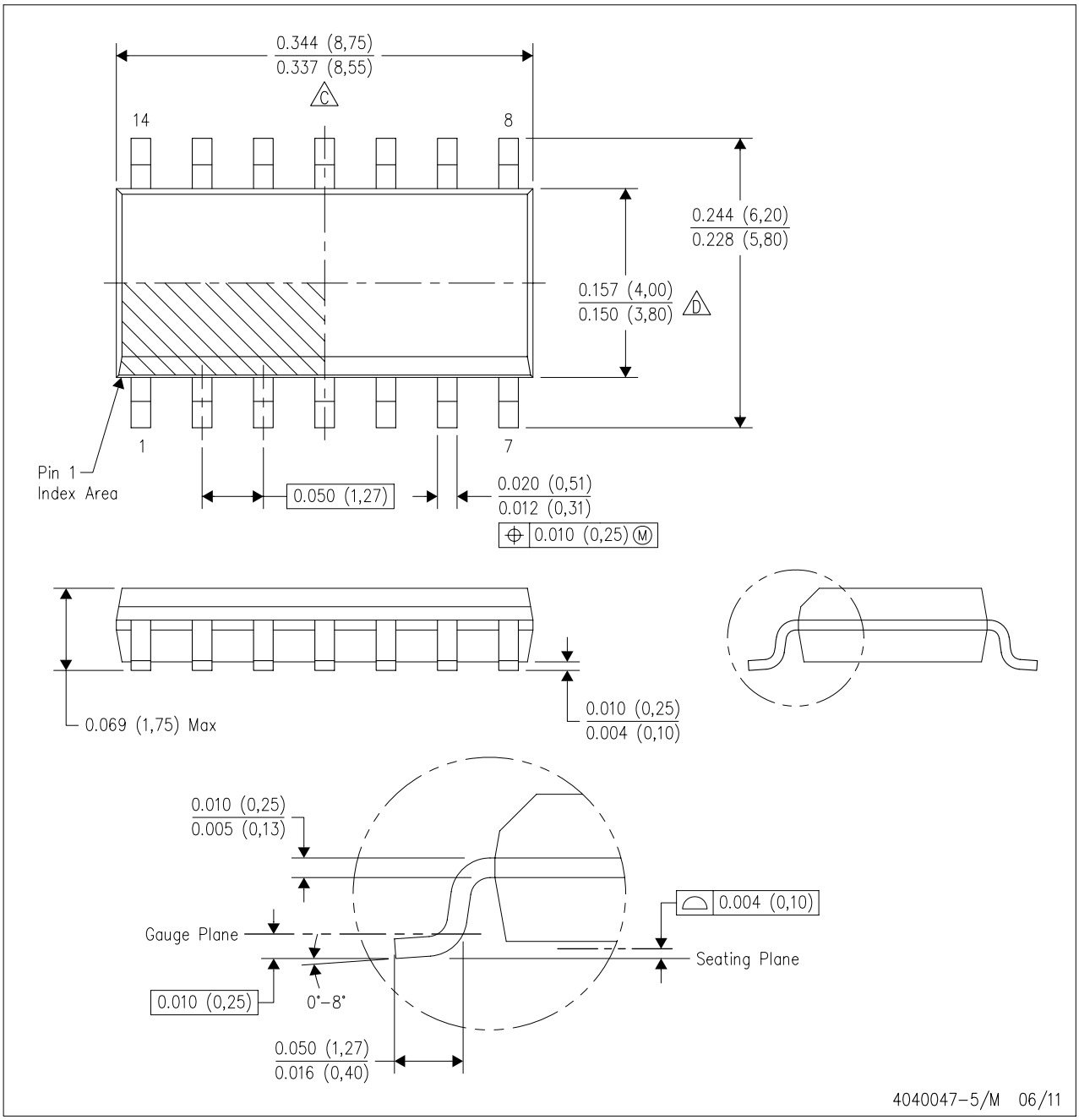
DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

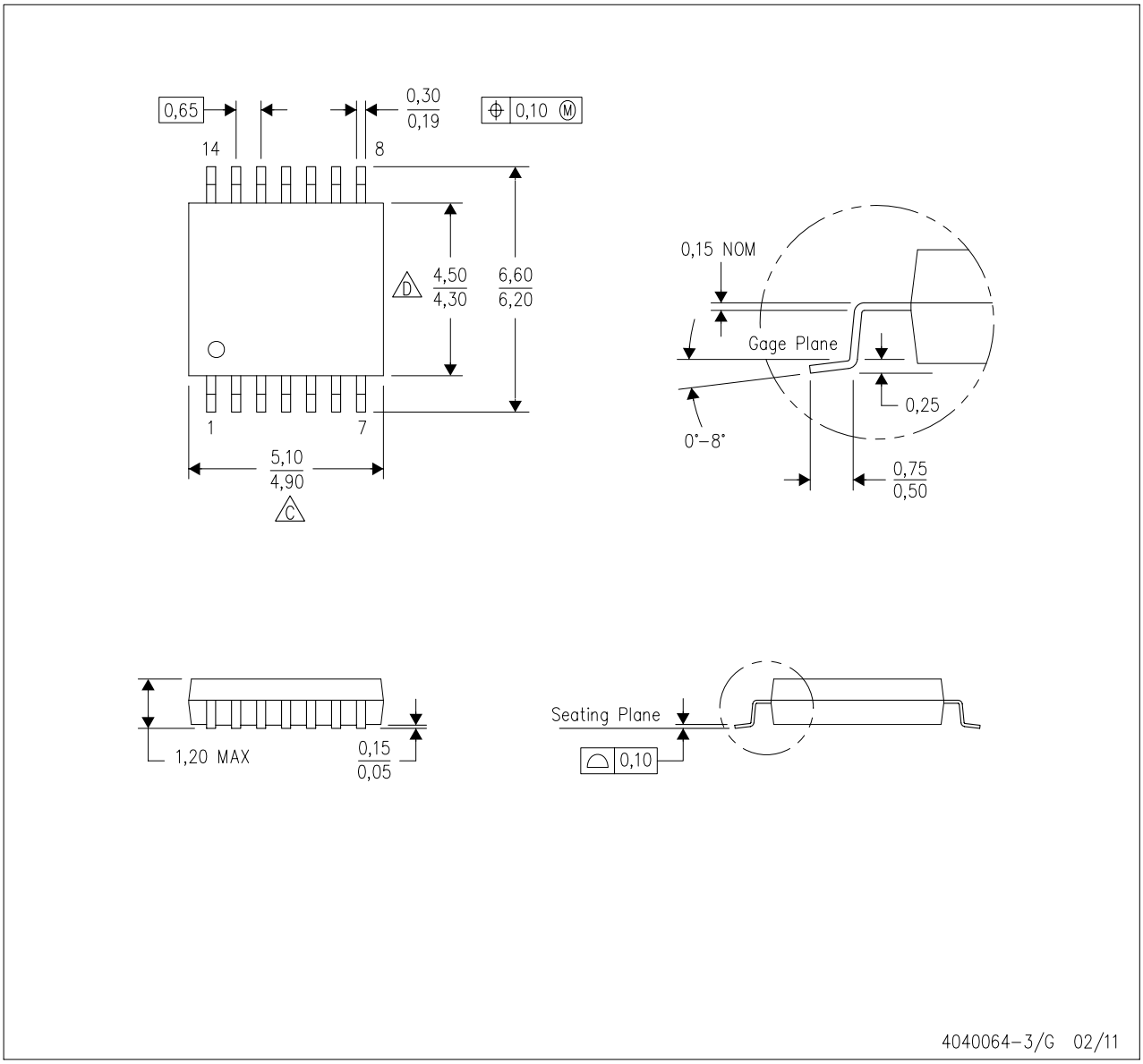
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

MECHANICAL DATA

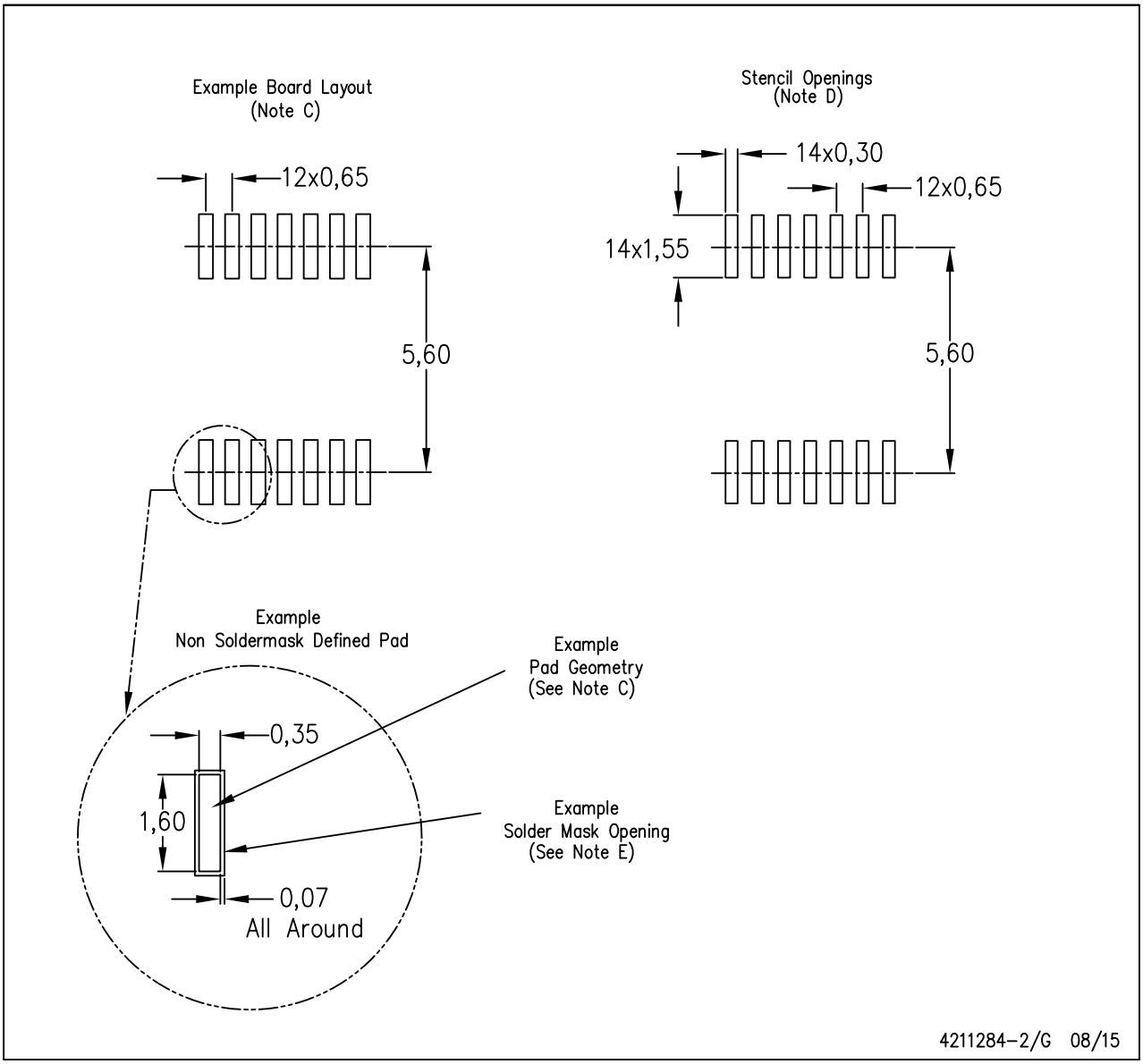
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

LAND PATTERN DATA

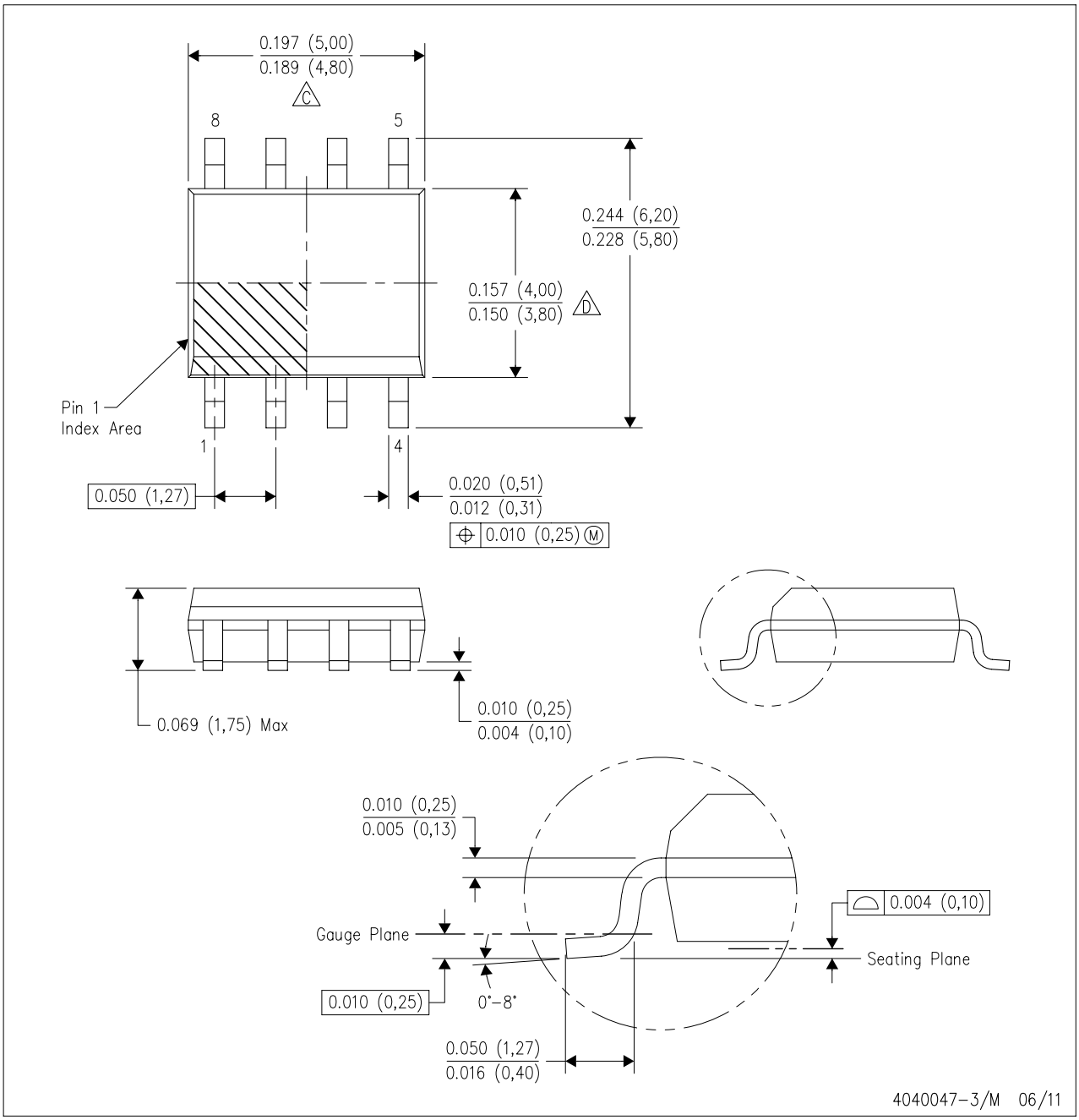
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265