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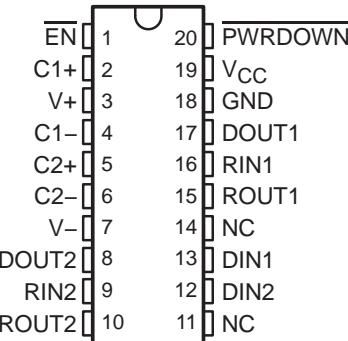
sales@integrated-circuit.com

**3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER
WITH $\pm 15\text{-kV ESD PROTECTION}$**

SLLS408G – JANUARY 2000 – REVISED MARCH 2004

- RS-232 Bus-Pin ESD Protection Exceeds $\pm 15\text{ kV}$ Using Human-Body Model (HBM)
- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards
- Operates With 3-V to 5.5-V V_{CC} Supply
- Operates Up To 250 kbit/s
- Two Drivers and Two Receivers
- Low Standby Current . . . 1 μA Typical
- External Capacitors . . . $4 \times 0.1\text{ }\mu\text{F}$
- Accepts 5-V Logic Input With 3.3-V Supply
- Alternative High-Speed Pin-Compatible Device (1 Mbit/s)
 - SNx5C3222
- Applications
 - Battery-Powered Systems, PDAs, Notebooks, Laptops, Palmtop PCs, and Hand-Held Equipment

**DB, DW, OR PW PACKAGE
(TOP VIEW)**



NC – No internal connection

description/ordering information

The MAX3222 consists of two line drivers, two line receivers, and a dual charge-pump circuit with $\pm 15\text{-kV ESD protection}$ pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The device operates at data signaling rates up to 250 kbit/s and a maximum of 30-V/ μs driver output slew rate.

ORDERING INFORMATION

T_A	PACKAGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
$-0^\circ\text{C to } 70^\circ\text{C}$	SOIC (DW)	Tube of 25	MAX3222CDW
		Reel of 2000	MAX3222CDWR
	SSOP (DB)	Tube of 70	MAX3222CDB
		Reel of 2000	MAX3222CDBR
	TSSOP (PW)	Tube of 70	MAX3222CPW
		Reel of 2000	MAX3222CPWR
$-40^\circ\text{C to } 85^\circ\text{C}$	SOIC (DW)	Tube of 25	MAX3222IDW
		Reel of 2000	MAX3222IDWR
	SSOP (DB)	Tube of 70	MAX3222IDB
		Reel of 2000	MAX3222IDBR
	TSSOP (PW)	Tube of 70	MAX3222IPW
		Reel of 2000	MAX3222IPWR

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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description/ordering information (continued)

The MAX3222 can be placed in the power-down mode by setting PWRDOWN low, which draws only $1\ \mu\text{A}$ from the power supply. When the device is powered down, the receivers remain active while the drivers are placed in the high-impedance state. Also, during power down, the onboard charge pump is disabled; V_+ is lowered to V_{CC} , and V_- is raised toward GND. Receiver outputs also can be placed in the high-impedance state by setting EN high.

Function Tables

EACH DRIVER

INPUTS		OUTPUT DOUT
DIN	<u>PWRDOWN</u>	
X	L	Z
L	H	H
H	H	L

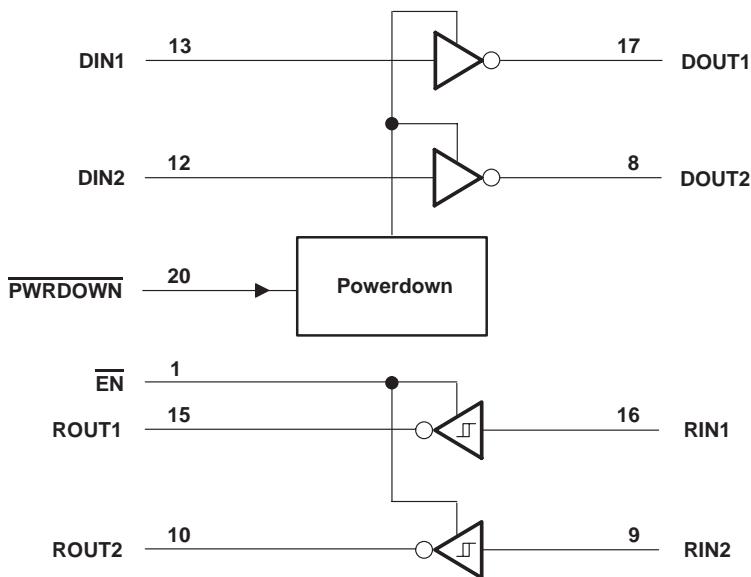
H = high level, L = low level, X = irrelevant,
 Z = high impedance

EACH RECEIVER

INPUTS		OUTPUT ROUT
RIN	<u>EN</u>	
L	L	H
H	L	L
X	H	Z
Open	L	H

H = high level, L = low level, X = irrelevant,
 Z = high impedance (off), Open = input
 disconnected or connected driver off

logic diagram (positive logic)



MAX3222 3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER WITH $\pm 15\text{-kV}$ ESD PROTECTION

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to network GND.

1. All voltages are with respect to ground (GND).
2. Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4 and Figure 5)

			MIN	NOM	MAX	UNIT
Supply voltage	V _{CC} = 3.3 V		3	3.3	3.6	V
	V _{CC} = 5 V		4.5	5	5.5	
V _{IH}	Driver and control high-level input voltage	DIN, EN, PWRDOWN	V _{CC} = 3.3 V	2		V
			V _{CC} = 5 V	2.4		
V _{IL}	Driver and control low-level input voltage	DIN, EN, PWRDOWN		0.8		V
V _I	Driver and control input voltage	DIN, EN, PWRDOWN		0	5.5	V
V _I	Receiver input voltage			-25	25	V
T _A	Operating free-air temperature	MAX3222C		0	70	°C
		MAX3222I		-40	85	

NOTE 4: Test conditions are C1–C4 = 0.1 μ F at $V_{CC} = 3.3$ V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at $V_{CC} = 5$ V \pm 0.5 V.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 5)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I _I Input leakage current (EN, PWRDOWN)			±0.01		±1	µA
I _{CC}	Supply current	No load, PWRDOWN at V _{CC}	0.3		1	mA
	Supply current (powered off)	No load, PWRDOWN at GND	1		10	µA

[†] All typical values are at $V_{CC} = 3.3$ V or $V_{CC} = 5$ V, and $T_A = 25^\circ\text{C}$.

NOTE 4: Test conditions are C1–C4 = 0.1 μF at $V_{\text{CC}} = 3.3\text{ V} \pm 0.3\text{ V}$; C1 = 0.047 μF , C2–C4 = 0.33 μF at $V_{\text{CC}} = 5\text{ V} \pm 0.5\text{ V}$.

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DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 5)

PARAMETER	TEST CONDITIONS	MIN	TYPT [†]	MAX	UNIT
V _{OH}	High-level output voltage DOUT at R _L = 3 k Ω to GND, DIN = GND	5	5.4		V
V _{OL}	Low-level output voltage DOUT at R _L = 3 k Ω to GND, DIN = V _{CC}	-5	-5.4		V
I _{IH}	High-level input current V _I = V _{CC}		± 0.01	± 1	μA
I _{IL}	Low-level input current V _I at GND		± 0.01	± 1	μA
I _{OS}	Short-circuit output current [‡] V _{CC} = 3.6 V, V _O = 0 V V _{CC} = 5.5 V, V _O = 0 V		± 35	± 60	mA
r _o	Output resistance V _{CC} , V ₊ , and V ₋ = 0 V, V _O = ± 2 V	300	10M		Ω
I _{off}	PWRDOWN = GND, V _O = ± 12 V, V _{CC} = 3 V to 3.6 V			± 25	μA
	PWRDOWN = GND, V _O = ± 10 V, V _{CC} = 4.5 V to 5.5 V			± 25	

[†] All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

[‡] Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.

NOTE 4: Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF , C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 5)

PARAMETER	TEST CONDITIONS	MIN	TYPT [†]	MAX	UNIT
Maximum data rate	C _L = 1000 pF, R _L = 3 k Ω , One DOUT switching, See Figure 1	150	250		kbit/s
t _{sk(p)}	Pulse skew [§] C _L = 150 pF to 2500 pF, R _L = 3 k Ω to 7 k Ω , See Figure 2		300		ns
SR(tr)	R _L = 3 k Ω to 7 k Ω , V _{CC} = 3.3 V	C _L = 150 pF to 1000 pF	6	30	V/ μs
		C _L = 150 pF to 2500 pF	4	30	

[†] All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

[§] Pulse skew is defined as |t_{PLH} – t_{PHL}| of each channel of the same device.

NOTE 4: Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF , C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 5)

PARAMETER		TEST CONDITIONS	MIN	TYPT [†]	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = -1 mA	V _{CC} – 0.6 V	V _{CC} – 0.1 V		V
V _{OL}	Low-level output voltage	I _{OL} = 1.6 mA			0.4	V
V _{IT+}	Positive-going input threshold voltage	V _{CC} = 3.3 V		1.5	2.4	V
		V _{CC} = 5 V		1.8	2.4	
V _{IT-}	Negative-going input threshold voltage	V _{CC} = 3.3 V	0.6	1.2		V
		V _{CC} = 5 V	0.8	1.5		
V _{hys}	Input hysteresis (V _{IT+} – V _{IT-})			0.3		V
I _{off}	Output leakage current	EN = V _{CC}		± 0.05	± 10	μA
r _i	Input resistance	V _I = $\pm 3\text{ V}$ to $\pm 25\text{ V}$	3	5	7	$\text{k}\Omega$

[†] All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

NOTE 4: Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF , C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4)

PARAMETER		TEST CONDITIONS	MIN	TYPT [†]	MAX	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	C _L = 150 pF, See Figure 3		300		ns
t _{PHL}	Propagation delay time, high- to low-level output	C _L = 150 pF, See Figure 3		300		ns
t _{en}	Output enable time	C _L = 150 pF, R _L = 3 k Ω , See Figure 4		200		ns
t _{dis}	Output disable time	C _L = 150 pF, R _L = 3 k Ω , See Figure 4		200		ns
t _{sk(p)}	Pulse skew [‡]	See Figure 3		300		ns

[†] All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

[‡] Pulse skew is defined as |t_{PLH} – t_{PHL}| of each channel of the same device.

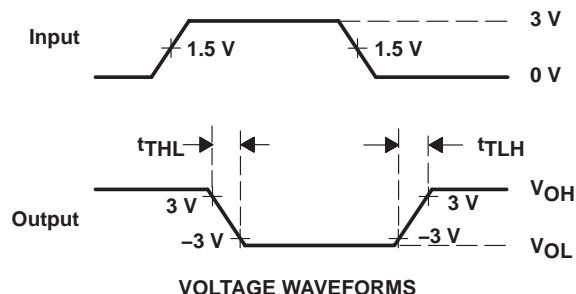
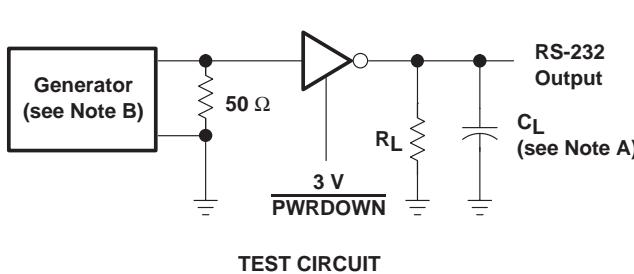
NOTE 4: Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF , C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

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PARAMETER MEASUREMENT INFORMATION

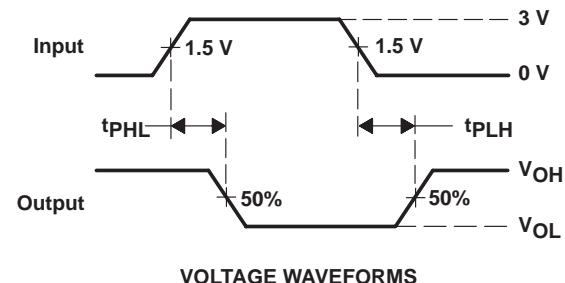
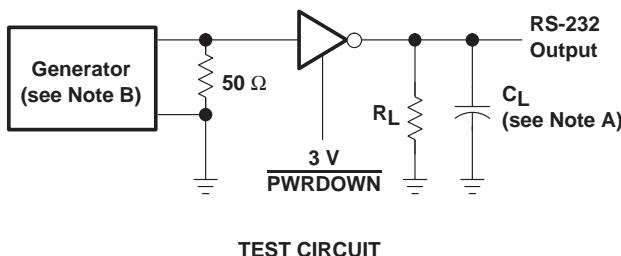


$$SR(tr) = \frac{6\text{ V}}{t_{THL} \text{ or } t_{TLH}}$$

NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50\text{ }\Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

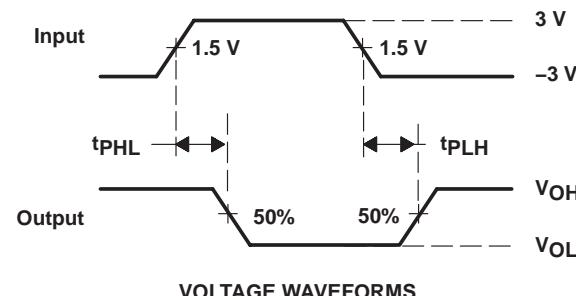
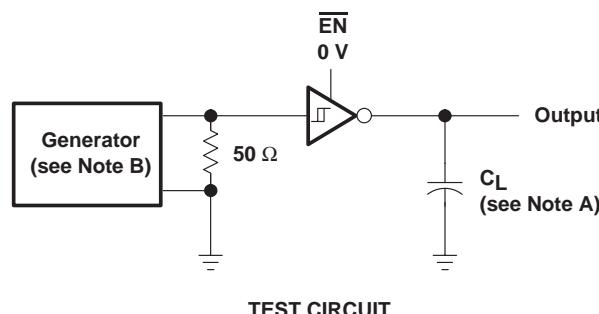
Figure 1. Driver Slew Rate



NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50\text{ }\Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 2. Driver Pulse Skew

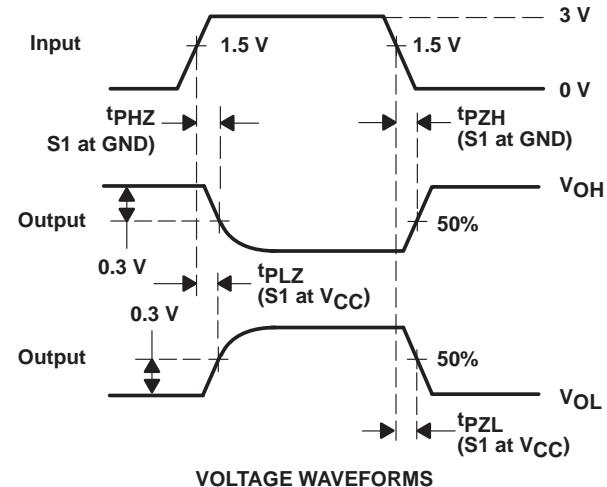
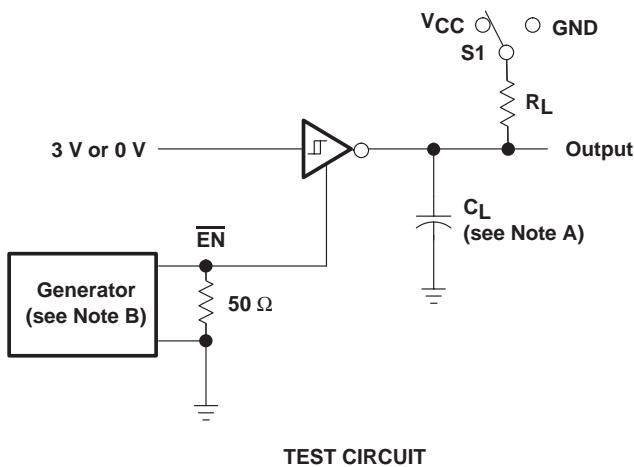


NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: $Z_O = 50\text{ }\Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 3. Receiver Propagation Delay Times

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.

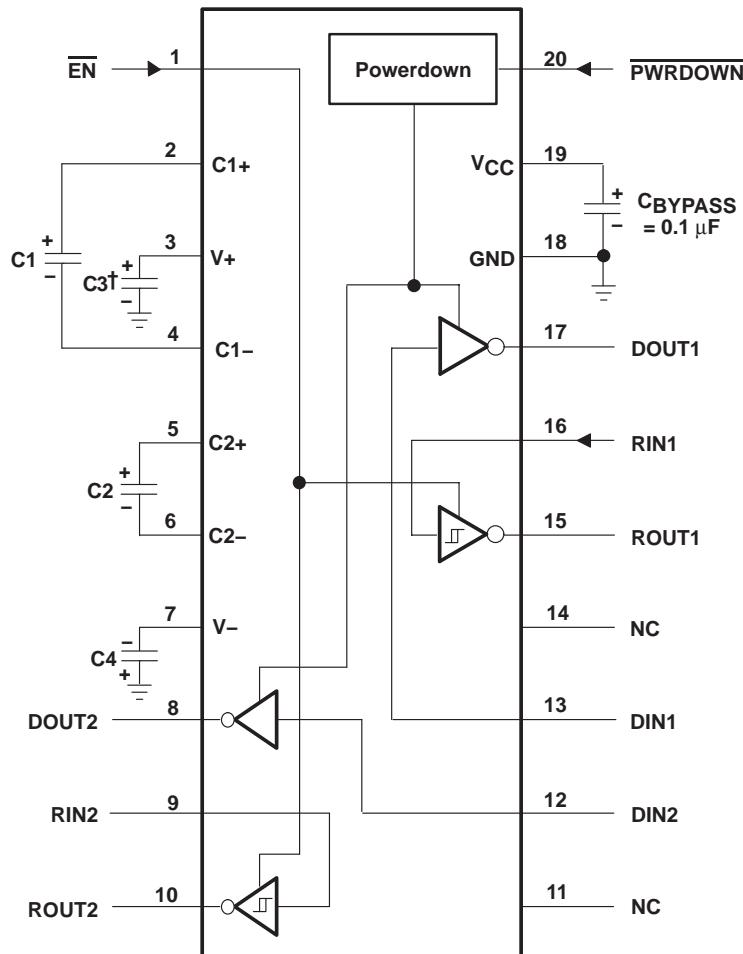
Figure 4. Receiver Enable and Disable Times

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APPLICATION INFORMATION



† C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. NC – No internal connection

C. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

V _{CC}	C1	C2, C3, and C4
3.3 V ± 0.3 V	0.1 μF	0.1 μF
5 V ± 0.5 V	0.047 μF	0.33 μF
3 V to 5.5 V	0.1 μF	0.47 μF

Figure 5. Typical Operating Circuit and Capacitor Values

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MAX3222CDB	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3222C	Samples
MAX3222CDBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3222C	Samples
MAX3222CDBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3222C	Samples
MAX3222CDBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3222C	Samples
MAX3222CDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3222C	Samples
MAX3222CDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3222C	Samples
MAX3222CDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3222C	Samples
MAX3222CDWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3222C	Samples
MAX3222CPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3222C	Samples
MAX3222CPWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3222C	Samples
MAX3222CPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3222C	Samples
MAX3222CPWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3222C	Samples
MAX3222IDB	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3222I	Samples
MAX3222IDBG4	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3222I	Samples
MAX3222IDBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3222I	Samples
MAX3222IDBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3222I	Samples
MAX3222IDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3222I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MAX3222IDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3222I	Samples
MAX3222IDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3222I	Samples
MAX3222IPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3222I	Samples
MAX3222IPWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3222I	Samples
MAX3222IPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3222I	Samples
MAX3222IPWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3222I	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "—" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

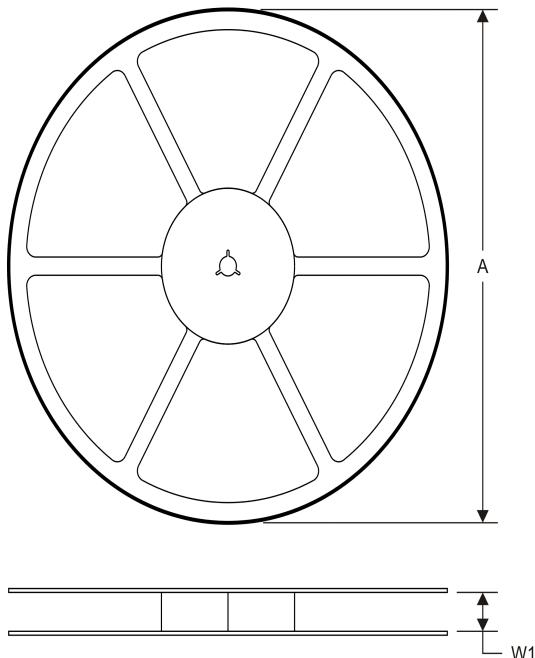
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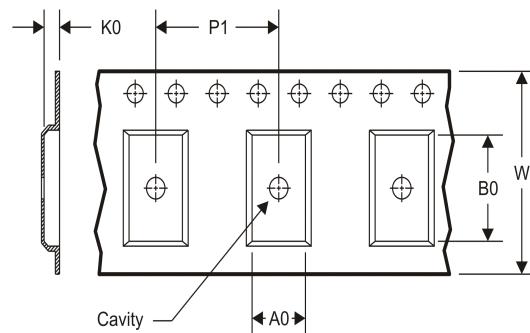
PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



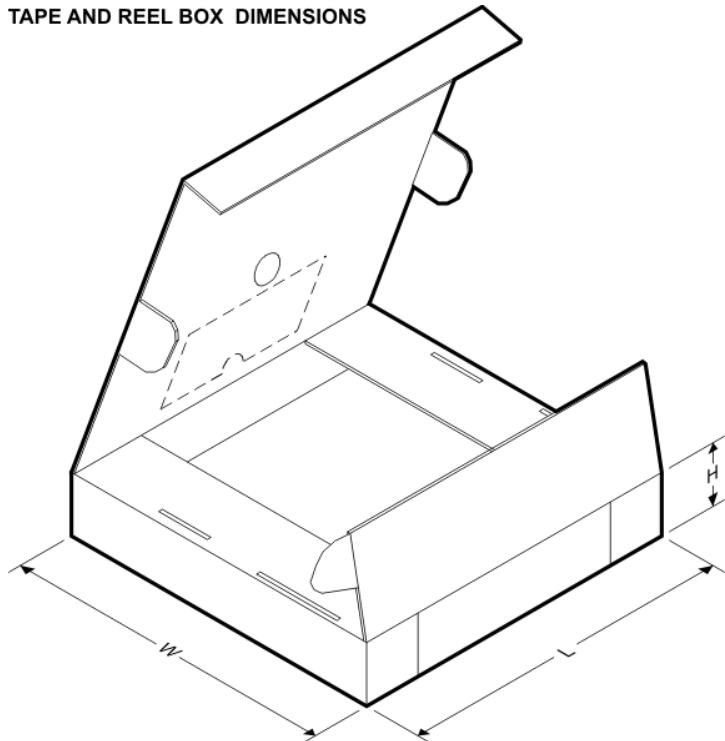
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX3222CDBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
MAX3222CDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
MAX3222CPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MAX3222IDBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
MAX3222IDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
MAX3222IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX3222CDBR	SSOP	DB	20	2000	367.0	367.0	38.0
MAX3222CDWR	SOIC	DW	20	2000	367.0	367.0	45.0
MAX3222CPWR	TSSOP	PW	20	2000	367.0	367.0	38.0
MAX3222IDBR	SSOP	DB	20	2000	367.0	367.0	38.0
MAX3222IDWR	SOIC	DW	20	2000	367.0	367.0	45.0
MAX3222IPWR	TSSOP	PW	20	2000	367.0	367.0	38.0

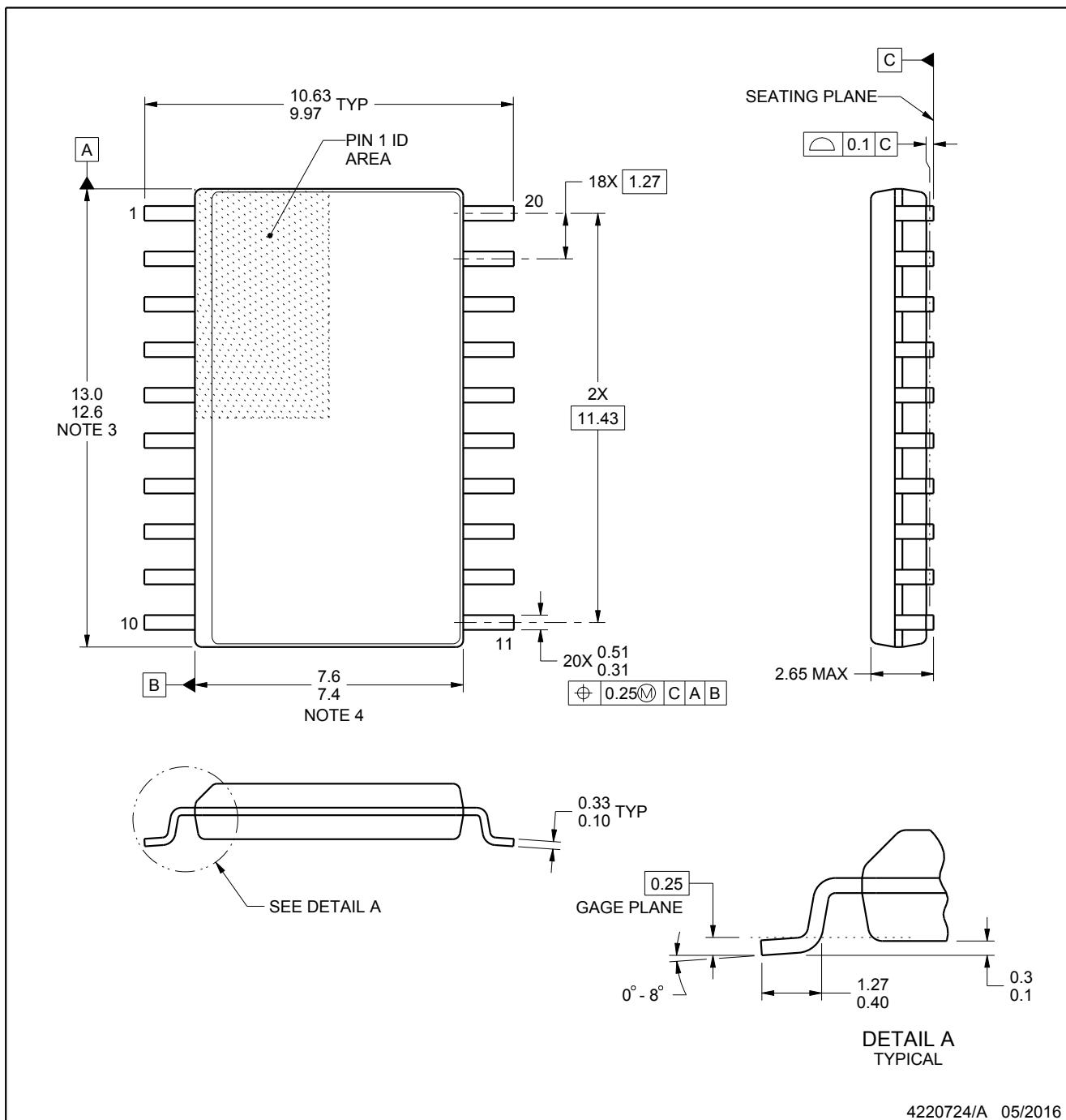


PACKAGE OUTLINE

DW0020A

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

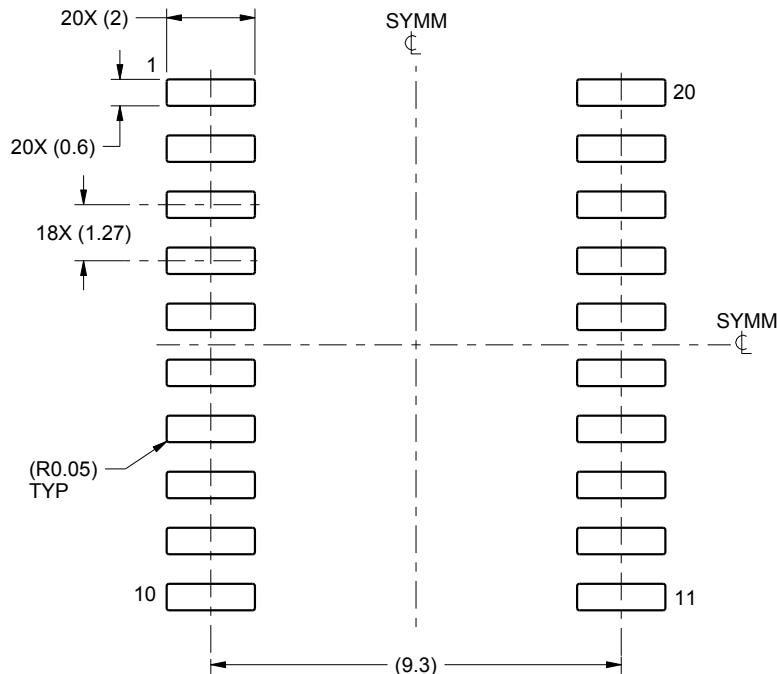
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

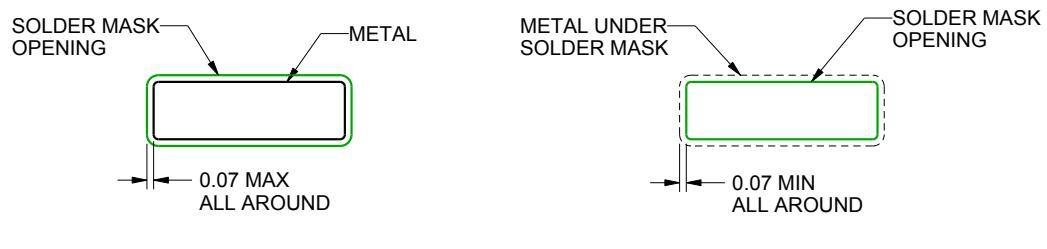
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

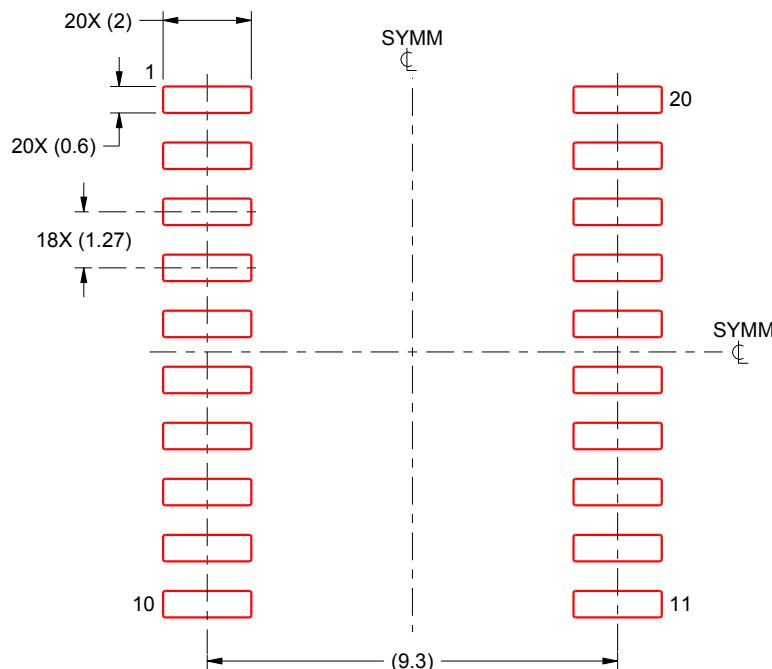
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

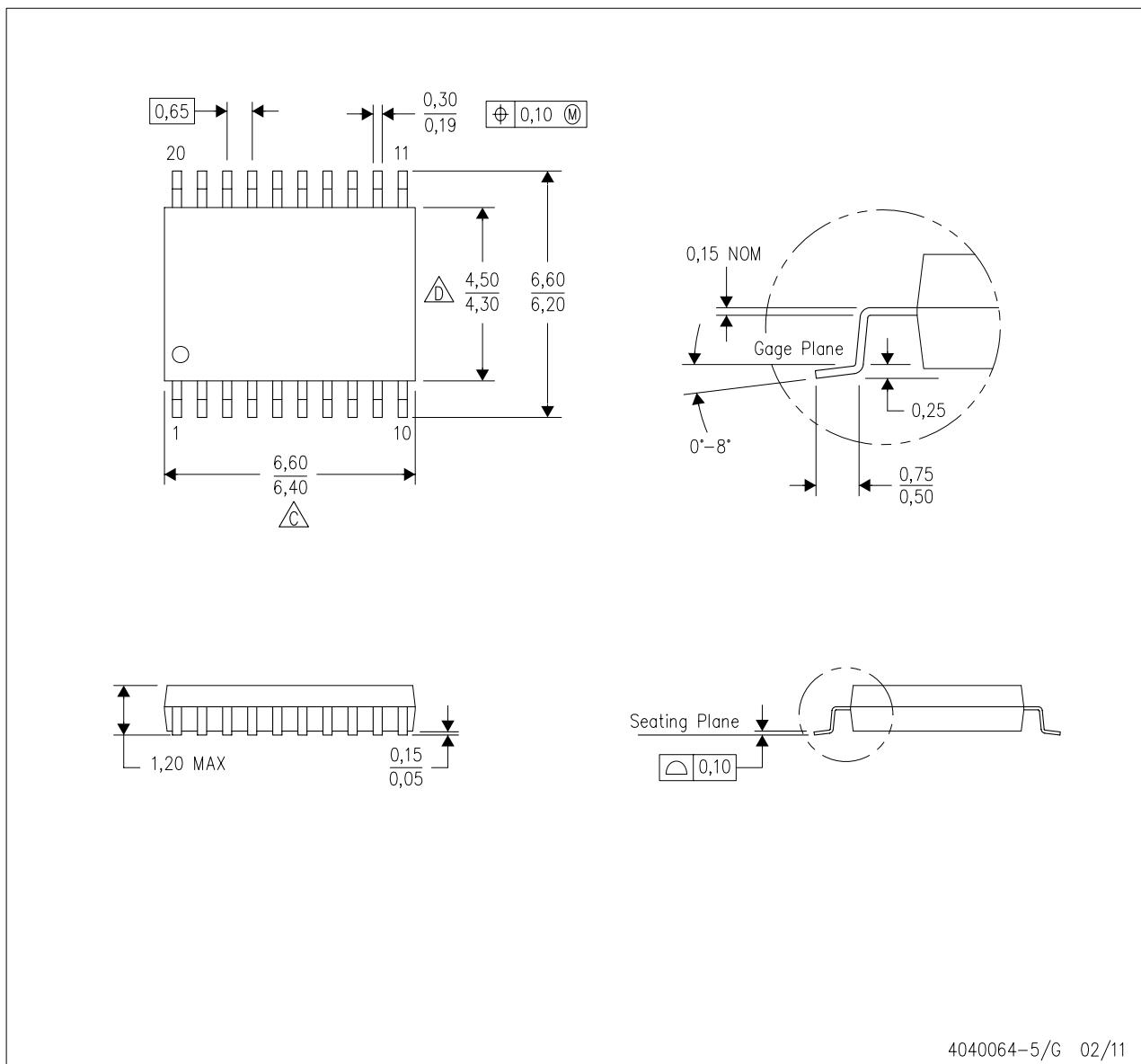
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4040064-5/G 02/11

NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
-  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
-  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153

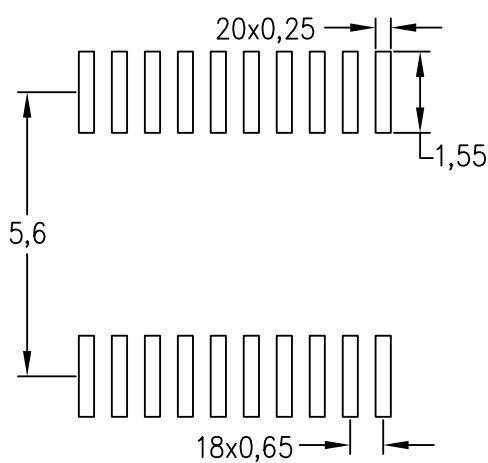
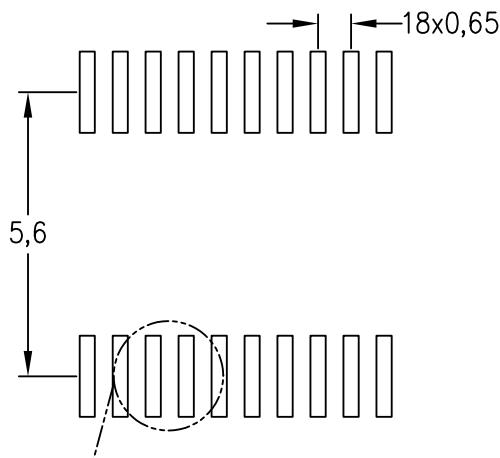
LAND PATTERN DATA

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

Example Board Layout

Based on a stencil thickness
of .127mm (.005inch).



Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note E)

Pad Geometry



4211284-5/G 08/15

NOTES:

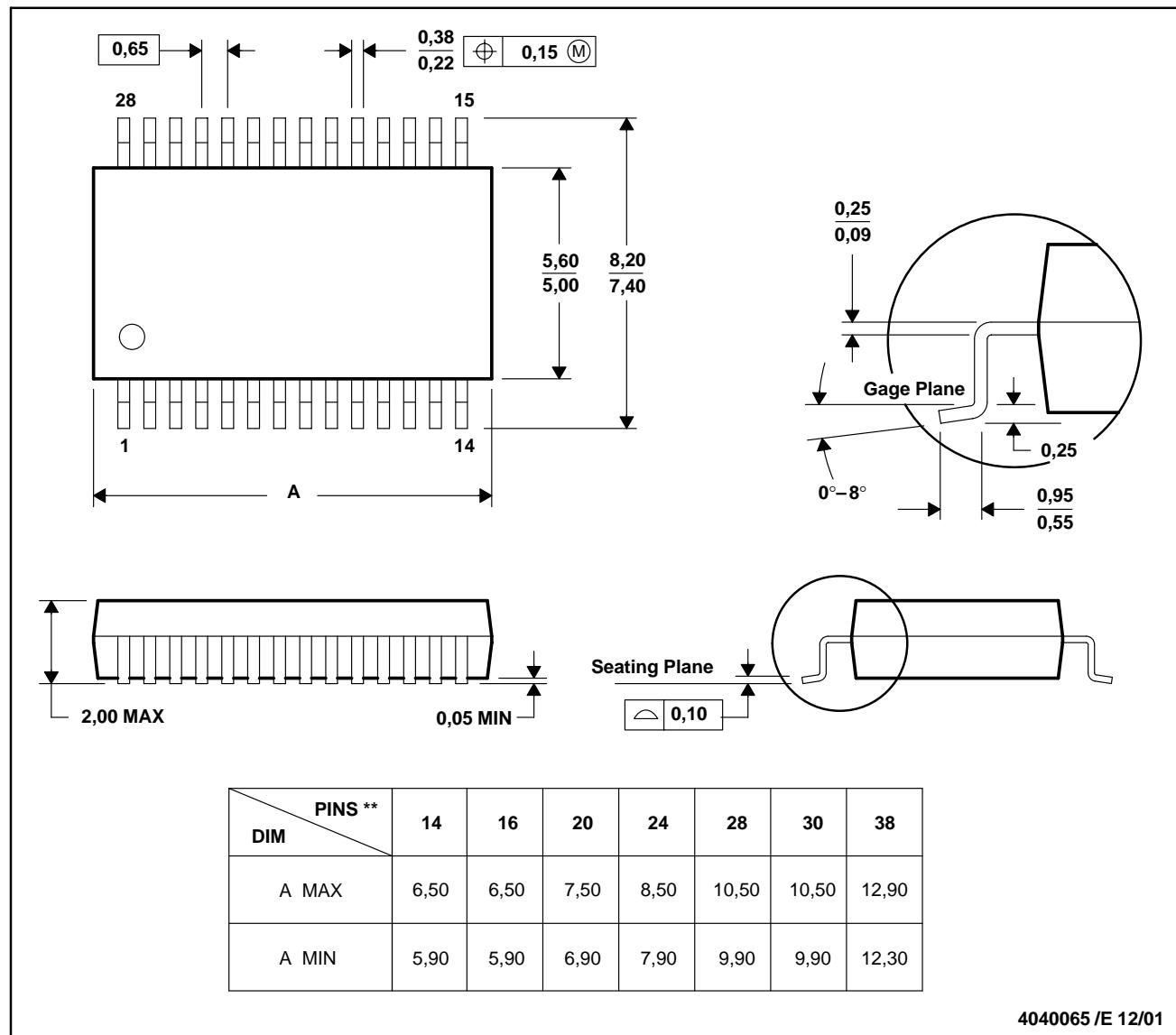
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MSS002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)**

28 PINS SHOWN

PLASTIC SMALL-OUTLINE



4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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