

Excellent Integrated System Limited

Stocking Distributor

Click to view price, real time Inventory, Delivery & Lifecycle Information:

[Texas Instruments](#)

[PCM1772PW](#)

For any questions, you can email us directly:

sales@integrated-circuit.com



Burr-Brown Products
from Texas Instruments

PCM1772, PCM1773

SLES010G – SEPTEMBER 2001 – REVISED MARCH 2007

LOW-VOLTAGE AND LOW-POWER STEREO AUDIO DIGITAL-TO-ANALOG CONVERTER WITH LINEOUT AMPLIFIER

FEATURES

- Multilevel DAC Including Lineout Amplifier
- Analog Performance (V_{CC1} , $V_{CC2} = 2.4\text{ V}$):
 - Dynamic Range: 98 dB Typ
 - THD+N at 0 dB: 0.007% Typ
- 1.6-V to 3.6-V Single Power Supply
- Low Power Dissipation:
6 mW at V_{CC1} , $V_{CC2} = 2.4\text{ V}$
- System Clock: 128 f_s , 192 f_s , 256 f_s , 384 f_s
- Sampling Frequency: 5 kHz to 50 kHz
- Software Control (PCM1772):
 - 16-, 20-, 24-Bit Word Available
 - Left-, Right-Justified, and I²S
 - Slave/Master Selectable
 - Digital Attenuation: 0 dB to –62 dB, 1 dB/Step
 - 44.1-kHz Digital De-Emphasis
 - Zero Cross Attenuation
 - Digital Soft Mute
 - Monaural Analog-In With Mixing
 - Monaural Speaker Mode
- Hardware Control (PCM1773):
 - Left-Justified and I²S
 - 44.1-kHz Digital De-Emphasis
 - Monaural Analog-In With Mixing
- Pop-Noise-Free Circuit
- 3.3-V Tolerant
- Packages: TSSOP-16 and VQFN-20

APPLICATIONS

- Portable Audio Player
- Cellular Phone
- PDA
- Other Applications Requiring Low-Voltage Operation

DESCRIPTION

The PCM1772 and PCM1773 devices are CMOS, monolithic, integrated circuits which include stereo digital-to-analog converters, lineout circuitry, and support circuitry in small TSSOP-16 and VQFN-20 packages.

The data converters use TI's enhanced multilevel Δ - Σ architecture, which employs noise shaping and multilevel amplitude quantization to achieve excellent dynamic performance and improved tolerance to clock jitter. The PCM1772 and PCM1773 devices accept several industry standard audio data formats with 16- to 24-bit data, left-justified, I²S, etc., providing easy interfacing to audio DSP and decoder devices. Sampling rates up to 50 kHz are supported. A full set of user-programmable functions is accessible through a 3-wire serial control port, which supports register write functions.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PCM1772, PCM1773

SLES010G–SEPTEMBER 2001–REVISED MARCH 2007



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted⁽¹⁾

	PCM1772 PCM1773
Supply voltage: V_{CC1} , V_{CC2}	–0.3 V to 4 V
Supply voltage differences: V_{CC1} , V_{CC2}	±0.1 V
Ground voltage differences	±0.1 V
Digital input voltage	–0.3 V to 4 V
Input current (any terminals except supplies)	±10 mA
Operating temperature	–40°C to 125°C
Storage temperature	–55°C to 150°C
Junction temperature	150°C
Lead temperature (soldering)	260°C, 5 s
Package temperature (IR reflow, peak)	260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range

	MIN	NOM	MAX	UNIT
Supply voltage: V_{CC1} , V_{CC2}	1.6	2.4	3.6	V
Digital input logic family	CMOS			
Digital input clock frequency	System clock	0.64	19.2	MHz
	Sampling clock	5	50	kHz
Analog output load resistance	10			kΩ
Analog input level ($V_{CC2} = 2.4$ V)			1.4	Vp-p
Operating free-air temperature, T_A	–25		85	°C

ELECTRICAL CHARACTERISTICS

all specifications at $T_A = 25^\circ\text{C}$, $V_{CC1} = V_{CC2} = 2.4\text{ V}$, $f_S = 44.1\text{ kHz}$, system clock = $256 f_S$ and 24-bit data, $R_L = 10\text{ k}\Omega$, unless otherwise noted

PARAMETER		TEST CONDITIONS	PCM1772PW, PCM1773PW, PCM1772RGA, PCM1773RGA			UNIT
			MIN	TYP	MAX	
Resolution			24			Bits
OPERATING FREQUENCY						
Sampling frequency (f _S)			5		50	kHz
System clock frequency			128 f _S , 192 f _S , 256 f _S , 384 f _S			
DIGITAL INPUT/OUTPUT ⁽¹⁾⁽²⁾						
V _{IH}	Input logic level		0.7 V _{CC1}			V _{dc}
V _{IL}			0.3 V _{CC1}			V _{dc}
I _{IH}	Input logic current	V _{IN} = V _{CC1}	10			μA
I _{IL}		V _{IN} = 0 V	−10			μA
V _{OH}	Output logic level ⁽³⁾	I _{OH} = −2 mA	0.7 V _{CC1}			V _{dc}
V _{OL}		I _{OL} = 2 mA	0.3 V _{CC1}			V _{dc}
DYNAMIC PERFORMANCE (LINE OUTPUT)						
Full-scale output voltage		0 dB	0.77 V _{CC2}			V _{P-P}
Dynamic range		EIAJ, A-weighted	90	98		dB
Signal-to-noise ratio		EIAJ, A-weighted	90	98		dB
THD+N		0 dB	0.007% 0.015%			
Channel separation			70	80		dB
Load resistance			10			kΩ
DC ACCURACY						
Gain error			±2 ±8			% of FSR
Gain mismatch, channel-to-channel			±2 ±8			% of FSR
Bipolar zero error		V _{OUT} = 0.5 V _{CC1} at BPZ	±30 ±75			mV
ANALOG LINE INPUT (MIXING CIRCUIT)						
Analog input voltage range			0.584 V _{CC2}			V _{P-P}
Gain (analog input to line output)			0.91			
Analog input impedance			10			kΩ
THD+N		A _{IN} = 0.56 V _{CC2} (peak-to-peak)	0.1%			
DIGITAL FILTER PERFORMANCE						
Pass band			0.454 f _S			
Stop band			0.546 f _S			
Pass-band ripple			±0.04			dB
Stop-band attenuation			−50			dB
Group delay			20/f _S			
44.1-kHz de-emphasis error			±0.1			dB
ANALOG FILTER PERFORMANCE						
Frequency response		at 20 kHz	±0.2			dB

- (1) Digital inputs and outputs are CMOS compatible.
(2) All logic inputs are 3.3-V tolerant and not terminated internally.
(3) LRCK and BCK terminals

PCM1772, PCM1773

SLES010G–SEPTEMBER 2001–REVISED MARCH 2007

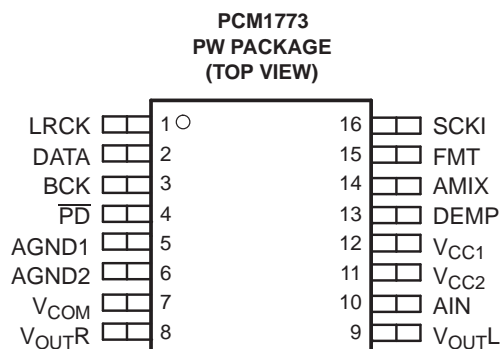
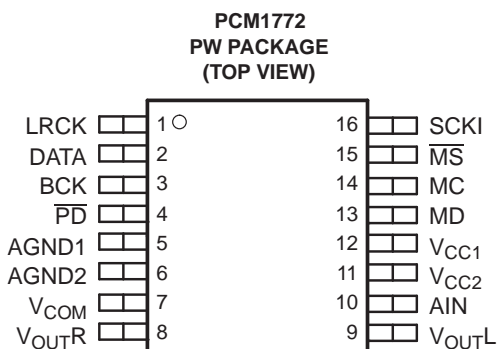
ELECTRICAL CHARACTERISTICS (continued)

all specifications at $T_A = 25^\circ\text{C}$, $V_{CC1} = V_{CC2} = 2.4\text{ V}$, $f_S = 44.1\text{ kHz}$, system clock = $256 f_S$ and 24-bit data, $R_L = 10\text{ k}\Omega$, unless otherwise noted

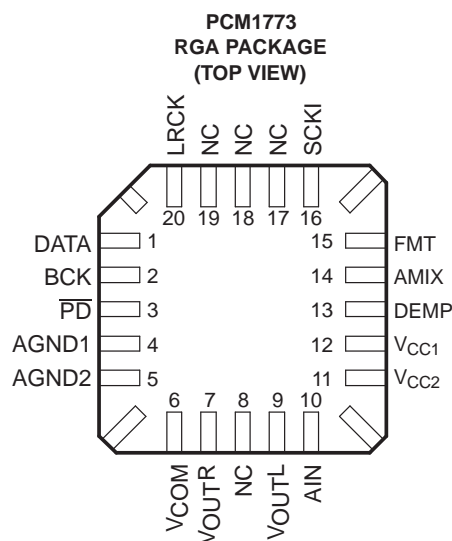
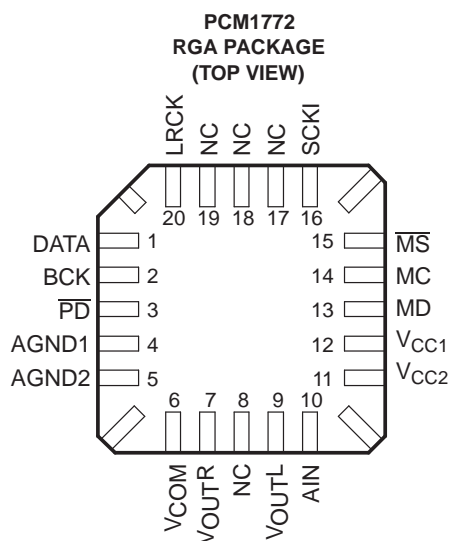
PARAMETER		TEST CONDITIONS	PCM1772PW, PCM1773PW, PCM1772RGA, PCM1773RGA			UNIT
			MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS						
Voltage range, V _{CC1} , V _{CC2}			1.6	2.4	3.6	Vdc
I _{CC1}	Supply current	BPZ input		1.5	2.5	mA
I _{CC2}		BPZ input		1	2.5	
I _{CC1} + I _{CC2}			Power down ⁽⁴⁾		5	15
Power dissipation		BPZ input		6	12	mW
		Power down ⁽⁴⁾		12	36	μW
TEMPERATURE RANGE						
Operation temperature			-25		85	°C
θ _{JA}	Thermal resistance	PCM1772PW, -73PW: 16-terminal TSSOP		150		°C/W
		PCM1772RGA, -73RGA: 20-terminal VQFN		130		

(4) All input signals are held static.

PIN ASSIGNMENTS



P0001-01



NC – No internal connection

P0002-01

TERMINAL FUNCTIONS

PCM1772PW

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND1	5	—	Analog ground. This is a return for V_{CC1} .
AGND2	6	—	Analog ground. This is a return for V_{CC2} .
AIN	10	I	Monaural analog signal mixer input. The signal can be mixed with the output of the L- and R-channel DACs.
BCK	3	I/O	Serial bit clock. Clocks the individual bits of the audio data input, DATA. In the slave interface mode, this clock is input from an external device. In master interface mode, the PCM1772 device generates the BCK output to an external device.
DATA	2	I	Serial audio data input
LRCK	1	I/O	Left and right clock. Determines which channel is being input on the audio data input, DATA. The frequency of LRCK must be the same as the audio sampling rate. In the slave interface mode, this clock is input from an external device. In the master interface mode, the PCM1772 device generates the LRCK output to an external device.
MC	14	I	Mode control port serial bit clock input. Clocks the individual bits of the control data input, MD.
MD	13	I	Mode control port serial data input. Controls the operation mode on the PCM1772 device.
\overline{MS}	15	I	Mode control port select. The control port is active when this terminal is low.
\overline{PD}	4	I	Reset input. When low, the PCM1772 device is powered down, and all mode control registers are reset to default settings.
SCKI	16	I	System clock input
V_{CC1}	12	—	Power supply for all analog circuits except the lineout amplifier.
V_{CC2}	11	—	Analog power supply for the lineout amplifier circuits. The voltage level must be the same as V_{CC1} .
V_{COM}	7	—	Decoupling capacitor connection. An external 10- μ F capacitor connected from this terminal to analog ground is required for noise filtering. Voltage level of this terminal is 0.5 V_{CC2} nominal.
V_{OUTL}	9	O	L-channel analog signal output of the lineout amplifiers
V_{OUTR}	8	O	R-channel analog signal output of the lineout amplifiers

PCM1772, PCM1773

SLES010G—SEPTEMBER 2001—REVISED MARCH 2007

PCM1772RGA

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND1	4	—	Analog ground. This is a return for V_{CC1} .
AGND2	5	—	Analog ground. This is a return for V_{CC2} .
AIN	10	I	Monaural analog signal mixer input. The signal can be mixed with the output of the L- and R-channel DACs.
BCK	2	I/O	Serial bit clock. Clocks the individual bits of the audio data input, DATA. In the slave interface mode, this clock is input from an external device. In the master interface mode, the PCM1772 device generates the BCK output to an external device.
DATA	1	I	Serial audio data input
LRCK	20	I/O	Left and right clock. Determines which channel is being input on the audio data input, DATA. The frequency of LRCK must be the same as the audio sampling rate. In the slave interface mode, this clock is input from an external device. In the master interface mode, the PCM1772 device generates the LRCK output to an external device.
MC	14	I	Mode control port serial bit clock input. Clocks the individual bits of the control data input, MD.
MD	13	I	Mode control port serial data input. Controls the operation mode on the PCM1772 device.
\overline{MS}	15	I	Mode control port select. The control port is active when this terminal is low.
NC	8, 17, 18, 19	—	No connect
\overline{PD}	3	I	Reset input. When low, the PCM1772 device is powered down, and all mode control registers are reset to default settings.
SCKI	16	I	System clock input
V_{CC1}	12	—	Power supply for all analog circuits except lineout amplifier.
V_{CC2}	11	—	Analog power supply for lineout amplifier circuits. The voltage level must be the same as V_{CC1} .
V_{COM}	6	—	Decoupling capacitor connection. An external 10- μ F capacitor connected from this terminal to analog ground is required for noise filtering. Voltage level of this terminal is 0.5 V_{CC2} nominal.
V_{OUTL}	9	O	L-channel analog signal output of lineout amplifiers.
V_{OUTR}	7	O	R-channel analog signal output of lineout amplifiers.

PCM1773PW

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND1	5	—	Analog ground. This is a return for V_{CC1} .
AGND2	6	—	Analog ground. This is a return for V_{CC2} .
AIN	10	I	Monaural analog signal mixer input. The signal can be mixed with the output of the L- and R-channel DACs.
AMIX	14	I	Analog mixing control
BCK	3	I	Serial bit clock. Clocks the individual bits of the audio data input, DATA.
DATA	2	I	Serial audio data input
DEMP	13	I	De-emphasis control
FMT	15	I	Data format select
LRCK	1	I	Left and right clock. Determines which channel is being input on the audio data input, DATA. The frequency of LRCK must be the same as the audio sampling rate.
\overline{PD}	4	I	Reset input. When low, the PCM1773 device is powered down, and all mode control registers are reset to default settings.
SCKI	16	I	System clock input
V_{CC1}	12	—	Power supply for all analog circuits except the lineout amplifier
V_{CC2}	11	—	Analog power supply for the lineout amplifier circuits. The voltage level must be the same as V_{CC1} .
V_{COM}	7	—	Decoupling capacitor connection. An external 10- μ F capacitor connected from this terminal to analog ground is required for noise filtering. Voltage level of this terminal is 0.5 V_{CC2} nominal.
V_{OUTL}	9	O	L-channel analog signal output of the lineout amplifiers
V_{OUTR}	8	O	R-channel analog signal output of the lineout amplifiers

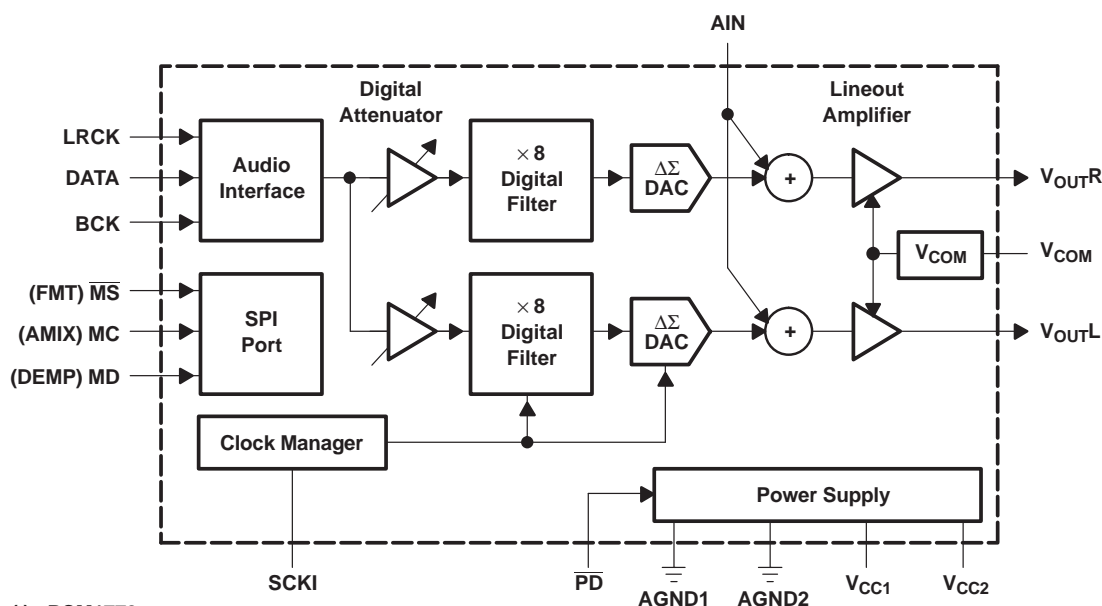
PCM1773RGA

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND1	4	—	Analog ground. This is a return for V_{CC1} .
AGND2	5	—	Analog ground. This is a return for V_{CC2} .
AIN	10	I	Monaural analog signal mixer input. The signal can be mixed with the output of the L- and R-channel DACs.
AMIX	14	I	Analog mixing control
BCK	2	I	Serial bit clock. Clocks the individual bits of the audio data input, DATA.
DATA	1	I	Serial audio data input
DEMP	13	I	De-emphasis control
FMT	15	I	Data format select
LRCK	20	I	Left and right clock. Determines which channel is being input on the audio data input, DATA. The frequency of LRCK must be the same as the audio sampling rate.
NC	8, 17, 18, 19	—	No connect
\overline{PD}	3	I	Reset input. When low, the PCM1773 device is powered down, and all mode control registers are reset to default settings.
SCKI	16	I	System clock input
V_{CC1}	12	—	Power supply for all analog circuits except the lineout amplifier
V_{CC2}	11	—	Analog power supply for the lineout amplifier circuits. The voltage level must be the same as V_{CC1} .
V_{COM}	6	—	Decoupling capacitor connection. An external 10- μ F capacitor connected from this terminal to analog ground is required for noise filtering. Voltage level of this terminal is 0.5 V_{CC2} nominal.
V_{OUTL}	9	O	L-channel analog signal output of the lineout amplifiers
V_{OUTR}	7	O	R-channel analog signal output of the lineout amplifiers

PCM1772, PCM1773

SLES010G–SEPTEMBER 2001–REVISED MARCH 2007

FUNCTIONAL BLOCK DIAGRAM



B0001-01

TYPICAL PERFORMANCE CURVES

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC1} = V_{CC2} = 2.4\text{ V}$, $f_S = 44.1\text{ kHz}$, system clock = $256 f_S$ and 24-bit data, $R_L = 10\text{ k}\Omega$, unless otherwise noted.

DIGITAL FILTER

Digital Filter (De-Emphasis Off)

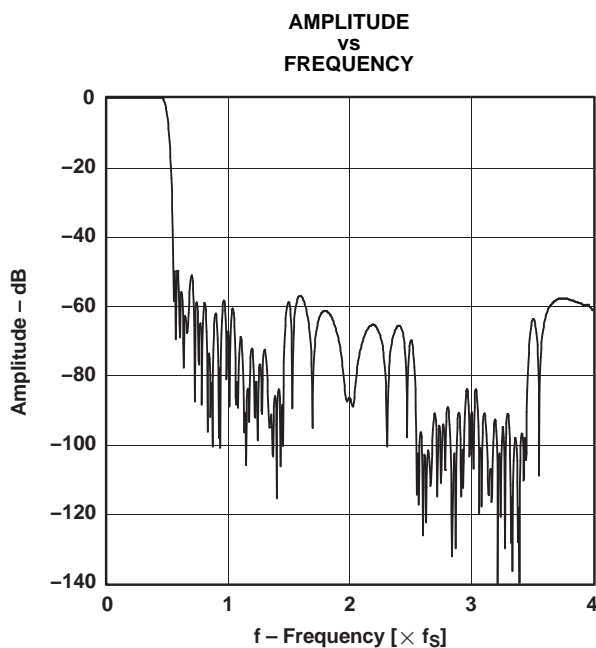


Figure 1.

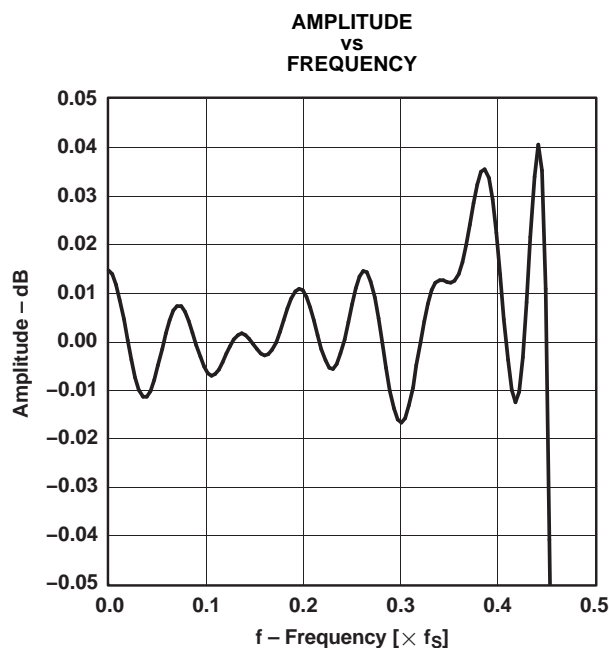
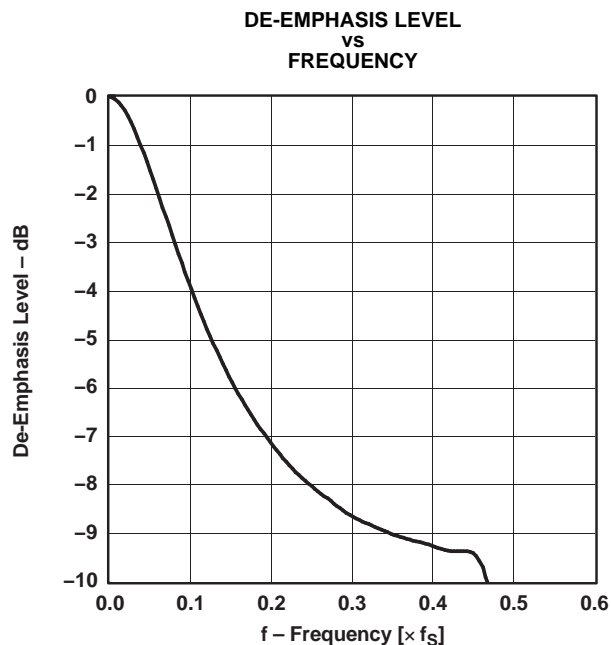


Figure 2.

TYPICAL PERFORMANCE CURVES (continued)

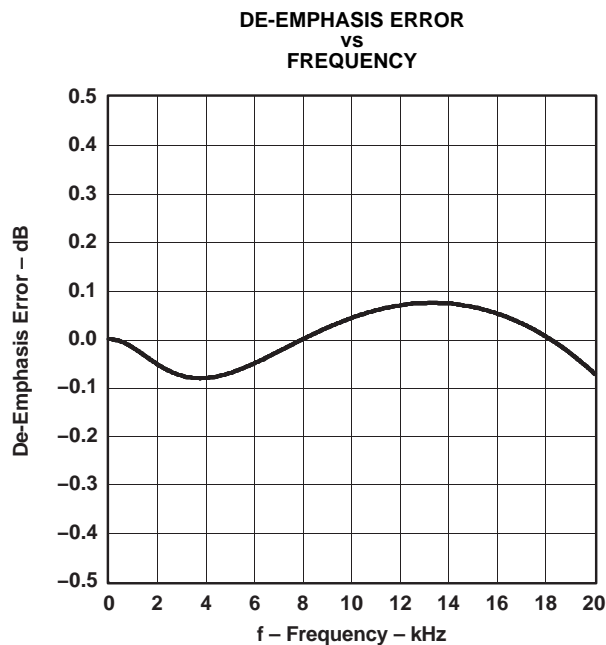
All specifications at $T_A = 25^\circ\text{C}$, $V_{CC1} = V_{CC2} = 2.4\text{ V}$, $f_S = 44.1\text{ kHz}$, system clock = $256 f_S$ and 24-bit data, $R_L = 10\text{ k}\Omega$, unless otherwise noted.

De-Emphasis Curves



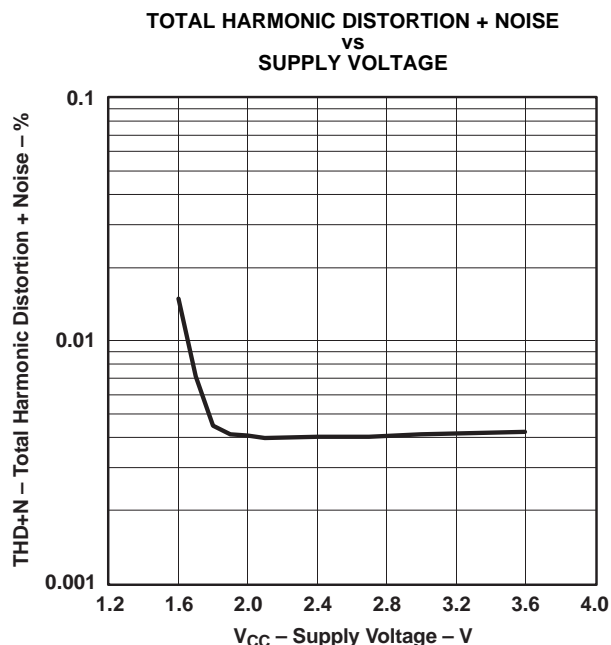
G003

Figure 3.



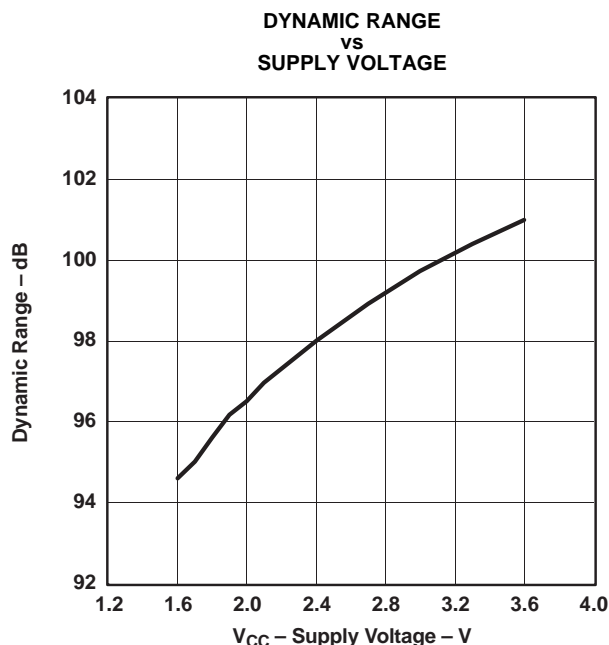
G004

Figure 4.



G005

Figure 5.



G006

Figure 6.

PCM1772, PCM1773

SLES010G–SEPTEMBER 2001–REVISED MARCH 2007

TYPICAL PERFORMANCE CURVES (continued)

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC1} = V_{CC2} = 2.4\text{ V}$, $f_S = 44.1\text{ kHz}$, system clock = $256 f_S$ and 24-bit data, $R_L = 10\text{ k}\Omega$, unless otherwise noted.

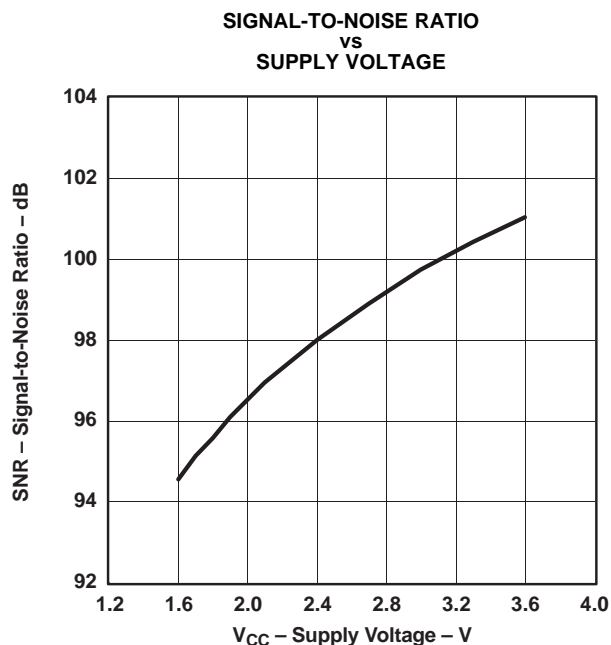


Figure 7.

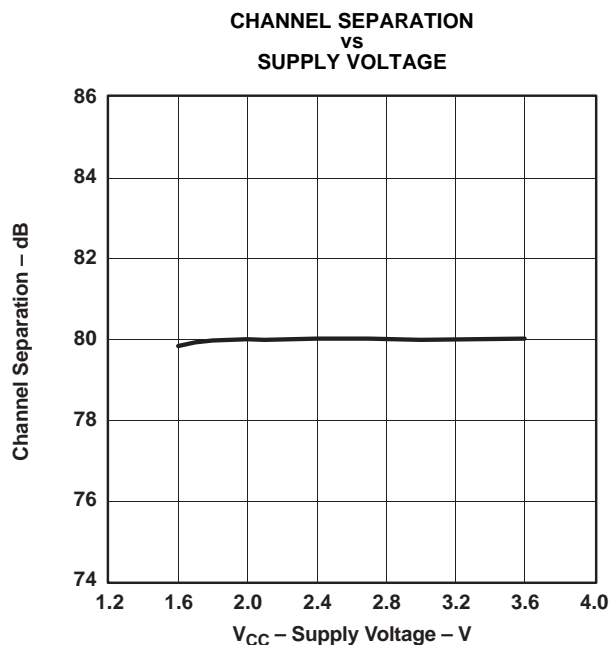


Figure 8.

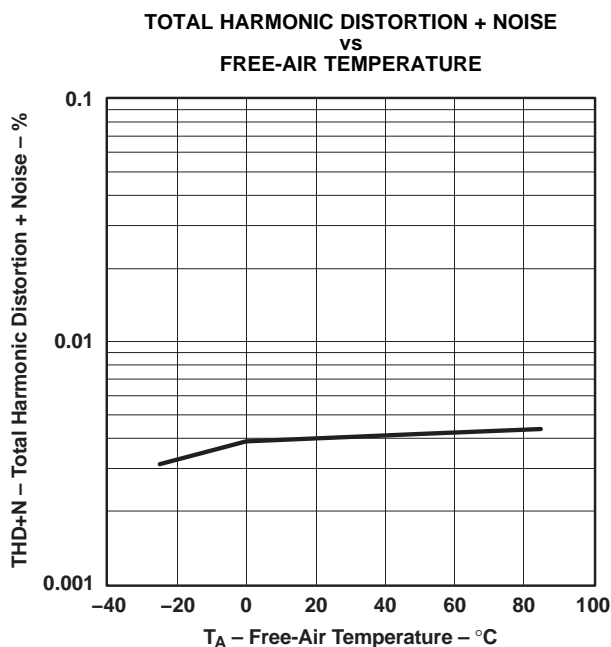


Figure 9.

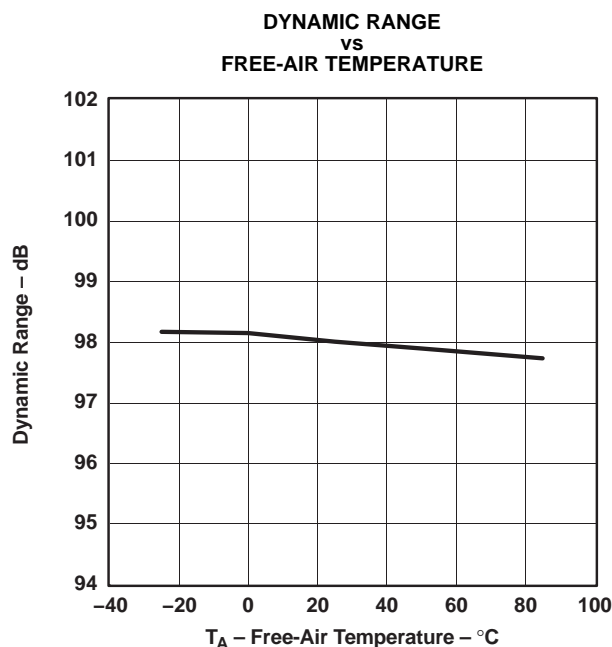


Figure 10.

TYPICAL PERFORMANCE CURVES (continued)

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC1} = V_{CC2} = 2.4\text{ V}$, $f_S = 44.1\text{ kHz}$, system clock = $256 f_S$ and 24-bit data, $R_L = 10\text{ k}\Omega$, unless otherwise noted.

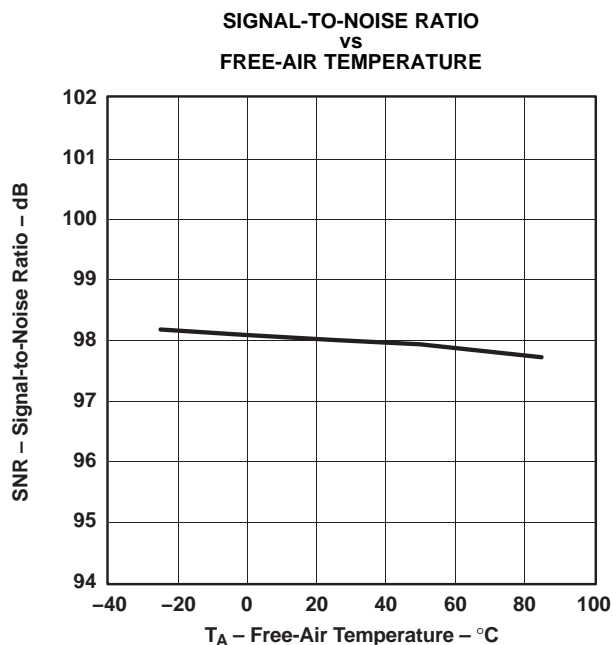


Figure 11.

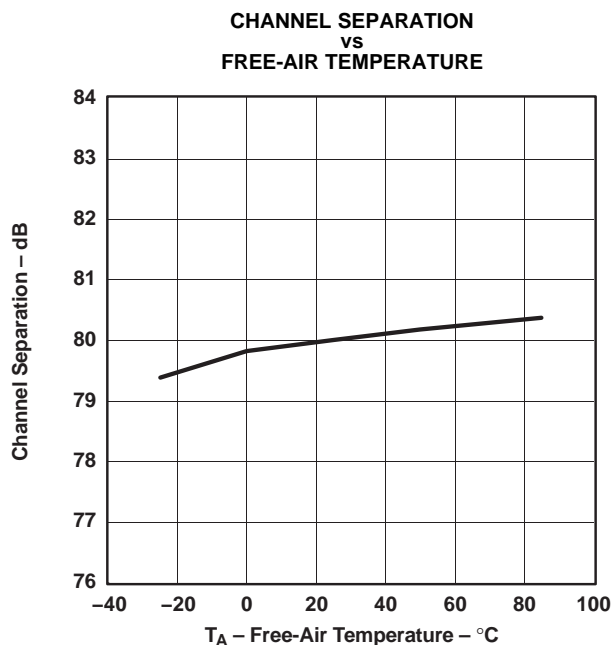


Figure 12.

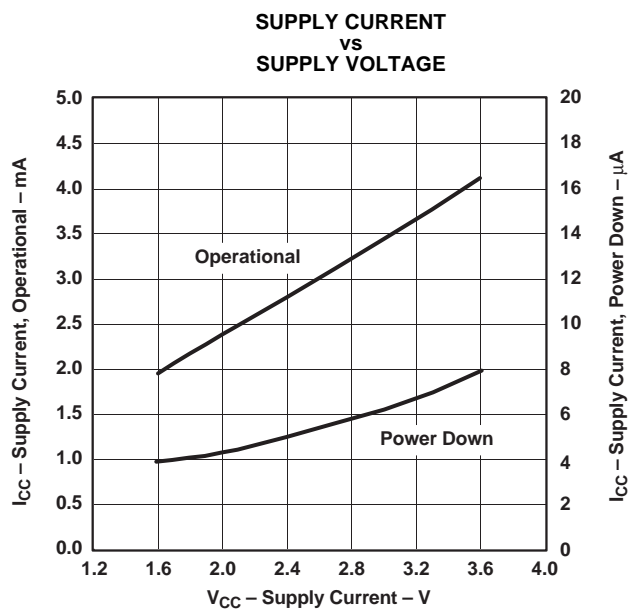


Figure 13.

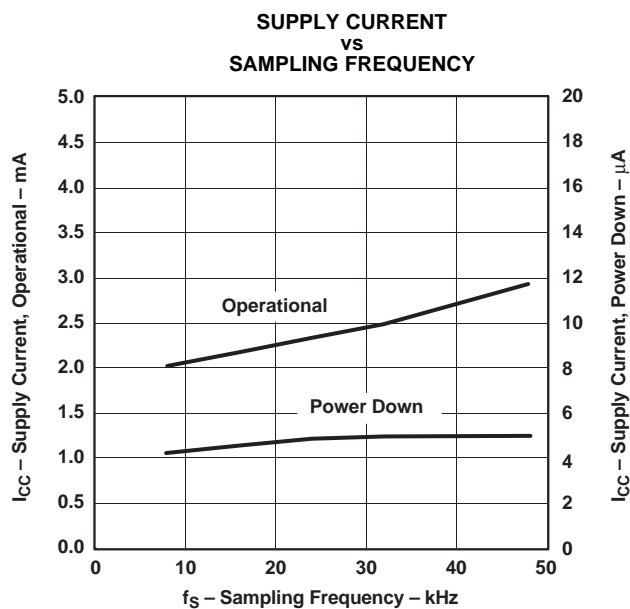


Figure 14.

PCM1772, PCM1773

SLES010G–SEPTEMBER 2001–REVISED MARCH 2007

TYPICAL PERFORMANCE CURVES (continued)

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC1} = V_{CC2} = 2.4\text{ V}$, $f_S = 44.1\text{ kHz}$, system clock = $256 f_S$ and 24-bit data, $R_L = 10\text{ k}\Omega$, unless otherwise noted.

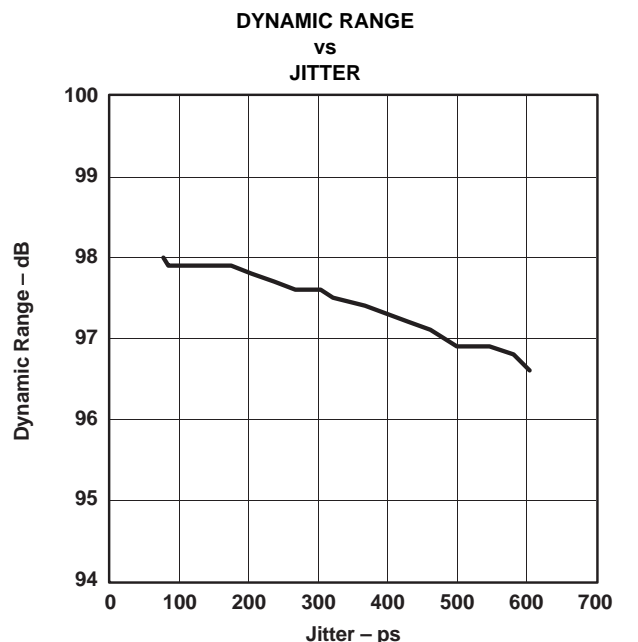


Figure 15.

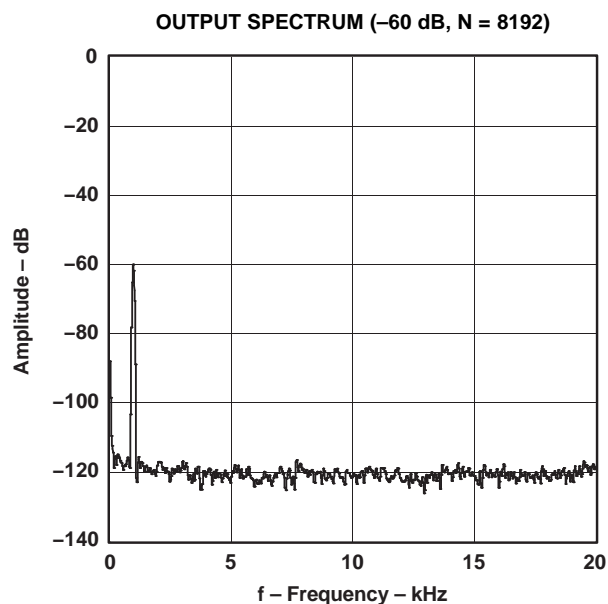


Figure 16.

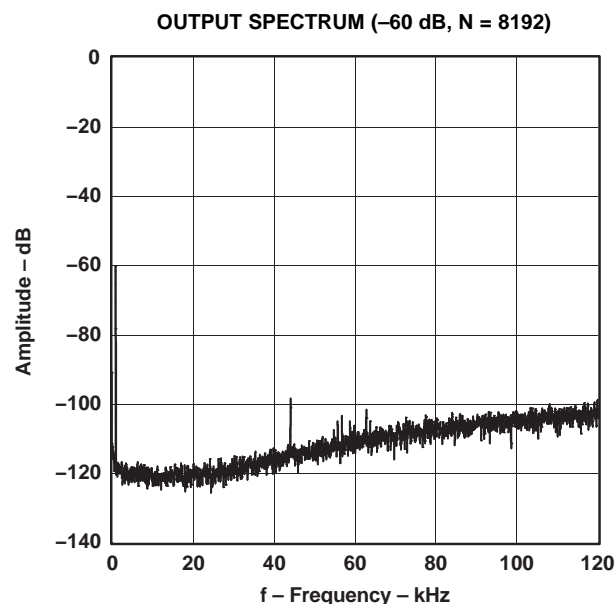


Figure 17.

DETAILED DESCRIPTION

System Clock, Reset, and Functions

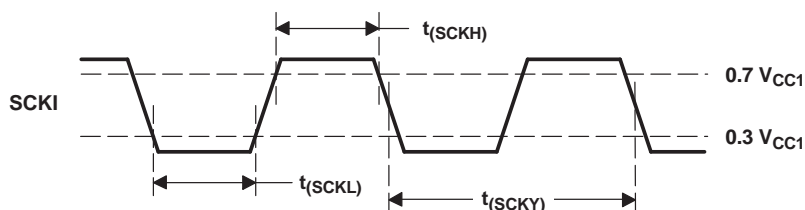
System Clock Input

The PCM1772 and PCM1773 devices require a system clock for operating the digital interpolation filters and multilevel Δ - Σ modulators. The system clock is applied at terminal 16 (SCKI). Table 1 shows examples of system clock frequencies for common audio sampling rates.

Figure 18 shows the timing requirements for the system clock input. For optimal performance, it is important to use a clock source with low phase jitter and noise.

Table 1. System Clock Frequency for Common Audio Sampling Frequencies

SAMPLING FREQUENCY, LRCK	SYSTEM CLOCK FREQUENCY, SCKI (MHz)			
	128 f _s	192 f _s	256 f _s	384 f _s
48 kHz	6.144	9.216	12.288	18.432
44.1 kHz	5.6448	8.4672	11.2896	16.9344
32 kHz	4.096	6.144	8.192	12.288
24 kHz	3.072	4.608	6.144	9.216
22.05 kHz	2.8224	4.2336	5.6448	8.4672
16 kHz	2.048	3.072	4.096	6.144
12 kHz	1.536	2.304	3.072	4.608
11.025 kHz	1.4112	2.1168	2.8224	4.2336
8 kHz	1.024	1.536	2.048	3.072



T0005-01

SYMBOL	PARAMETER	MIN	UNIT
t(SCKH)	System clock pulse duration, HIGH	7	ns
t(SCKL)	System clock pulse duration, LOW	7	ns
t(SCKY)	System clock pulse cycle time ⁽¹⁾	52	ns

(1) 1/(128 f_s), 1/(192 f_s), 1/(256 f_s) or 1/(384 f_s)

Figure 18. System Clock Timing

PCM1772, PCM1773

SLES010G–SEPTEMBER 2001–REVISED MARCH 2007

Power On/Off and Reset

The PCM1772/73 always must have the $\overline{\text{PD}}$ pin set from LOW to HIGH once after power-supply voltages V_{CC1} and V_{CC2} have reached the specified voltage range and stable clocks SCKI, BCK, and LRCK are being supplied for the power-on sequence. A minimum time of 1 ms after both the clock and power-supply requirements are met is required before the $\overline{\text{PD}}$ pin changes from LOW to HIGH, as shown in Figure 19. Subsequent to the $\overline{\text{PD}}$ LOW-to-HIGH transition, the internal logic state is held in reset for 1024 system clock cycles prior to the start of the power-on sequence. During the power-on sequence, V_{OUTL} and V_{OUTR} increase gradually from ground level, reaching an output level that corresponds to the input data after a period of $9334/f_{\text{S}}$. When powering off, the $\overline{\text{PD}}$ pin is set from HIGH to LOW first. Then V_{OUTL} and V_{OUTR} decrease gradually to ground level over a period of $9334/f_{\text{S}}$, as shown in Figure 20, after which power can be removed without creating pop noise. When powering on or off, adhering to the timing requirements of Figure 19 and Figure 20 ensures that pop noise does not occur. If the timing requirements are not met, pop noise might occur.

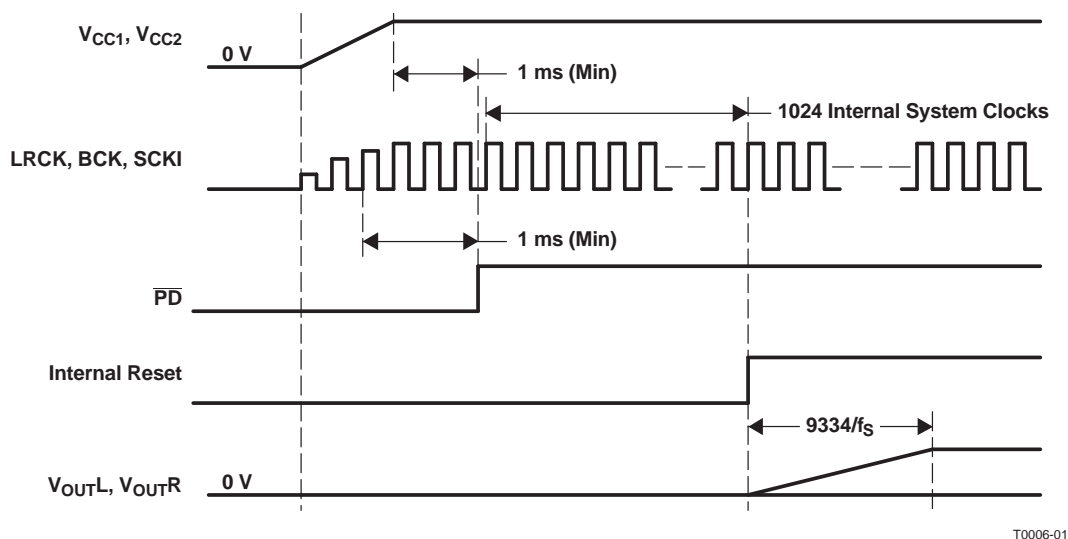


Figure 19. Power-On Sequence

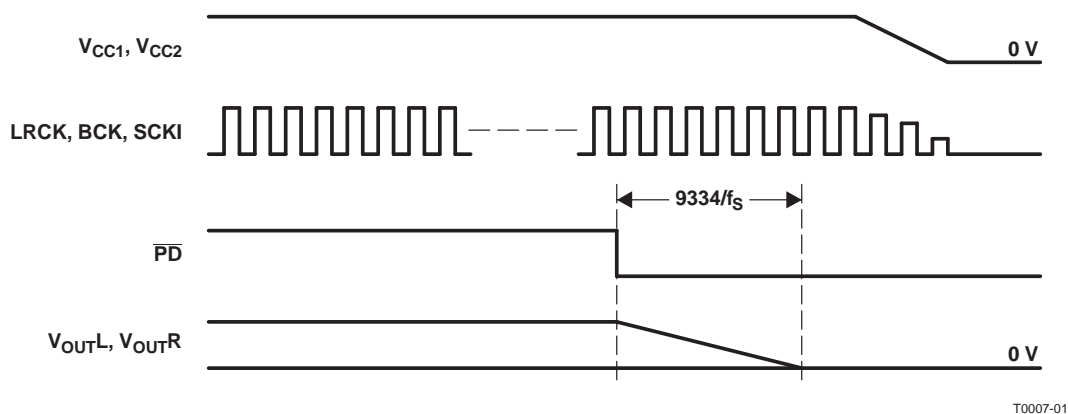


Figure 20. Power-Off Sequence

Power-Up/-Down Sequence and Reset

The PCM1772 device has two kinds of power-up/-down methods: the $\overline{\text{PD}}$ terminal through hardware control and PWRD (register 4, B0) through software control. The PCM1773 device has only the $\overline{\text{PD}}$ terminal through hardware control for the power-up/-down sequence. The power-up or power-down sequence operates the same as the power-on or power-off sequence. When powering up or down using the $\overline{\text{PD}}$ terminal, all digital circuits are reset. When powering up or down using PWRD, all digital circuits are reset except for maintaining the logic states of the registers. Figure 21 shows the power-up/power-down sequence.

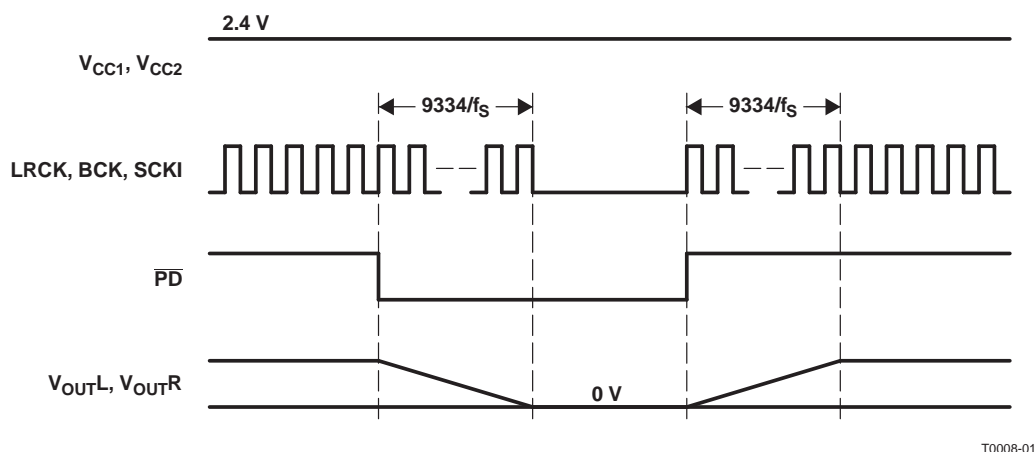


Figure 21. Power-Down and Power-Up Sequences

PCM1772, PCM1773



SLES010G–SEPTEMBER 2001–REVISED MARCH 2007

Audio Serial Interface

The audio serial interface for the PCM1772 and PCM1773 devices consists of a 3-wire synchronous serial port. It includes terminals 1 (LRCK), 2 (DATA), and 3 (BCK). BCK is the serial audio bit clock, and it clocks the serial data present on DATA into the audio interface serial shift register. Serial data is clocked into the PCM1772 and PCM1773 devices on the rising edge of BCK. LRCK is the serial audio left/right word clock. It latches serial data into the serial audio interface internal registers.

Both LRCK and BCK of the PCM1772 device support the slave and master modes, which are set by FMT (register 3). LRCK and BCK are outputs during the master mode and inputs during the slave mode.

In slave mode, BCK and LRCK are synchronous to the audio system clock, SCKI. Ideally, it is recommended that LRCK and BCK be derived from SCKI. LRCK is operated at the sampling frequency, f_s . BCK can be operated at 32, 48, and 64 times the sampling frequency.

In master mode, BCK and LRCK are derived from the system clock, and these terminals are outputs. The BCK and LRCK are synchronous to SCKI. LRCK is operated at the sampling frequency, f_s . BCK can be operated at 64 times the sampling frequency.

The PCM1772 and PCM1773 devices operate under LRCK, synchronized with the system clock. The PCM1772 and PCM1773 devices do not need a specific phase relationship between LRCK and the system clock, but do require the synchronization of LRCK and the system clock. If the relationship between the system clock and LRCK changes more than ± 3 BCK during one sample period, internal operation of the PCM1772 and PCM1773 devices halts within $1/f_s$, and the analog output is kept in last data until resynchronization between system clock and LRCK is completed.

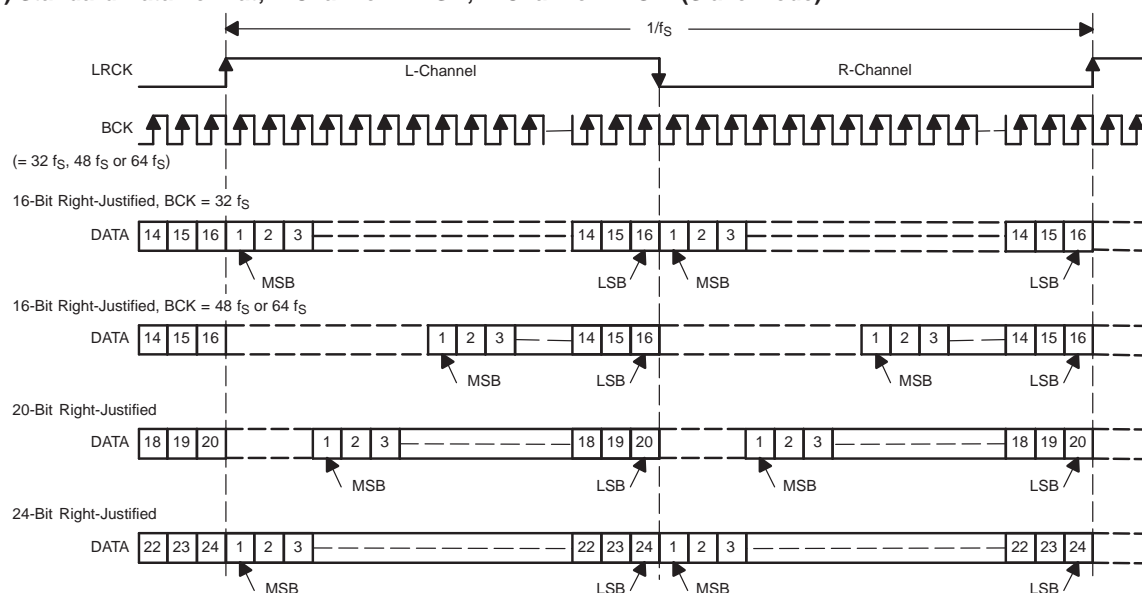
Audio Data Formats and Timing

The PCM1772 device supports industry-standard audio data formats, including standard, I²S, and left justified. The PCM1773 device supports the I²S and left-justified data formats. [Table 2](#) lists the main features of the audio data interface. [Figure 22](#) shows the data formats. Data formats are selected using the format bits, FMT[2:0] of control register 3 in case of the PCM1772 device, and are selected using the FMT terminal in case of the PCM1773 device. The default data format is 24-bit, left-justified, slave mode. All formats require binary 2s complement, MSB-first audio data. [Figure 23](#) shows a detailed timing diagram for the serial audio interface in slave mode. [Figure 24](#) shows a detailed timing diagram for the serial audio interface in master mode.

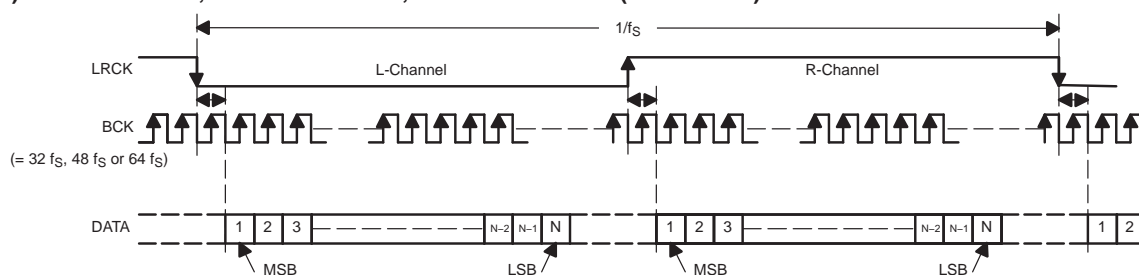
Table 2. Audio Data Interface

AUDIO-DATA INTERFACE FEATURE		CHARACTERISTIC
Audio data interface format	PCM1772	Standard, I ² S, left-justified
	PCM1773	I ² S, left-justified
Audio data bit length		16-, 20-, 24-bit, selectable
Audio data format		MSB first, 2s complement

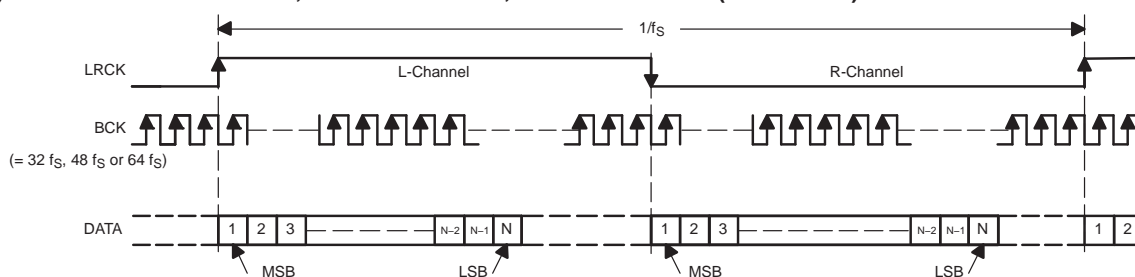
(1) Standard Data Format; L-Channel = HIGH, R-Channel = LOW (Slave Mode)



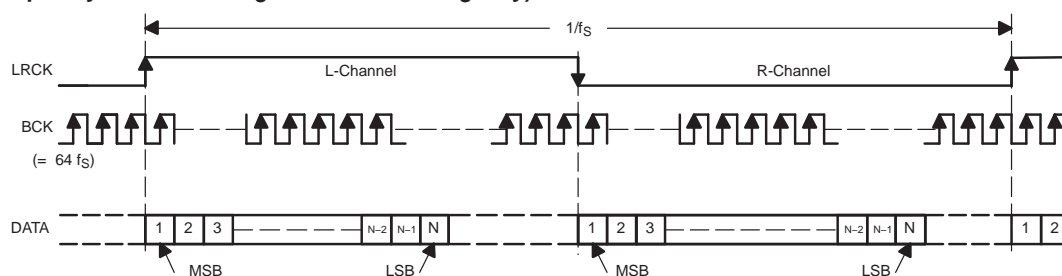
(2) I²S Data Format; L-Channel = LOW, R-Channel = HIGH (Slave Mode)



(3) Left-Justified Data Format; L-Channel = HIGH, R-Channel = LOW (Slave Mode)



(4) Left-Justified Data Format; L-Channel = HIGH, R-Channel = LOW (Master Mode)
(The frequency of BCK is $64 f_s$ and SCKI is $256 f_s$ only)

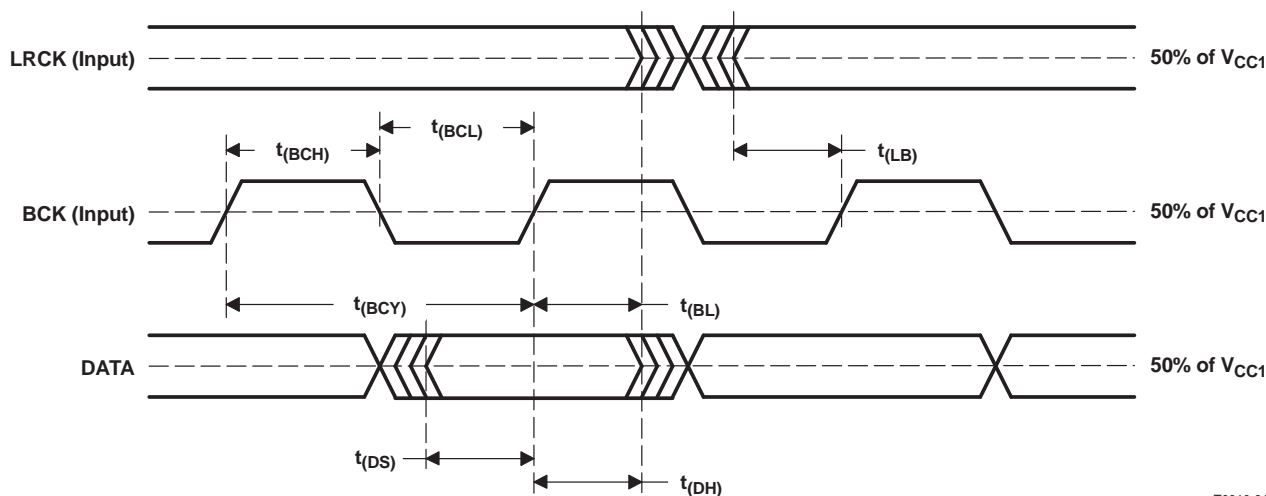


T0009-01

Figure 22. Audio Data Input Formats

PCM1772, PCM1773

SLES010G–SEPTEMBER 2001–REVISED MARCH 2007

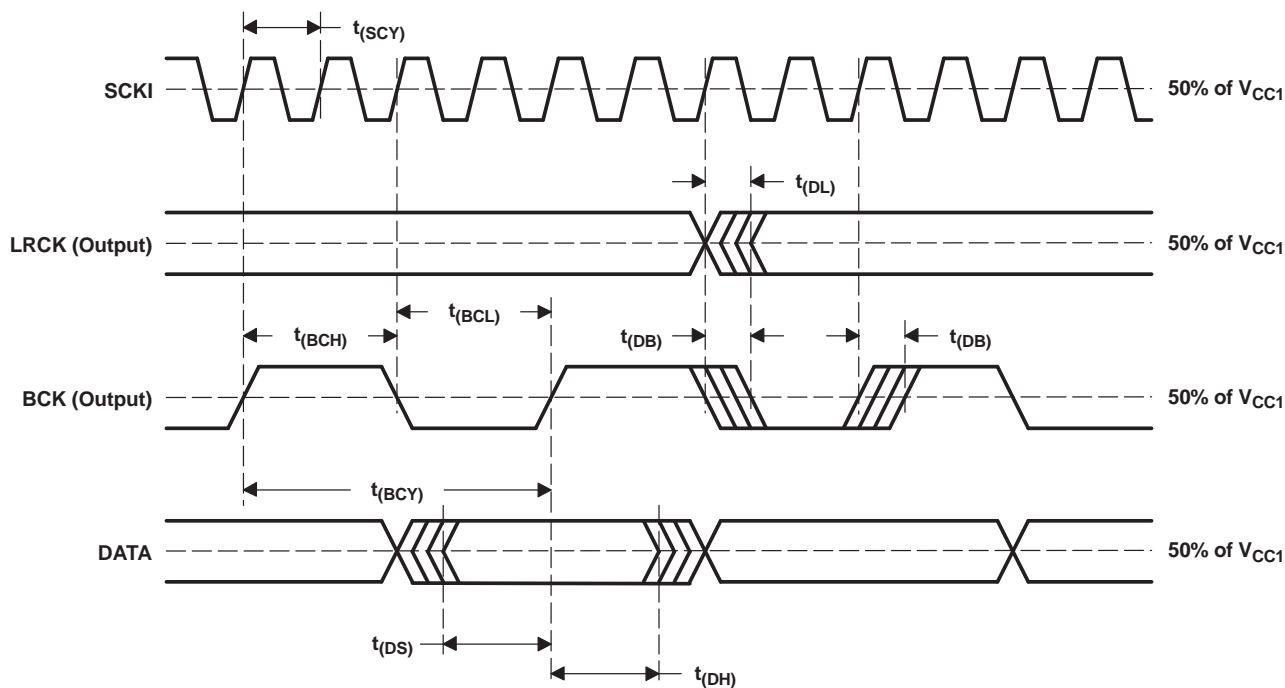


T0010-01

PARAMETERS	SYMBOL	MIN	MAX	UNIT
BCK pulse cycle time	$t_{(BCY)}$	$1/(64 f_S)^{(1)}$		
BCK high-level time	$t_{(BCH)}$	35		ns
BCK low-level time	$t_{(BCL)}$	35		ns
BCK rising edge to LRCK edge	$t_{(BL)}$	10		ns
LRCK edge to BCK rising edge	$t_{(LB)}$	10		ns
DATA setup time	$t_{(DS)}$	10		ns
DATA hold time	$t_{(DH)}$	10		ns

(1) f_S is the sampling frequency.

Figure 23. Audio Interface Timing (Slave Mode)



T0011-01

PARAMETERS	SYMBOL	MIN	MAX	UNIT
SCKI pulse cycle time	$t_{(SCY)}$	$1/(256 f_s)^{(1)}$		
LRCK edge from SCKI rising edge	$t_{(DL)}$	0	40	ns
BCK edge from SCKI rising edge	$t_{(DB)}$	0	40	ns
BCK pulse cycle time	$t_{(BCY)}$	$1/(64 f_s)^{(1)}$		
BCK high-level time	$t_{(BCH)}$	146		ns
BCK low-level time	$t_{(BCL)}$	146		ns
DATA setup time	$t_{(DS)}$	10		ns
DATA hold time	$t_{(DH)}$	10		ns

(1) f_s is up to 48 kHz. f_s is the sampling frequency.

Figure 24. Audio Interface Timing (Master Mode)

PCM1772, PCM1773

SLES010G–SEPTEMBER 2001–REVISED MARCH 2007

Hardware Control (PCM1773)

The digital functions of the PCM1773 device are capable of hardware control. [Table 3](#) shows selectable formats, [Table 4](#) shows de-emphasis control, and [Table 5](#) shows analog mixing control.

Table 3. Data Format Select

FMT	DATA FORMAT
Low	16- to 24-bit, left-justified format
High	16- to 24-bit, I ² S format

Table 4. De-Emphasis Control

DEMP	DE-EMPHASIS FUNCTION
Low	44.1-kHz de-emphasis OFF
High	44.1-kHz de-emphasis ON

Table 5. Analog Mixing Control

AMIX	ANALOG MIXING
Low	Analog mixing OFF
High	Analog mixing ON

Software Control (PCM1772)

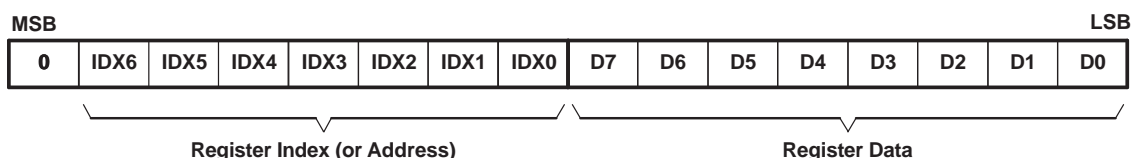
The PCM1772 device has many programmable functions that can be controlled in the software control mode. The functions are controlled by programming the internal registers using \overline{MS} , MC, and MD.

The software control interface is a 3-wire serial port that operates asynchronously to the serial audio interface. The serial control interface is used to program the on-chip mode registers. MD is the serial data input, used to program the mode registers. MC is the serial bit clock, used to shift data into the control port. \overline{MS} is the mode control port select signal.

Register Write Operation (PCM1772)

All write operations for the serial control port use 16-bit data words. Figure 25 shows the control data word format. The most significant bit must be 0. Seven bits, labeled $IDX[6:0]$, set the register index (or address) for the write operation. The eight least significant bits, $D[7:0]$, contain the data to be written to the register specified by $IDX[6:0]$.

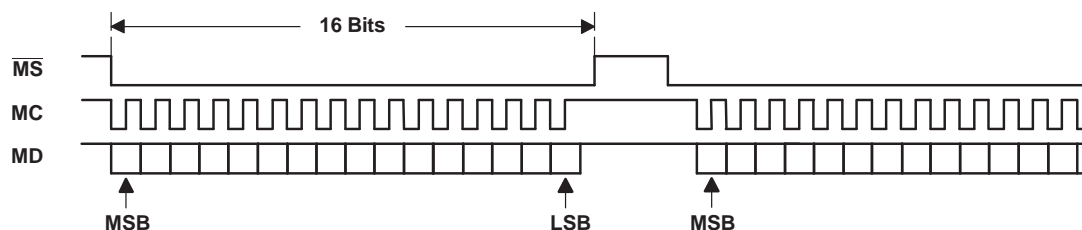
Figure 26 shows the functional timing diagram for writing to the serial control port. To write data into the mode register, data is clocked into an internal shift register on the rising edge of the MC clock. Serial data can change on the falling edge of the MC clock and must be stable on the rising edge of the MC clock. The \overline{MS} signal must be low during the write mode, and the rising edge of the \overline{MS} signal must be aligned with the falling edge of the last MC clock pulse in the 16-bit frame. The MC clock can run continuously between transactions while the \overline{MS} signal is low.



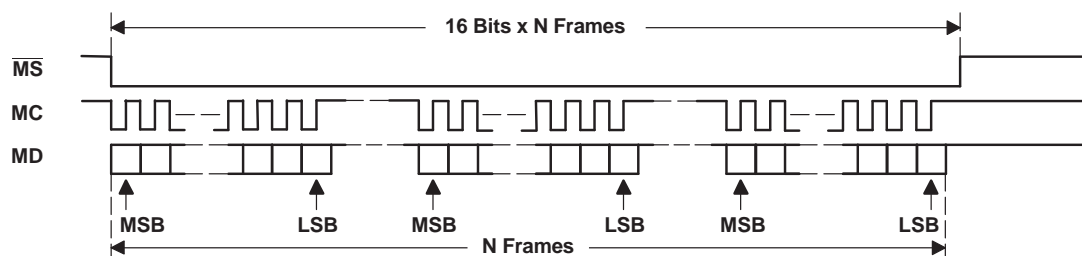
R0001-01

Figure 25. Control Data Word Format for MD

(1) Single Write Operation



(2) Continuous Write Operation



T0012-01

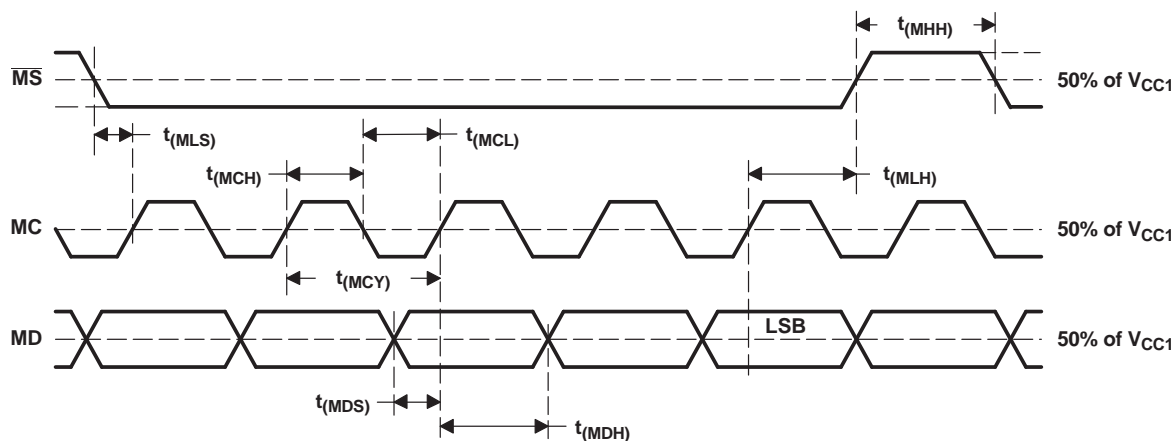
Figure 26. Register Write Operation

PCM1772, PCM1773

SLES010G–SEPTEMBER 2001–REVISED MARCH 2007

Control Interface Timing Requirements (PCM1772)

Figure 27 shows a detailed timing diagram for the serial control interface. These timing parameters are critical for proper control port operation.



T0013-01

PARAMETERS	SYMBOL	MIN	TYP	MAX	UNIT
MC pulse cycle time	$t_{(MCY)}$	100 ⁽¹⁾			ns
MC low-level time	$t_{(MCL)}$	50			ns
MC high-level time	$t_{(MCH)}$	50			ns
\overline{MS} high-level time	$t_{(MHH)}$	⁽²⁾			ns
\overline{MS} falling edge to MC rising edge	$t_{(MLS)}$	20			ns
\overline{MS} hold time	$t_{(MLH)}$	20			ns
MD hold time	$t_{(MDH)}$	15			ns
MD setup time	$t_{(MDS)}$	20			ns

(1) When MC runs continuously between transactions, MC pulse cycle time is specified as $3/(128 f_s)$, where f_s is the sampling rate.

(2) $3/(128 f_s)$ s (minimum), where f_s is sampling rate

Figure 27. Control Interface Timing

Mode Control Registers (PCM1772)

User-Programmable Mode Controls

The PCM1772 device has a number of user-programmable functions that can be accessed via mode control registers. The registers are programmed using the serial control interface, as discussed in the *Software Control (PCM1772)* section. Table 6 lists the available mode control functions, along with their reset default conditions and associated register index.

Register Map

Table 7 shows the mode control register map. Each register includes an index (or address) indicated by the IDX[6:0] bits.

Table 6. User-Programmable Mode Controls

FUNCTION	RESET DEFAULT	REGISTER NO.	BIT(S)
Soft mute control, L/R independently	Disabled	01	MUTL, MUTR
Digital attenuation level setting, 0 dB to –62 dB in 1-dB steps, L/R independently	0 dB	01, 02	ATL[5:0], ATR[5:0]
Oversampling rate control (128 f _S , 192 f _S , 256 f _S , 384 f _S)	128 f _S oversampling	03	OVER
Polarity control for analog output for R-channel DAC	Not inverted	03	RINV
Analog mixing control for analog in, AIN (terminal 14)	Disabled	03	AMIX
44.1-kHz de-emphasis control	Disabled	03	DEM
Audio data format select	24-bit, left-justified format	03	FMT[2:0]
Zero cross attenuation	Disabled	04	ZCAT
Power-down control	Disabled	04	PWRD

Table 7. Mode Control Register Map

Register	IDX [6:0] (B14- B8)	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 01	01h	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	MUTR	MUTL	ATL5	ATL4	ATL3	ATL2	ATL1	ATL0
Register 02	02h	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV ⁽¹⁾	RSV ⁽¹⁾	ATR5	ATR4	ATR3	ATR2	ATR1	ATR0
Register 03	03h	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	OVER	RSV ⁽¹⁾	RINV	AMIX	DEM	FMT2	FMT1	FMT0
Register 04	04h	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV ⁽¹⁾	RSV ⁽¹⁾	RSV ⁽¹⁾	ZCAT	RSV ⁽¹⁾	RSV ⁽¹⁾	RSV ⁽¹⁾	PWRD

(1) RSV: Reserved for test operation. It must be set to 0 during regular operation.

PCM1772, PCM1773

SLES010G–SEPTEMBER 2001–REVISED MARCH 2007

Register Definitions

Register 01

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	MUTR	MUTL	ATL5	ATL4	ATL3	ATL2	ATL1	ATL0

IDX[6:0]: 000 0001b

MUTx: Soft Mute Control

Where, x = L or R, corresponding to the line output V_{OUTL} or V_{OUTR} .

Default Value: 0

MUTL, MUTR = 0	Mute disabled (default)
MUTL, MUTR = 1	Mute enabled

The mute bits, MUTL and MUTR, enable or disable the soft mute function for the corresponding line outputs, V_{OUTL} and V_{OUTR} . The soft mute function is incorporated into the digital attenuators. When mute is disabled ($MUTx = 0$), the attenuator and DAC operate normally. When mute is enabled by setting $MUTx = 1$, the digital attenuator for the corresponding output is decreased from the current setting to infinite attenuation, one attenuator step (1 dB) at a time. This provides pop-free muting of the line output.

By setting $MUTx = 0$, the attenuator is increased one step at a time to the previously programmed attenuation level.

ATL[5:0]: Digital Attenuation Level Setting for Line Output, V_{OUTL}

Default value: 11 1111b

Line output, V_{OUTL} , includes a digital attenuation function. The attenuation level can be set from 0 dB to –62 dB, in 1-dB steps. Changes in attenuator levels are made by incrementing or decrementing by one step (1 dB) for every $8/f_s$ time interval until the programmed attenuator setting is reached. Alternatively, the attenuation level can be set to infinite attenuation (or mute).

The following table shows attenuation levels for various settings:

ATL[5:0]	ATTENUATION LEVEL SETTING
11 1111b	0 dB, no attenuation (default)
11 1110b	–1 dB
11 1101b	–2 dB
:	:
00 0010b	–61 dB
00 0001b	–62 dB
00 0000b	Mute

Register 02

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	ATR5	ATR4	ATR3	ATR2	ATR1	ATR0

IDX[6:0]: 000 0010b

ATR[5:0]: Digital Attenuation Level Setting for Line Output, V_{OUTR}

Default Value: 11 1111b

Line output, V_{OUTR} , includes a digital attenuation function. The attenuation level can be set from 0 dB to –62 dB, in 1-dB steps. Changes in attenuator levels are made by incrementing or decrementing by one step (1 dB) for every $8/f_s$ time interval until the programmed attenuator setting is reached. Alternatively, the attenuation level can be set to infinite attenuation (or mute).

To set the attenuation levels for ATR[5:0], see the table for ATL[5:0], register 01.

Register 03

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	OVER	RSV	RINV	AMIX	DEM	FMT2	FMT1	FMT0

IDX[6:0]: 000 0011b

OVER: Oversampling Control

Default Value: 0

OVER = 0	128f _S oversampling
OVER = 1	192f _S , 256f _S , 384f _S oversampling

The OVER bit controls the oversampling rate of the Δ - Σ D/A converters. When it operates at a low sampling rate, less than 24 kHz, this function is recommended.

RINV: Polarity Control for Line Output, V_{OUTR}

Default Value: 0

RINV = 0	Not inverted
RINV = 1	Inverted output

The RINV bits allow the user to control the polarity of the line output, V_{OUTR}. This function can be used to connect the monaural speaker with BTL connection method. This bit is recommended to be 0 during the power-up/down sequence for minimizing audible pop noise.

AMIX: Analog Mixing Control for External Analog Signal, AIN

Default Value: 0

AMIX = 0	Disabled (not mixed)
AMIX = 1	Enabled (mixing to the DAC output)

AMIX bit allows the user to mix analog input (AIN) with line outputs (V_{OUTL}/V_{OUTR}) internally.

DEM: 44.1-kHz De-Emphasis Control

Default Value: 0

DEM = 0	Disabled
DEM = 1	Enabled

The DEM bit enables or disables the digital de-emphasis filter for 44.1-kHz sampling rate.

FMT[2:0]: Audio Interface Data Format

Default Value: 000

The FMT[2:0] bits select the data format for the serial audio interface. The following table shows the available format options.

FMT[2:0]	Audio Data Format Selection
000	16- to 24-bit, left-justified format (default)
001	16- to 24-bit, I ² S format
010	24-bit right-justified data
011	20-bit right-justified data
100	16-bit right-justified data
101	16- to 24-bit, left-justified format, master mode
110	Reserved
111	Reserved

PCM1772, PCM1773

SLES010G–SEPTEMBER 2001–REVISED MARCH 2007

Register 04

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	ZCAT	RSV	RSV	RSV	PWRD

IDX[6:0]: 000 0100b

ZCAT: Zero Cross Attenuation

Default Value: 0

ZCAT = 0	Normal attenuation (default)
ZCAT = 1	Zero cross attenuation

This bit enables changing the signal level on zero crossing during attenuation control or muting. If the signal does not cross BPZ beyond $512/f_s$ (11.6 ms at the 44.1-kHz sampling rate), the signal level is changed similarly to normal attenuation control. This function is independently monitored for each channel; moreover, change of signal level is alternated between both channels. Figure 28 shows an example of zero cross attenuation.

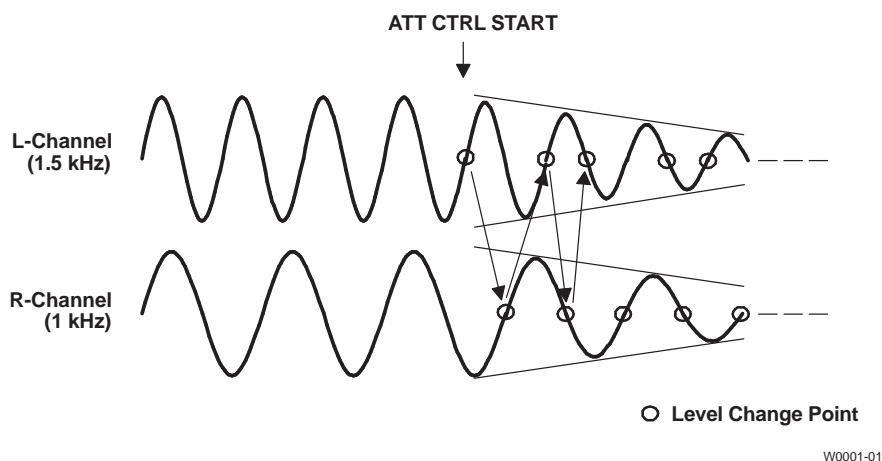


Figure 28. Example of Zero Cross Attenuation

PWRD: Power Down Control

Default Value: 0

PWRD = 0	Normal operation (default)
PWRD = 1	Power-down state

This bit is used to enter into low-power mode. Note that PWRD has no reset function.

When this bit is set to 1, the PCM1772 device enters low-power mode, and all digital circuits are reset except the register states, which remain unchanged.

Analog In/Out

Line Output (Stereo)

The PCM1772 and PCM1773 devices have two independent lineout amplifiers, and each amplifier output is provided at the corresponding V_{OUTL} or V_{OUTR} terminal. The capability of line output is designed for driving a 10-k Ω minimum load.

Monaural Output (BTL Mode/Monaural Speaker)

When the user needs monaural output, the PCM1772 device can provide it. The PCM1772 device has RINV bit on control register 03. Because this bit allows the user to invert the polarity of the line output for the right channel, the user can create a monaural output by summing the line output for left and right channels through the external power amplifier or headphone amplifier. The RINV bit is recommended to be 0 during power-up/-down sequence for minimizing audible pop noise.

Analog Input

The PCM1772 and PCM1773 devices have an analog input, AIN (terminal 10). The AMIX bit (PCM1772) or the AMIX terminal (PCM1773) allows the user to mix AIN with the line outputs (V_{OUTL} and V_{OUTR}) internally. When in MIXING mode, an ac-coupling capacitor is needed for AIN. But if AIN is not used, AIN must be open and the AMIX bit (PCM1772) must be disabled or the AMIX terminal (PCM1773) must be low.

Because AIN does not have an internal low-pass filter, it is recommended that the bandwidth of the input signal into AIN is limited to less than 100 kHz. The source of signals connected to AIN must be connected by low impedance.

Although the maximum input voltage on AIN is designed to be as large as $0.584 V_{CC2}$ [peak-to-peak], the user must attenuate the input voltage on AIN and control the digital input data so that each line output (V_{OUTL} and V_{OUTR}) does not exceed $0.75 V_{CC2}$ [peak-to-peak] during mixing mode.

V_{COM} Output

One unbuffered common-mode voltage output terminal, V_{COM} , is brought out for decoupling purposes. This terminal is nominally biased to a dc voltage level equal to $0.5 V_{CC2}$ and connected to a 10- μ F capacitor. In the case of a capacitor smaller than 10 μ F, pop noise can be generated during the power-on/-off or power-up/-down sequences.

PCM1772, PCM1773

SLES010G–SEPTEMBER 2001–REVISED MARCH 2007

APPLICATION INFORMATION

Connection Diagrams

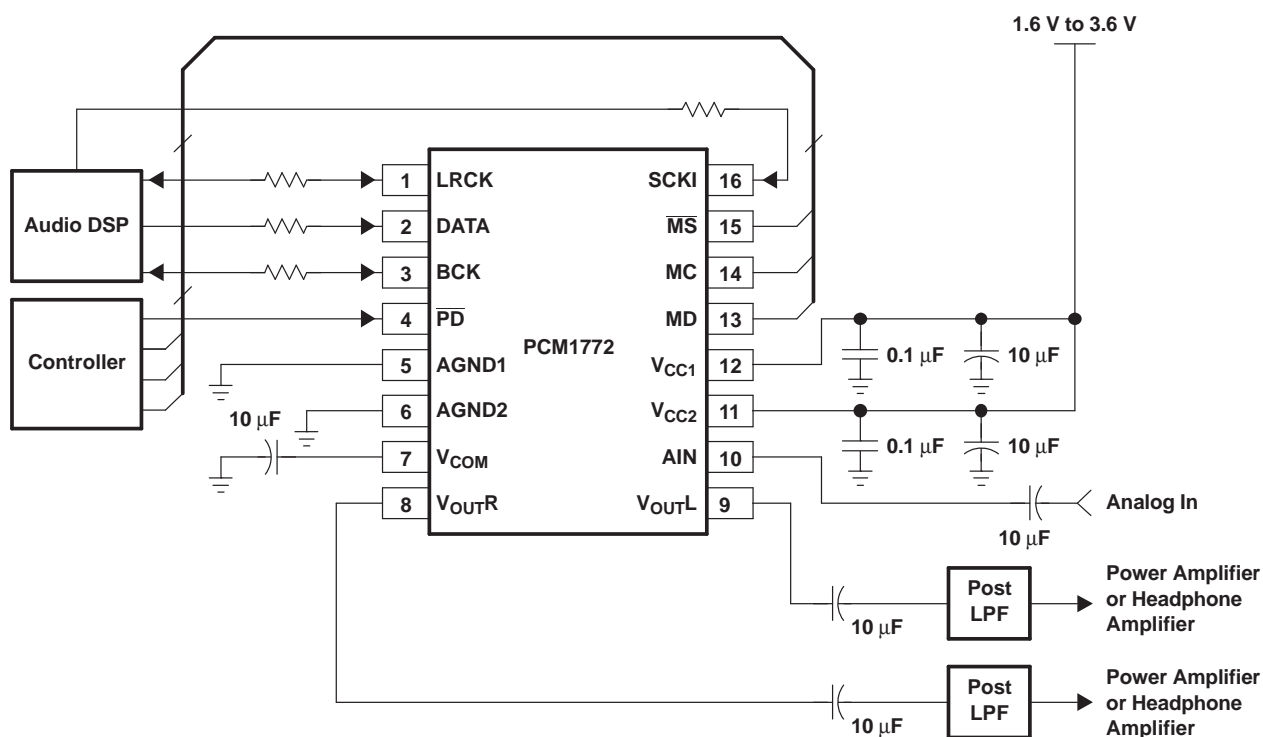
Figure 29 shows the basic connection diagram with the necessary power supply bypassing and decoupling components. It is recommended that the component values shown in Figure 29 be used for all designs.

The use of series resistors ($22\ \Omega$ to $100\ \Omega$) is recommended for the SCKI, LRCK, BCK, and DATA inputs. The series resistor combines with the stray PCB and device input capacitance to form a low-pass filter that reduces high-frequency noise emissions and helps to dampen glitches and ringing present on the clock and data lines.

Power Supplies and Grounding

The PCM1772 and PCM1773 devices require a 2.4-V typical analog supply for V_{CC1} and V_{CC2} . These 2.4-V supplies power the DAC, analog output filter, and other circuits. For best performance, these 2.4-V supplies must be derived from the analog supply using a linear regulator, as shown in Figure 29.

Figure 29 shows the proper power supply bypassing. The $10\text{-}\mu\text{F}$ capacitors must be tantalum or aluminum electrolytic, while the $0.1\text{-}\mu\text{F}$ capacitors are ceramic (X7R type is recommended for surface-mount applications).



S0007-01

Figure 29. Basic Connection Diagram

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from F Revision (November 2005) to G Revision	Page
<ul style="list-style-type: none"> Changed signal name from MCKI to SCKI Corrected errors, added recommended parts, and changed incorrect symbols 	<ul style="list-style-type: none"> 28 28
Changes from E Revision (April 2005) to F Revision	Page
<ul style="list-style-type: none"> Changed dynamic performance for full-scale output voltage of line output from 0.75 Vcc2 to 0.77 Vcc2 	<ul style="list-style-type: none"> 3
Changes from D Revision (May 2004) to E Revision	Page
<ul style="list-style-type: none"> Changed data sheet to new format Changed value for power-supply voltage Removed package/ordering information, reformatted, and appended at end of data sheet Added new Recommended Operating Conditions table to data sheet Changed page layout for terminal function tables Changed page layout of Figure 13 and Figure 14 In Figure 22, added arrows to all rising edges of BCK for data formats (2), (3), and (4) In Figure 29, changed signal direction on SCKI pin 	<ul style="list-style-type: none"> 1 2 2 2 5 11 17 28

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCM1772PW	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1772	Samples
PCM1772PWG4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1772	Samples
PCM1772PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1772	Samples
PCM1772PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1772	Samples
PCM1772RGA	ACTIVE	VQFN	RGA	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		1772	Samples
PCM1772RGAR	ACTIVE	VQFN	RGA	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		1772	Samples
PCM1773PW	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1773	Samples
PCM1773PWG4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1773	Samples
PCM1773PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1773	Samples
PCM1773RGA	ACTIVE	VQFN	RGA	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		1773	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

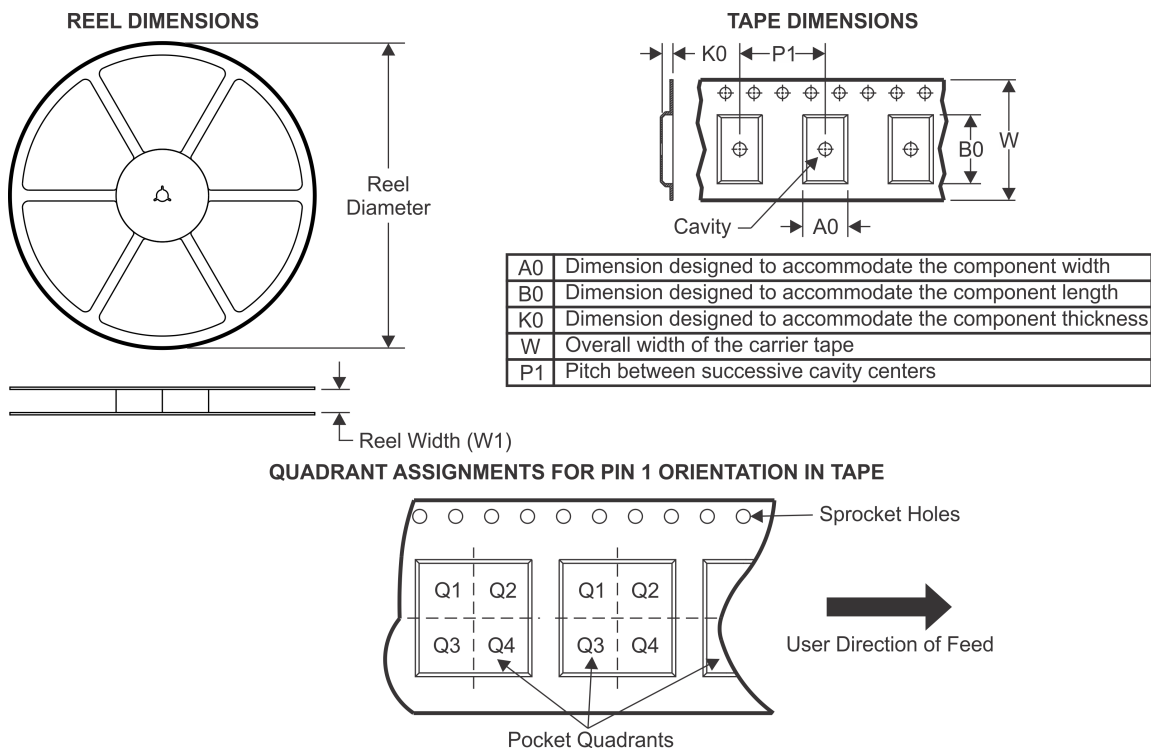
⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

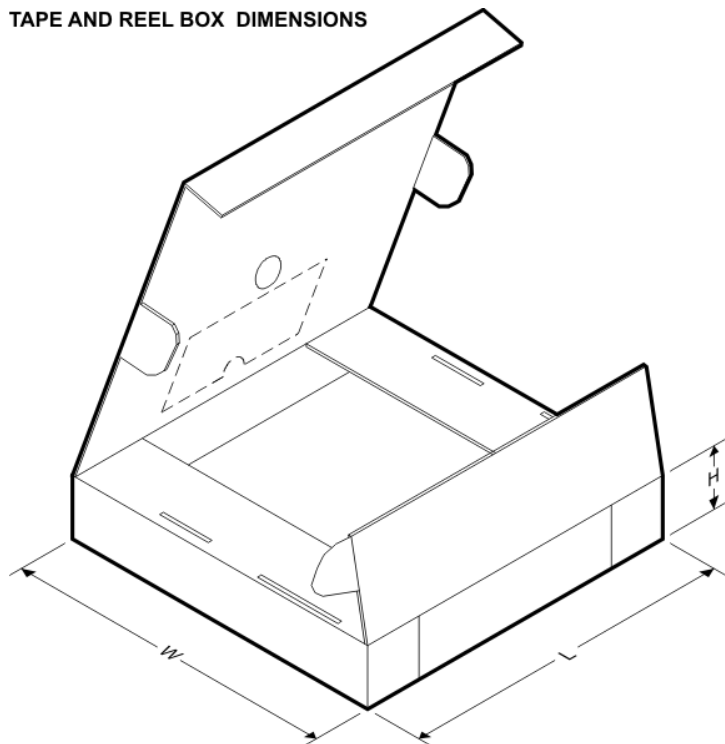
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM1772PWR	TSSOP	PW	16	2000	330.0	17.4	6.8	5.4	1.6	8.0	16.0	Q1
PCM1772RGAR	VQFN	RGA	20	2000	330.0	13.4	4.4	4.4	1.3	8.0	12.0	Q1
PCM1773PWR	TSSOP	PW	16	2000	330.0	17.4	6.8	5.4	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



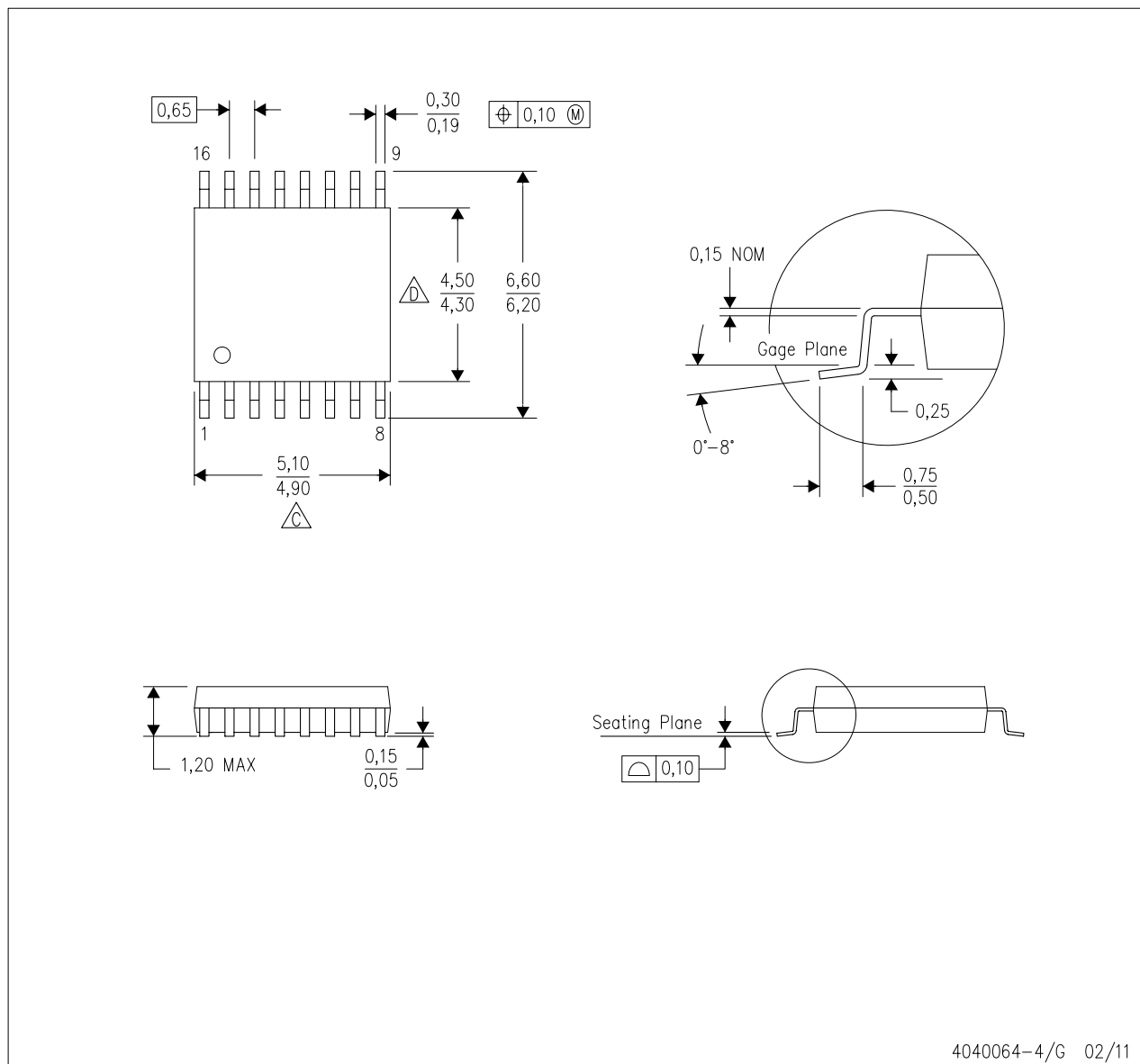
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM1772PWR	TSSOP	PW	16	2000	367.0	367.0	38.0
PCM1772RGAR	VQFN	RGA	20	2000	367.0	367.0	35.0
PCM1773PWR	TSSOP	PW	16	2000	367.0	367.0	38.0

MECHANICAL DATA

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

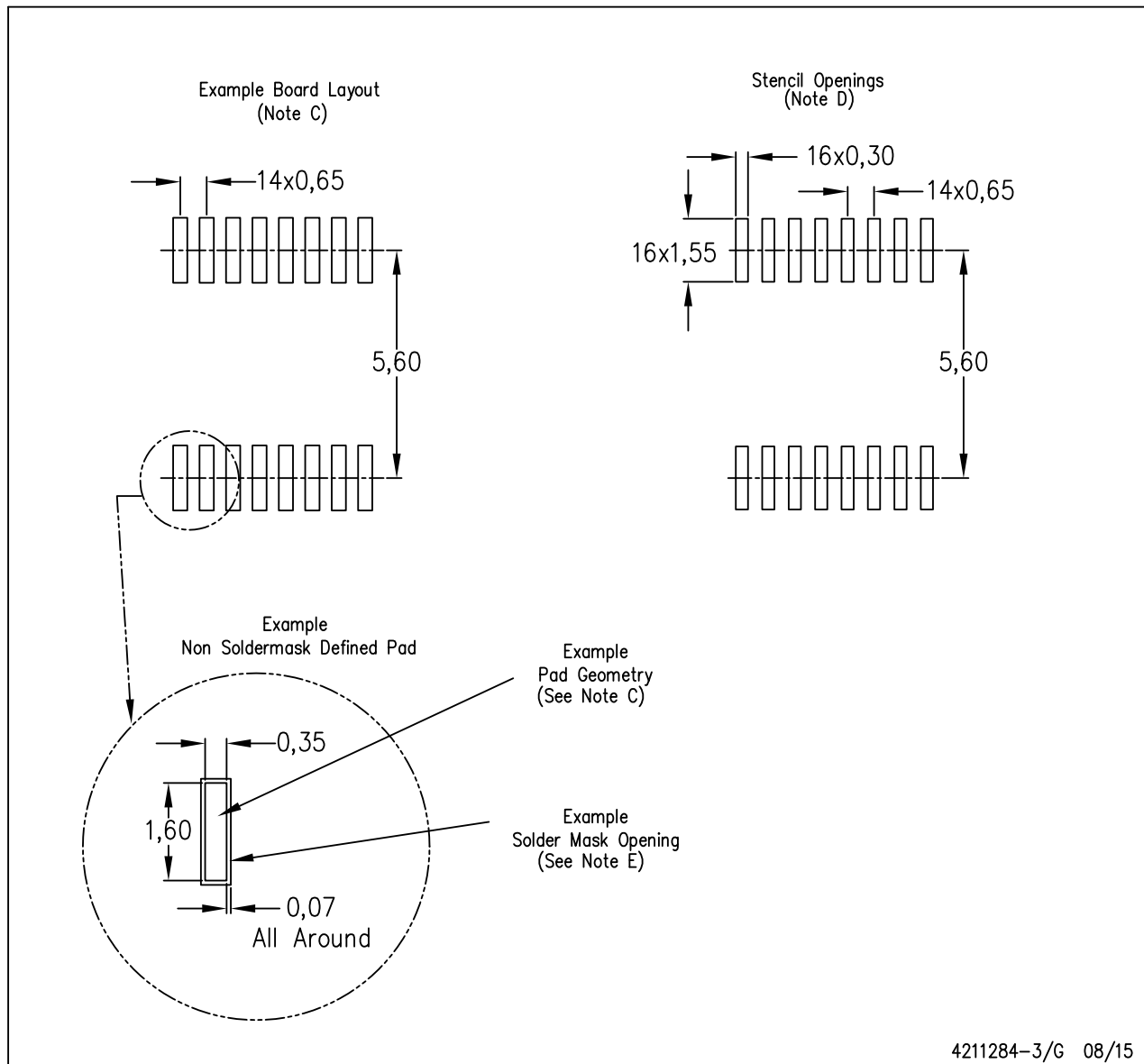


4040064-4/G 02/11

LAND PATTERN DATA

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

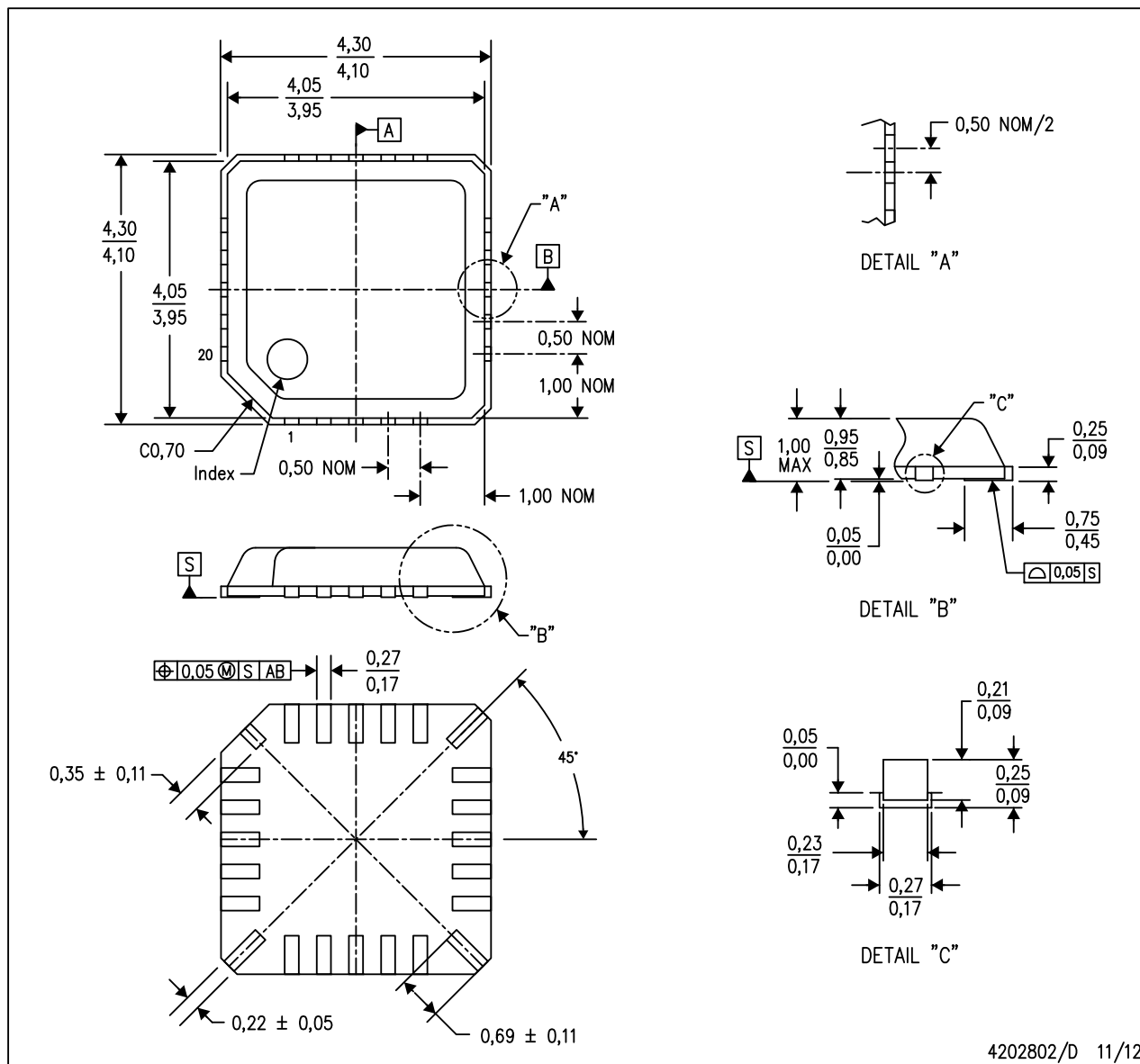


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

RGA (S-PQFP-N20)

PLASTIC QUAD FLATPACK



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - These dimensions include package bend.
 - Falls within EIAJ: EDR-7324.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com