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SiT9102

LVPECL / HCSL / LVDS / CML

1 to 220 MHz High Performance Oscillator



Features

- Extremely low RMS phase jitter (random)
 - <1 ps (typical)
- Wide frequency range
 - 1 MHz to 220 MHz
 - 220 MHz to 800 MHz refer to SiT9107
- High frequency stability
 - ± 10 PPM, ± 15 PPM, ± 20 PPM
 - ± 25 PPM, ± 50 PPM
- Operating voltage
 - 1.8, 2.5 or 3.3 V
 - Other voltages up to 3.63 V (contact SiTime)
- Operating temperature range
 - Industrial, -40 to 85 °C
 - Extended Commercial, -20 to 70 °C
 - Commercial, 0 to 70 °C
- Small footprint
 - 5.0 x 3.2 x 0.75 mm
 - 7.0 x 5.0 x 0.90 mm
- Pb-free and RoHS compliant
- For Spread Spectrum see SiT9002
- Ultra-reliable start up and greater immunity from interference

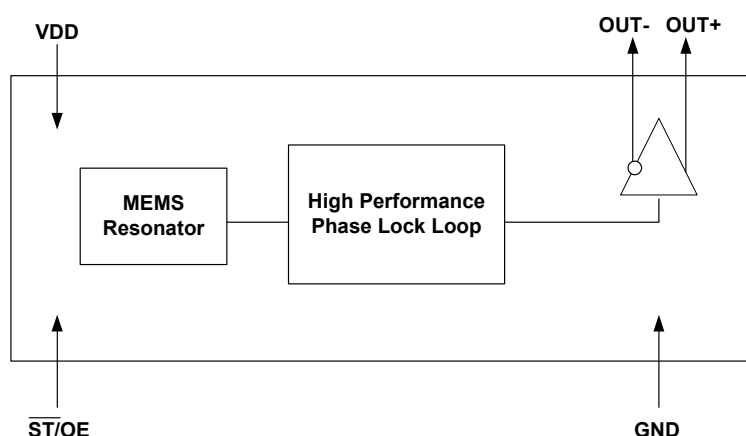
Benefits

- Ultra fast lead time: 2 to 3 weeks
- No crystal or capacitors required
- Eliminates crystal qualification time
- 50% + board saving space
- More cost effective than quartz oscillators, quartz crystals and clock ICs.
- Completely quartz-free

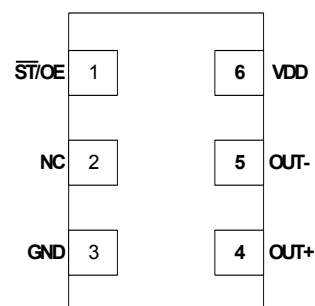
Applications

- Server
- Router
- RAID controller
- Gigabit Ethernet
- 10 Gigabit Ethernet
- Fiber Channel
- SATA / SAS
- PCI-Express
- Fully Buffered DIMM
- System clock
- Networking and computing

Block Diagram



Pinout



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Pin Description

Pin No.	Name		Pin Description
1	ST/OE	Input	Standby or Output Enable pin for OUT+ and OUT-. OE: When High or Open : OUT+ and OUT- = active When Low : OUT+ and OUT- = High Impedance state ST: When High or Open : OUT+ and OUT- = active When Low : OUT+ and OUT- = Output is low (weak pull down), oscillation stops
2	NC	NA	Do Not connect pin, leave it floating.
3	GND	Power	VDD power supply ground. Connect to Ground
4	OUT+	Output	1 to 220 MHz programmable clock output .
5	OUT-	Output	
6	VDD	Power	Power supply

Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Absolute Maximum Table

Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
VDD	-0.5	4	V
Vin	GND - 0.5	VDD + 0.5	V
Theta JA (with copper plane on VDD and GND) 5.0 x 3.2 package 7.0 x 5.0 package when center pad is soldered down 7.0 x 5.0 package when center pad is not soldered down	—	68	°C/W
	—	38	°C/W
	—	90	°C/W
Theta JC (with PCB traces of 0.010 inch to all pins) 5.0 x 3.2 package 7.0 x 5.0 package when center pad is soldered down 7.0 x 5.0 package when center pad is not soldered down	—	45	°C/W
	—	35	°C/W
	—	48	°C/W
Soldering Temperature (follow standard Pb free soldering guidelines)	—	260	°C
Number of Program Writes	—	1	NA
Program Retention over -40 to 125C, Process, VDD (0 to 3.6V)	—	1,000+	years
Human Body Model (JESD22-A114)	2000	—	—
Charged Device Model (JESD22-C101)	750	—	—
Machine Model (JESD22-A115)	200	—	—

Environmental Compliance

Parameter	Condition/Test Method
Mechanical Shock	MIL-STD-883F, Method 2002
Mechanical Vibration	MIL-STD-883F, Method 2007
Temperature Cycle	MIL-STD-883F, Method 1010-65-150°C (1000 cycle)
Solderability	MIL-STD-883F, Method 2003
Moisture Sensitivity Level	MSL1 @ 260°C

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DC Electrical Specifications

LVCMOS input, OE or ST pin, 3.3V $\pm 10\%$ or 2.5V $\pm 10\%$ or 1.8V $\pm 5\%$, -40 to 85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V _{IH}	Input High Voltage		70	–	–	%V _{DD}
V _{IL}	Input Low Voltage		–	–	30	%V _{DD}
I _{IH}	Input High Current	OE or ST pin	–	–	10	μA
I _{IL}	Input Low Current	OE or ST pin	-10	–	–	μA
T _{pu}	Power Up Time	Time from minimum power supply voltage to the first cycle (Guaranteed no runt pulses)	–	–	10	ms

LVPECL, 3.3V $\pm 10\%$ or 2.5V $\pm 10\%$, -40 to 85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage		2.97	3.3	3.63	V
			2.25	2.5	2.75	V
I _{DD}	Supply Current	V _{DD} = 3.3, Excluding Load Termination Current	–	68	74	mA
		V _{DD} = 2.5, Excluding Load Termination Current	–	65	71	mA
V _{OH}	Output High Voltage	50 Ohm termination to V _{DD} - 2.0V	V _{DD} -1.1	–	V _{DD} -0.7	V
V _{OL}	Output Low Voltage	See Figure 2, 3.	V _{DD} -2.0	–	V _{DD} -1.4	V
V _{swing}	Pk-Pk Output Voltage Swing		600	800	1000	mV

HCSL, 3.3V $\pm 10\%$ or 2.5V $\pm 10\%$, -40 to 85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage		2.97	3.3	3.63	V
			2.25	2.5	2.75	V
I _{DD}	Supply Current	V _{DD} = 3.3, Excluding Load Termination Current	–	65	70	mA
		V _{DD} = 2.5, Excluding Load Termination Current	–	62	67	mA
V _{OH}	Output High Voltage	50 Ohm termination to GND	600	–	950	mV
V _{OL}	Output Low Voltage	See Figure 4.	0.0	–	50	mV
V _{swing}	Pk-Pk Output Voltage Swing		600	–	950	mV

LVDS, 3.3V $\pm 10\%$ or 2.5V $\pm 10\%$, -40 to 85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage		2.97	3.3	3.63	V
			2.25	2.5	2.75	V
I _{DD}	Supply Current	V _{DD} = 3.3, Excluding Load Termination Current	–	73	79	mA
		V _{DD} = 2.5, Excluding Load Termination Current	–	70	76	mA
V _{OD1}	Differential Output Voltage	Swing Mode = Normal	250	350	450	mV
ΔV _{OD1}	V _{OD} Magnitude Change	Single load termination. See Figure 5.	–	–	50	mV
V _{OS1}	Offset Voltage		–	1.2	–	V
ΔV _{OS1}	V _{OS} Magnitude Change		–	–	50	mV
V _{OD2}	Differential Output Voltage	Swing Mode = High	500	700	900	mV
ΔV _{OD2}	V _{OD} Magnitude Change	Single load termination. See Figure 5.	–	–	50	mV
V _{OS2}	Offset Voltage		–	1.2	–	V
ΔV _{OS2}	V _{OS} Magnitude Change		–	–	50	mV
V _{OD3}	Differential Output Voltage	Swing Mode = High	250	350	450	mV
ΔV _{OD3}	V _{OD} Magnitude Change	Double load termination. See Figure 6.	–	–	50	mV
V _{OS3}	Offset Voltage		–	1.2	–	V
ΔV _{OS3}	V _{OS} Magnitude Change		–	–	50	mV

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CML, 3.3V $\pm 10\%$ or 2.5V $\pm 10\%$ or 1.8V $\pm 5\%$, -40 to 85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage		2.97	3.3	3.63	V
			2.25	2.5	2.75	V
			1.71	1.8	1.89	V
I _{DD}	Supply Current	V _{DD} = 3.3V	Excluding Load Termination Current	48	51	mA
		V _{DD} = 2.5V		47	50	mA
		V _{DD} = 1.8V		38	41	mA
V _{OH1}	Output High Voltage	Swing Mode = Normal Single Load Termination See Figure 7.	V _{DD} -0.1	—	V _{DD}	V
V _{OL1}	Output Low Voltage		V _{DD} -0.55	V _{DD} -0.425	V _{DD} -0.3	V
V _{swing1}	Pk-Pk Output Voltage Swing		300	425	550	mV
V _{OH2}	Output High Voltage	Swing Mode = High Single Load Termination See Figure 7.	V _{DD} -0.1	—	V _{DD}	V
V _{OL2}	Output Low Voltage		V _{DD} -1.1	V _{DD} -0.85	V _{DD} -0.6	V
V _{swing2}	Pk-Pk Output Voltage Swing		600	850	1100	mV
V _{OH3}	Output High Voltage	Swing Mode = High Double Load Termination See Figure 8.	V _{DD} -0.1	—	V _{DD}	V
V _{OL3}	Output Low Voltage		V _{DD} -0.55	V _{DD} -0.425	V _{DD} -0.3	V
V _{swing3}	Pk-Pk Output Voltage Swing		300	425	550	mV

AC Electrical Specifications

LVPECL, 3.3V $\pm 10\%$, -40 to 85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F _{out}	Output Frequency		1.0	—	220	MHz
F _{stab}	Frequency Stability	Inclusive of initial stability, operating temp., rated power supply voltage change, load change	0 to 70°C	—	+10	PPM
			-20 to 70°C	—	+15	PPM
			-40 to 85°C	—	+20	PPM
			—	—	+25	PPM
			—	—	+50	PPM
F _{age}	Aging	First year @ 25°C	—	—	1	PPM
DC	Duty Cycle		45	—	55	%
t _R /t _F	Output Rise/Fall Time	20% to 80%	100	150	300	ps
PH _J	RMS Phase Jitter (random)	F _{out} = 106.25 MHz @ BW: 637 kHz to 10 MHz	—	1.6	—	ps
		F _{out} = 156.25 MHz @ BW: 1.875 to 20 MHz	—	0.5	—	ps
		F _{out} = 200 MHz @ BW: 1 to 20 MHz	—	0.7	—	ps
P _J	RMS Period Jitter	F _{out} = 106.25 MHz	—	1.8	2.3	ps
		F _{out} = 156.25 MHz	—	1.3	1.8	ps
		F _{out} = 200 MHz	—	1.3	1.8	ps

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LVPECL / HCSL / LVDS / CML

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LVPECL, 2.5V $\pm 10\%$, -40 to 85°C

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
F _{out}	Output Frequency			1.0	–	220	MHz
F _{stab}	Frequency Stability	Inclusive of initial stability, operating temp., rated power supply voltage change, load change	0 to 70°C	-10	–	+10	PPM
			-20 to 70°C -40 to 85°C	-15	–	+15	PPM
				-20	–	+20	PPM
				-25		+25	PPM
				-50		+50	PPM
F _{age}	Aging	First year @ 25°C		–	–	1	PPM
DC	Duty Cycle			45	–	55	%
t _R /t _F	Output Rise/Fall Time	20% to 80%		100	150	300	ps
PH _J	RMS Phase Jitter (random)	F _{out} = 106.25 MHz @ BW: 637 kHz to10 MHz		–	1.6	–	ps
		F _{out} = 156.25 MHz @ BW: 1.875 to 20 MHz		–	0.5	–	ps
		F _{out} = 200 MHz @ BW: 1 to 20 MHz		–	0.7	–	ps
P _J	RMS Period Jitter	F _{out} = 106.25 MHz		–	1.8	2.3	ps
		F _{out} = 156.25 MHz		–	1.3	1.8	ps
		F _{out} = 200 MHz		–	1.3	1.8	ps

HCSL, 3.3V $\pm 10\%$, -40 to 85°C

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
F _{out}	Output Frequency			1.0	–	220	MHz
F _{stab}	Frequency Stability	Inclusive of initial stability, operating temp., rated power supply voltage change, load change	0 to 70°C	-10	–	+10	PPM
			-20 to 70°C	-15	–	+15	PPM
			-40 to 85°C	-20	–	+20	PPM
				-25		+25	PPM
				-50		+50	PPM
F _{age}	Aging	First year @ 25°C		–	–	1	PPM
DC	Duty Cycle			45	–	55	%
t _R /t _F	Output Rise/Fall Time	20% to 80%		200	280	375	ps
PH _J	RMS Phase Jitter (random)	F _{out} = 100 MHz @ BW: 1.5 MHz to 22 MHz		–	0.8	–	ps
		F _{out} = 200 MHz @ BW: 1.5 MHz to 22 MHz		–	0.4	–	ps
P _J	RMS Period Jitter	F _{out} = 100 MHz		–	1.6	2.2	ps
		F _{out} = 200 MHz		–	1.5	1.9	ps

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HCSL, 2.5V $\pm 10\%$, -40 to 85°C

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
F _{out}	Output Frequency			1.0	–	220	MHz
F _{stab}	Frequency Stability	Inclusive of initial stability, operating temp., rated power supply voltage change, load change	0 to 70°C	-10	–	+10	PPM
			-20 to 70°C	-15	–	+15	PPM
			-40 to 85°C	-20	–	+20	PPM
				-25		+25	PPM
				-50		+50	PPM
F _{age}	Aging	First year @ 25°C		–	–	1	PPM
DC	Duty Cycle			45	–	55	%
t _R /t _F	Output Rise/Fall Time	20% to 80%		200	300	400	ps
PH _J	RMS Phase Jitter (random)	F _{out} = 100 MHz @ BW: 1.5 MHz to 22 MHz		–	0.8	–	ps
		F _{out} = 200 MHz @ BW: 1.5 MHz to 22 MHz		–	0.4	–	ps
P _J	RMS Period Jitter	F _{out} = 100 MHz		–	1.6	2.2	ps
		F _{out} = 200 MHz		–	1.5	2.1	ps

LVDS, 3.3V $\pm 10\%$, -40 to 85°C

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
F _{out}	Output Frequency			10	–	220	MHz
F _{stab}	Frequency Stability	Inclusive of initial stability, operating temp., rated power supply voltage change, load change	0 to 70°C	-10	–	+10	PPM
			-20 to 70°C	-15	–	+15	PPM
			-40 to 85°C	-20	–	+20	PPM
				-25		+25	PPM
				-50		+50	PPM
F _{age}	Aging	First year @ 25°C		–	–	1	PPM
DC	Duty Cycle			45	–	55	%
t _R /t _F	Output Rise/Fall Time	20% to 80%		100	200	325	ps
PH _J	RMS Phase Jitter (random)	F _{out} = 106.25 MHz @ BW: 637 kHz to 10 MHz		–	1.7	–	ps
		F _{out} = 156.25 MHz @ BW: 1.875 to 20 MHz		–	0.7	–	ps
		F _{out} = 200 MHz @ BW: 1 to 20 MHz		–	0.7	–	ps
P _J	RMS Period Jitter	F _{out} = 106.25 MHz		–	2.0	2.7	ps
		F _{out} = 156.25 MHz		–	1.8	2.5	ps
		F _{out} = 200 MHz		–	1.8	2.5	ps

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LVDS, 2.5V $\pm 10\%$, -40 to 85°C

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
F _{out}	Output Frequency			1.0	–	220	MHz
F _{stab}	Frequency Stability	Inclusive of initial stability, operating temp., rated power supply voltage change, load change	0 to 70°C	-10	–	+10	PPM
			-20 to 70°C -40 to 85°C	-15	–	+15	PPM
				-20	–	+20	PPM
				-25		+25	PPM
				-50		+50	PPM
F _{age}	Aging	First year @ 25°C		–	–	1	PPM
DC	Duty Cycle			45	–	55	%
t _R /t _F	Output Rise/Fall Time	20% to 80%		100	260	325	ps
PH _J	RMS Phase Jitter (random)	F _{out} = 106.25 MHz @ BW: 637 kHz to10 MHz		–	1.7	–	ps
		F _{out} = 156.25 MHz @ BW: 1.875 to 20 MHz		–	0.7	–	ps
		F _{out} = 200 MHz @ BW: 1 to 20 MHz		–	0.7	–	ps
P _J	RMS Period Jitter	F _{out} = 106.25 MHz		–	2.5	3.3	ps
		F _{out} = 156.25 MHz		–	2.4	3.5	ps
		F _{out} = 200 MHz		–	2.4	3.5	ps

CML, 3.3V $\pm 10\%$, -40 to 85°C

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
F _{out}	Output Frequency			1.0	–	220	MHz
F _{stab}	Frequency Stability	Inclusive of initial stability, operating temp., rated power supply voltage change, load change	0 to 70°C	-10	–	+10	PPM
			-20 to 70°C -40 to 85°C	-15	–	+15	PPM
				-20	–	+20	PPM
				-25		+25	PPM
				-50		+50	PPM
F _{age}	Aging	First year @ 25°C		–	–	1	PPM
DC	Duty Cycle			45	–	55	%
t _R /t _F	Output Rise/Fall Time	20% to 80%		150	220	300	ps
PH _J	RMS Phase Jitter (random)	F _{out} = 106.25 MHz @ BW: 637 kHz to10 MHz		–	1.6	–	ps
		F _{out} = 156.25 MHz @ BW: 1.875 to 20 MHz		–	0.6	–	ps
		F _{out} = 200 MHz @ BW: 1 to 20 MHz		–	0.8	–	ps
P _J	RMS Period Jitter	F _{out} = 106.25 MHz		–	2	2.5	ps
		F _{out} = 156.25 MHz		–	1.9	2.5	ps
		F _{out} = 200 MHz		–	1.9	2.4	ps

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CML, 2.5V $\pm$ 10%, -40 to 85°C

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
F _{out}	Output Frequency			1.0	–	220	MHz
F _{stab}	Frequency Stability	Inclusive of initial stability, operating temp., rated power supply voltage change, load change	0 to 70°C	-10	–	+10	PPM
			-20 to 70°C -40 to 85°C	-15	–	+15	PPM
				-20	–	+20	PPM
				-25		+25	PPM
				-50		+50	PPM
F _{age}	Aging	First year @ 25°C		–	–	1	PPM
DC	Duty Cycle			45	–	55	%
t _R /t _F	Output Rise/Fall Time	20% to 80%		150	230	300	ps
PH _J	RMS Phase Jitter (random)	F _{out} = 106.25 MHz @ BW: 637 kHz to10 MHz		–	1.6	–	ps
		F _{out} = 156.25 MHz @ BW: 1.875 to 20 MHz		–	0.6	–	ps
		F _{out} = 200 MHz @ BW: 1 to 20 MHz		–	0.8	–	ps
P _J	RMS Period Jitter	F _{out} = 106.25 MHz		–	2.1	2.5	ps
		F _{out} = 156.25 MHz		–	1.9	2.5	ps
		F _{out} = 200 MHz		–	1.9	2.5	ps

CML, 1.8V $\pm$ 5%, -40 to 85°C

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
F _{out}	Output Frequency			1.0	–	220	MHz
F _{stab}	Frequency Stability	Inclusive of initial stability, operating temp., rated power supply voltage change, load change	0 to 70°C	-15	–	+15	PPM
			-20 to 70°C	-20	–	+20	PPM
			-40 to 85°C	-25		+25	PPM
				-50		+50	PPM
F _{age}	Aging	First year @ 25°C		–	–	1	PPM
DC	Duty Cycle			45	–	55	%
t _R /t _F	Output Rise/Fall Time	20% to 80%		150	240	325	ps
PH _J	RMS Phase Jitter (random)	F _{out} = 106.25 MHz @ BW: 637 kHz to10 MHz		–	1.7	–	ps
		F _{out} = 156.25 MHz @ BW: 1.87 to 20 MHz		–	0.6	–	ps
		F _{out} = 200 MHz @ BW: 1 to 20 MHz		–	0.8	–	ps
P _J	RMS Period Jitter	F _{out} = 106.25 MHz		–	2.3	2.9	ps
		F _{out} = 156.25 MHz		–	2.1	2.7	ps
		F _{out} = 200 MHz		–	2.1	2.7	ps

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Termination Diagrams

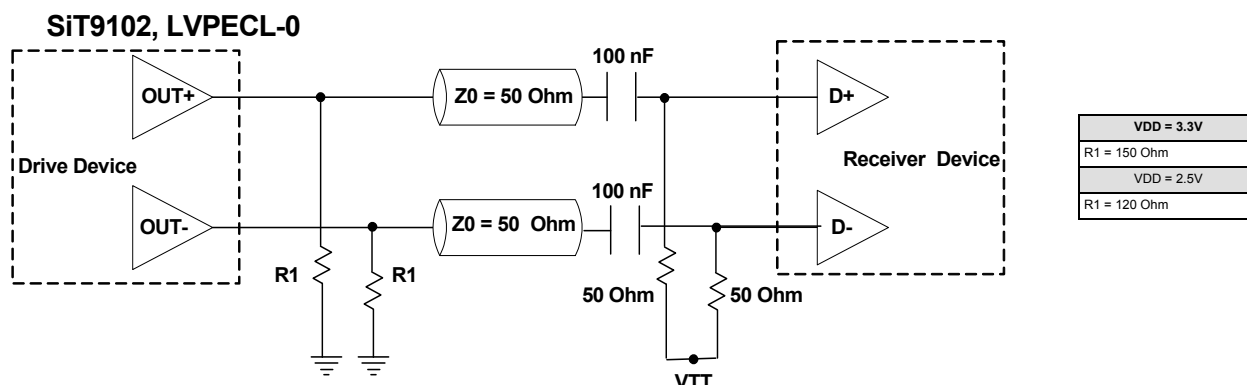


Figure 1. LVPECL AC Coupled Typical Termination

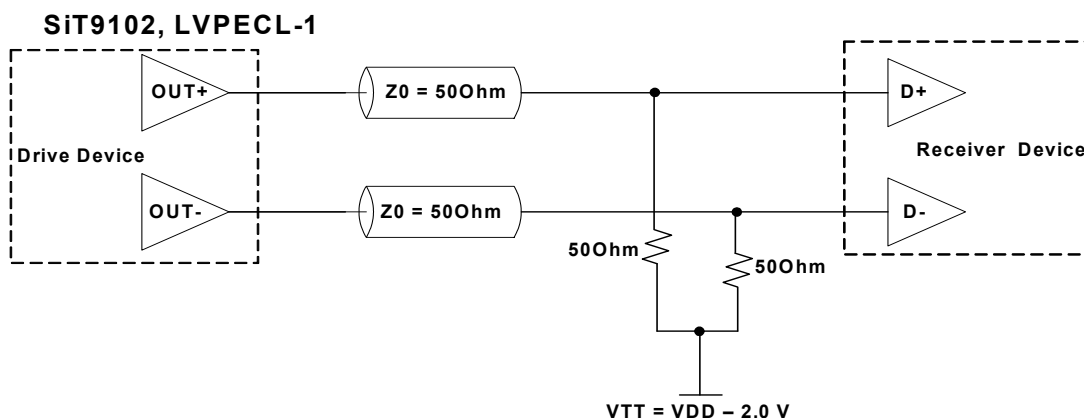


Figure 2. LVPECL DC Coupled Typical Termination with Termination Voltage

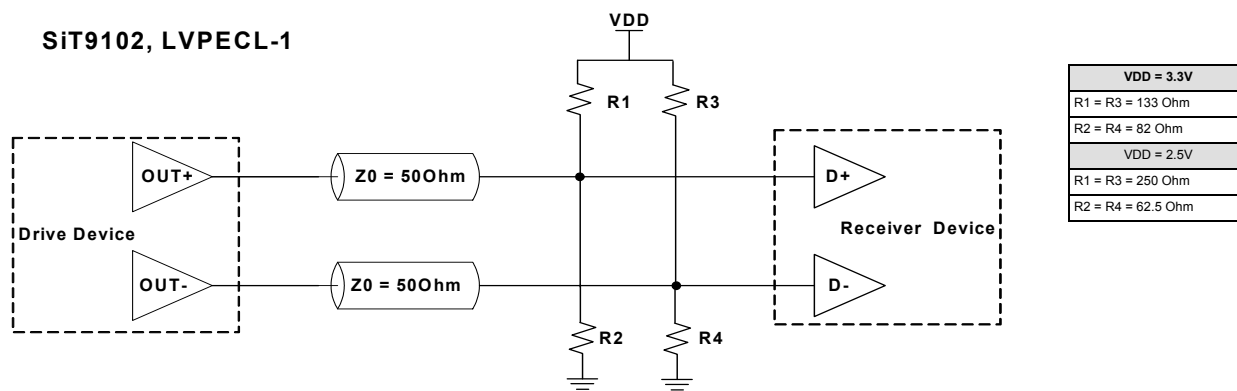


Figure 3. LVPECL DC Coupled Typical Termination without Termination Voltage

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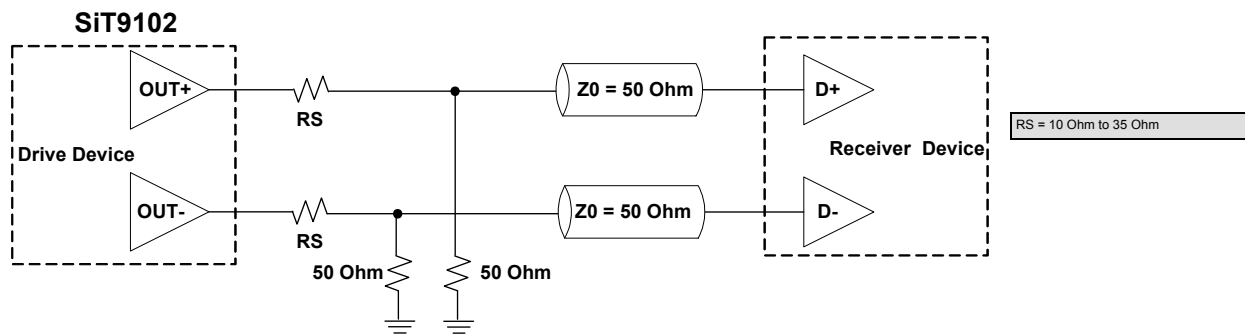


Figure 4. HCSL Typical Termination

Note:

1. All the tests are done with RS = 20 Ohm (recommended).

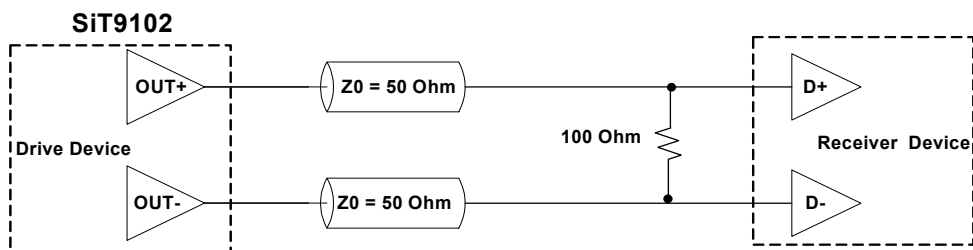
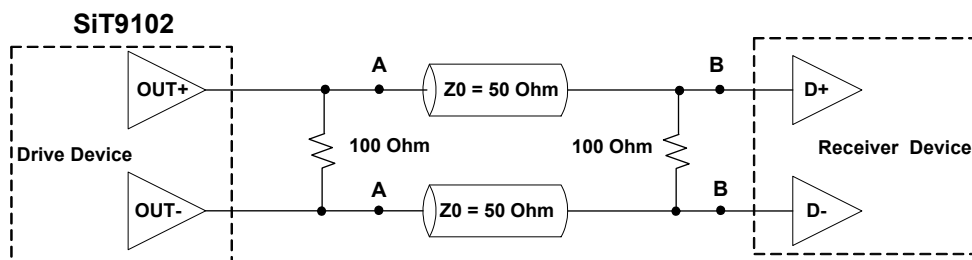


Figure 5. LVDS Single Termination (Load Terminated)



Note: For AC coupled operation, include/insert decoupling caps at points A or B

Figure 6. LVDS Double Termination (Source + Load Terminated)

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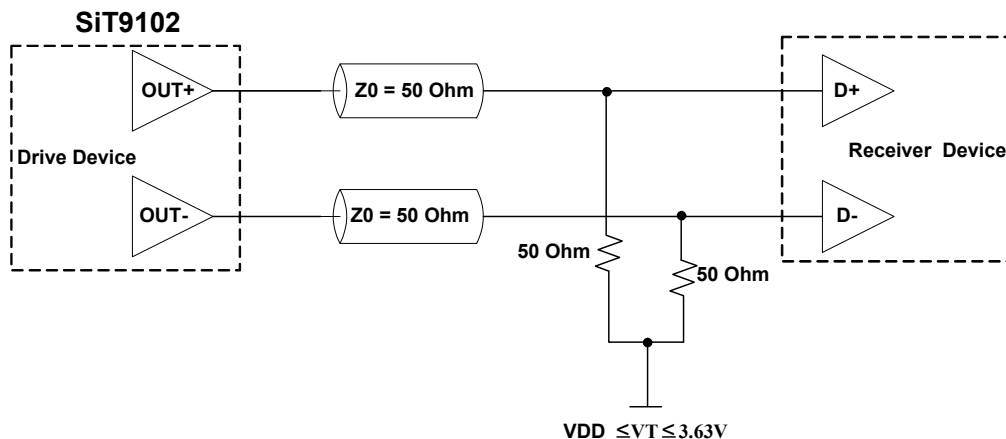
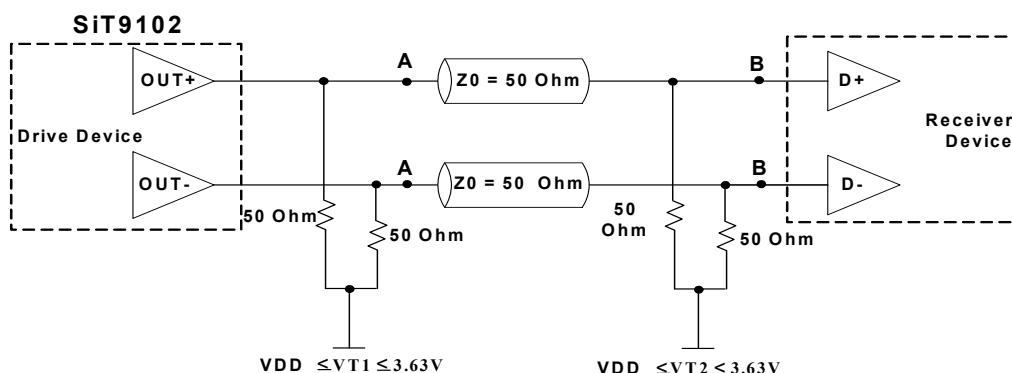


Figure 7. CML Single Load Termination



Notes:

1. For DC-coupled operation, $VT1 = VT2$
2. For AC coupled operation, include/insert decoupling caps at points A or B
2. For AC-coupled operation with capacitors placed at point A, $VT2$ sets the input common mode of Receiver Device and need not to be related to $VT1$

Figure 8. CML Double Load Termination

SiT9102

LVPECL / HCSL / LVDS / CML

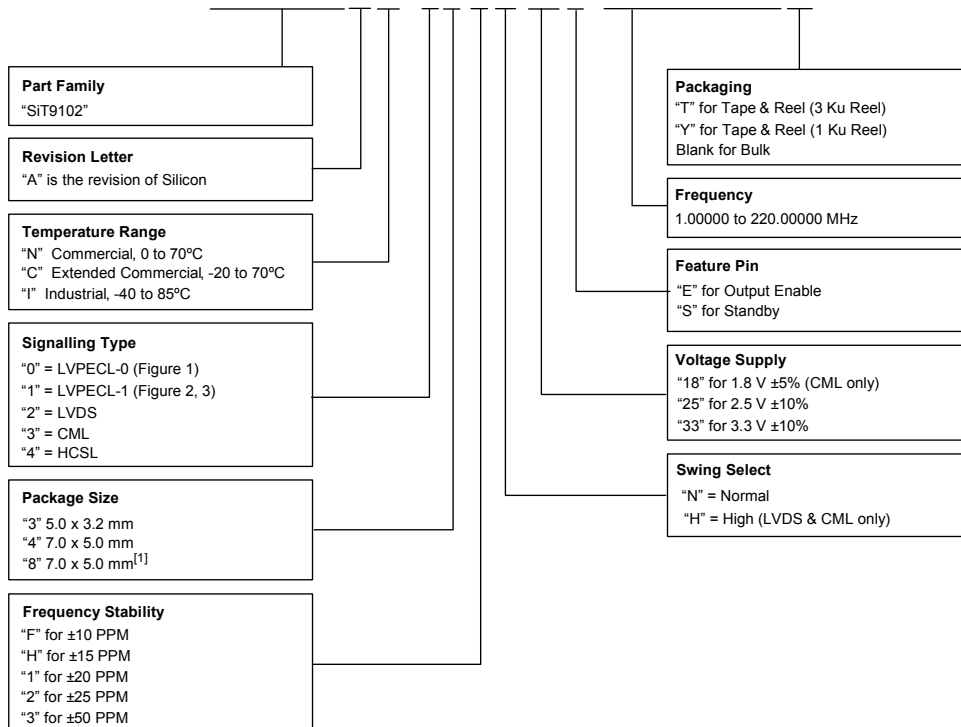
1 to 220 MHz High Performance Oscillator



Ordering Information

The Part No. Guide is for reference only. For real-time customization and exact part number, use the SiTime [Part Number Generator](#).

SiT9102AC-132N33E123.12345T



Frequency Stability vs. Temperature Range Options

Frequency Stability (PPM)	Temperature Range	Supply Voltage		
		1.8 V	2.5 V	3.3 V
±10	N (0 to +70°C)	–	✓	✓
	C (-20 to +70°C)	–	–	–
	I (-40 to +85°C)	–	–	–
±15	N (0 to +70°C)	✓	✓	✓
	C (-20 to +70°C)	–	✓	✓
	I (-40 to +85°C)	–	✓	✓
±20	N (0 to +70°C)	✓	✓	✓
	C (-20 to +70°C)	✓	✓	✓
	I (-40 to +85°C)	✓	✓	✓
±25	N (0 to +70°C)	✓	✓	✓
	C (-20 to +70°C)	✓	✓	✓
	I (-40 to +85°C)	✓	✓	✓
±50	N (0 to +70°C)	✓	✓	✓
	C (-20 to +70°C)	✓	✓	✓
	I (-40 to +85°C)	✓	✓	✓

Note:

1. Without Center Pad.

Signaling Type vs. Swing Select Options

Signaling Type	Swing Select	Supply Voltage		
		1.8 V	2.5 V	3.3 V
LVPECL-0	Normal	–	✓	✓
	High	–	–	–
LVPECL-1	Normal	–	✓	✓
	High	–	–	–
LVDS	Normal	–	✓	✓
	High	–	✓	✓
CML	Normal	✓	✓	✓
	High	✓	✓	✓
HCSL	Normal	–	✓	✓
	High	–	–	–

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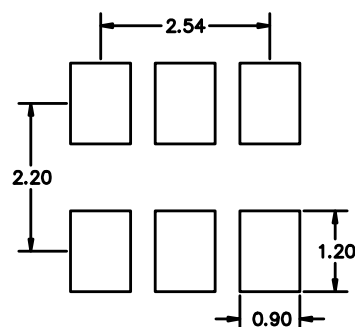
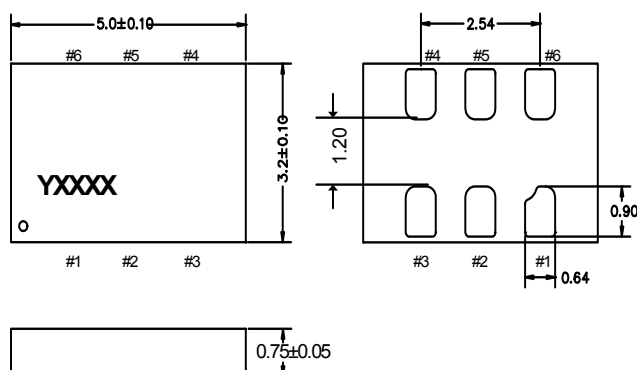


Package Information [2]

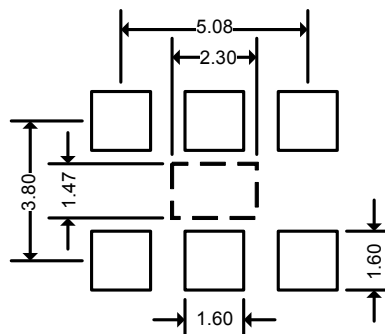
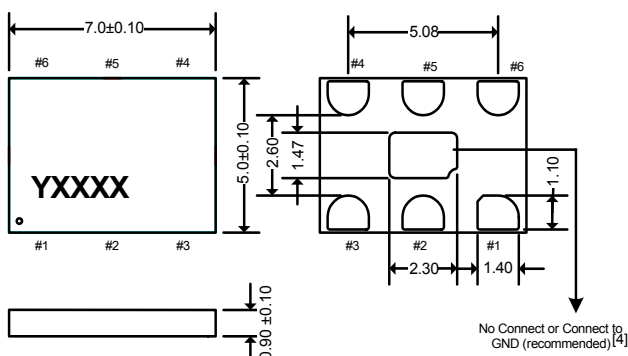
Dimension (mm)

Land Pattern [3] (recommended) (mm)

5.0 x 3.2 x 0.75mm



7.0 x 5.0 x 0.90mm



Notes:

2. "Y" denotes manufacturing origin and "XXX" denotes manufacturing lot number. The value of "Y" depend on the assembly location of the device.
3. A capacitor of value 0.1μF between VDD and GND is recommended.
4. The 7050 package with part number designation "-8" has NO center pad.

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