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[VBUS053BZ-HNH-G-08](#)

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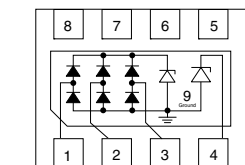
sales@integrated-circuit.com



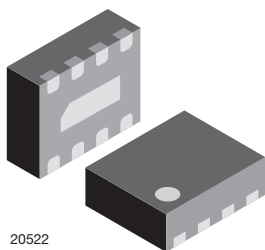
VBUS053BZ-HNH

Vishay Semiconductors

USB-OTG BUS-Port ESD-Protection for $V_{BUS} = 12\text{ V}$



21765



20522

MARKING (example only)



20719

Dot = pin 1 marking
 YY = type code (see table below)
 XX = date code

FEATURES

- Ultra compact LLP1713-9L package
- Low package height < 0.6 mm
- 3-line USB ESD-protection with max. working range = 5.5 V
- V_{BUS} - protection with 12 V working range
- Low leakage current
- Low load capacitance $C_D = 0.7\text{ pF}$
- ESD-protection acc. IEC 61000-4-2
 $\pm 12\text{ kV}$ contact discharge
 $\pm 15\text{ kV}$ air discharge
- Surge current acc. IEC 61000-4-5 $I_{PP} > 3\text{ A}$
- e4 - precious metal (e.g. Ag, Au, NiPd, NiPdAu) (no Sn)
- Compliant to RoHS Directive 2002/95/EC and in accordance to WEEE 2002/96/EC



ORDERING INFORMATION			
DEVICE NAME	ORDERING CODE	TAPED UNITS PER REEL (8 mm TAPE ON 7" REEL)	MINIMUM ORDER QUANTITY
VBUS053BZ-HNH	VBUS053BZ-HNH-G-08	3000	15 000

PACKAGE DATA						
DEVICE NAME	PACKAGE NAME	TYPE CODE	WEIGHT	MOLDING COMPOUND FLAMMABILITY RATING	MOISTURE SENSITIVITY LEVEL	SOLDERING CONDITIONS
VBUS053BZ-HNH	LLP1713-9L	K	3.7 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	260 °C/10 s at terminals

ABSOLUTE MAXIMUM RATINGS VBUS053BZ-HNH					
RATING	TEST CONDITIONS	SYMBOL	VALUE	UNIT	
Data line D+, D-, ID: Pin 1, 2 and 3 to ground (pin 9)					
Peak pulse current	acc. IEC 61000-4-5, $t_p = 8/20\ \mu\text{s}/\text{single shot}$	I_{PPM}	3	A	
Peak pulse power	acc. IEC 61000-4-5, $t_p = 8/20\ \mu\text{s}/\text{single shot}$	P_{PP}	36	W	
ESD immunity	Contact discharge acc. IEC 61000-4-2; 10 pulses	V_{ESD}	± 12	kV	
	Air discharge acc. IEC 61000-4-2; 10 pulses		± 15	kV	
V_{BUS}: Pin 4 to ground (pin 9)					
Peak pulse current	acc. IEC 61000-4-5, $t_p = 8/20\ \mu\text{s}/\text{single shot}$	I_{PPM}	8	A	
Peak pulse power	acc. IEC 61000-4-5, $t_p = 8/20\ \mu\text{s}/\text{single shot}$	P_{PP}	240	W	
ESD immunity	Contact discharge acc. IEC 61000-4-2; 10 pulses	V_{ESD}	± 30	kV	
	Air discharge acc. IEC 61000-4-2; 10 pulses		± 30	kV	
Operating temperature	Junction temperature	T_J	- 40 to + 125	°C	
Storage temperature		T_{stg}	- 55 to + 150	°C	

** Please see document "Vishay Material Category Policy": www.vishay.com/doc?99902

VBUS053BZ-HNH



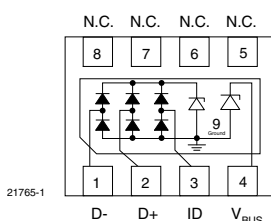
Vishay Semiconductors USB-OTG BUS-Port ESD-Protection
 for $V_{BUS} = 12\text{ V}$

APPLICATION NOTE

The VBUS053BZ-HNH is intended as an ESD-protection and transient voltage suppressor for one USB-OTG port. The LLP1713-9L package contains two separate dies which are mounted on a common ground plane (pin 9). The high-speed data lines D-, D+ and ID, are connected to any of the pins no. 1 to 3. As long as the signal voltage on the data lines is between the ground- and the 5 V working range, the low capacitance PN-diodes offer a very high isolation to ground and to the other data lines. But as soon as any transient signal like an ESD-signal, exceeds this working range of 5 V in either the positive or negative direction, one of the PN-diodes gets into the forward mode and clamps the transient either to ground or to the avalanche break through level.

An extra avalanche diode (separate die) clamps the supply line voltage (V_{BUS} at pin 4) above the 12 V working range to ground (pin 9).

Due to the “two die construction” the V_{BUS} line has a very high isolation to the data lines. In case of a destructive transient signal, i.e. coming from a charger, the data lines will not be influenced.



Remark:

The input pins no. 1, 2 and 3 are symmetrical. Each of the data signals D-, D+ and ID can be connected to pin 1, 2 or 3.

ELECTRICAL CHARACTERISTICS VBUS053BZ-HNH						
PARAMETER	TEST CONDITIONS/REMARKS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Data line D+, D-, ID: Pin 1, 2 and 3 to ground (pin 9)						
Protection paths	Number of lines which can be protected	$N_{channel}$	-	-	3	lines
Reverse working voltage	at $I_R = 0.1\ \mu\text{A}$	V_{RWM}	5.5	-	-	V
Reverse current	at $V_R = V_{RWM} = 3.3\text{ V}$; $T = 65\text{ }^\circ\text{C}$	I_R	-	-	0.0085	μA
	at $V_R = V_{RWM} = 5\text{ V}$	I_R	-	-	1	μA
Forward voltage	at $I_F = 15\text{ mA}$	V_F	0.7	-	1.2	V
Reverse breakdown voltage	at $I_R = 1\text{ mA}$	V_{BR}	6.5	-	10	V
Reverse clamping voltage	at $I_{PP} = 1\text{ A}$, acc. IEC 61000-4-5; $T = 25\text{ }^\circ\text{C}$	V_C	-	10	12	V
	at $I_{PP} = 3\text{ A}$, acc. IEC 61000-4-5; $T = 25\text{ }^\circ\text{C}$	V_C	-	15	18	V
Forward clamping voltage	at $I_F = 3\text{ A}$, acc. IEC 61000-4-5;	V_F	-	3.4	4.1	V
Capacitance	Test pin at $V_R = 0\text{ V}$; any other I/O pin at $V_R = 3.3\text{ V}$; $f = 1\text{ MHz}$	C_D	-	0.7	1	pF
Symmetry	Difference of the line capacitance	dC_D	-	-	0.1	pF
Line to line capacitance	Among pins 1, 2 and 3 at $V_R = 0\text{ V}$; $f = 1\text{ MHz}$	C_{DD}	-	0.35	0.5	pF
V_{BUS}: Pin 4 to ground (pin 9)						
Protection paths	Number of lines which can be protected	$N_{channel}$	-	-	1	lines
Reverse working voltage	at $I_R = 100\text{ nA}$	V_{RWM}	12	-	-	V
Reverse current	at $V_R = V_{RWM} = 12\text{ V}$	I_R	-	-	100	nA
Forward voltage	at $I_F = 10\text{ mA}$	V_F	0.6	0.75	0.9	V
Reverse breakdown voltage	at $I_R = 1\text{ mA}$	V_{BR}	15	-	18	V
Reverse clamping voltage	at $I_{PP} = 1\text{ A}$, acc. IEC 61000-4-5; $T = 25\text{ }^\circ\text{C}$	V_C	-	17.5	20	V
	at $I_{PP} = 8\text{ A}$, acc. IEC 61000-4-5; $T = 25\text{ }^\circ\text{C}$	V_C	-	25	30	V
Forward clamping voltage	at $I_F = 8\text{ A}$, acc. IEC 61000-4-5;	V_F	-	-	2.2	V
Capacitance	at $V_R = 0\text{ V}$; $f = 1\text{ MHz}$	C_D	-	70	85	pF

Note

- Ratings at $-40\text{ }^\circ\text{C}$ to $85\text{ }^\circ\text{C}$, ambient temperature unless otherwise specified



VBUS053BZ-HNH

USB-OTG BUS-Port ESD-Protection Vishay Semiconductors
for $V_{BUS} = 12\text{ V}$

TYPICAL CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)

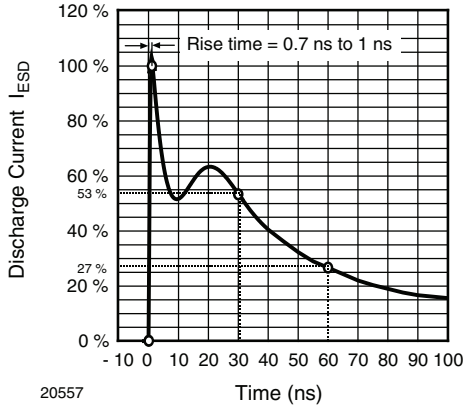


Fig. 1 - ESD Discharge Current Wave Form acc. IEC 61000-4-2 (330 Ω /150 pF)

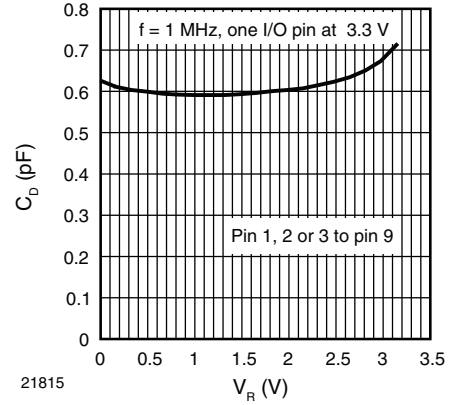


Fig. 4 - Typical Capacitance C_D vs. Reverse Voltage V_R

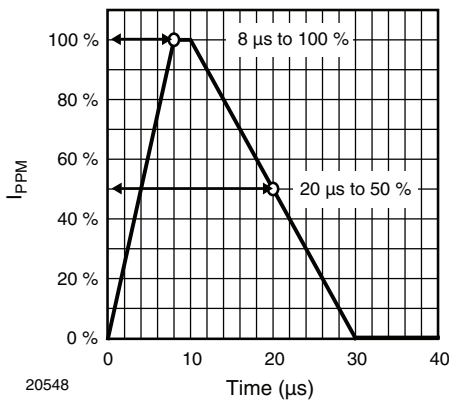


Fig. 2 - 8/20 μs Peak Pulse Current Wave Form acc. IEC 61000-4-5

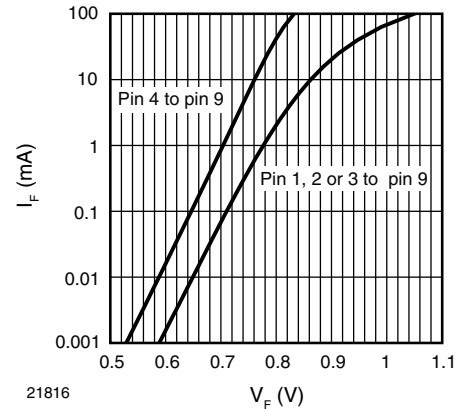


Fig. 5 - Typical Forward Current I_F vs. Forward Voltage V_F

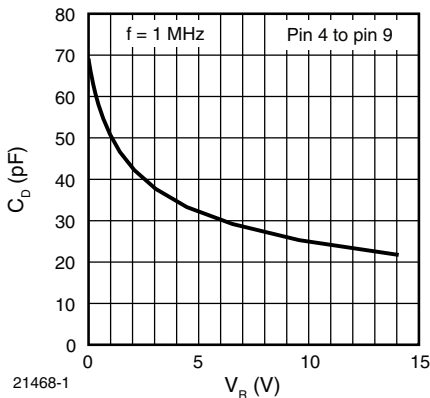


Fig. 3 - Typical Capacitance C_D vs. Reverse Voltage V_R

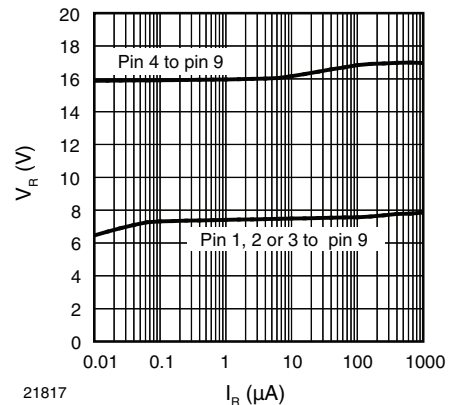


Fig. 6 - Typical Reverse Voltage V_R vs. Reverse Current I_R

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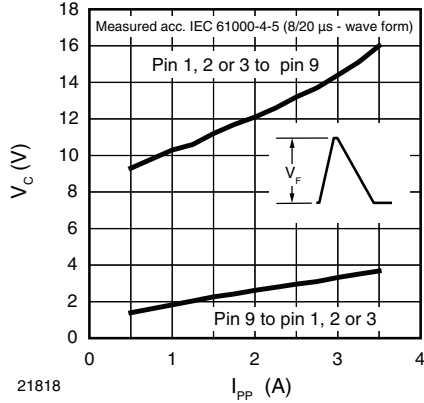


Fig. 7 - Typical Peak Clamping Voltage V_C vs. Peak Pulse Current I_{PP}

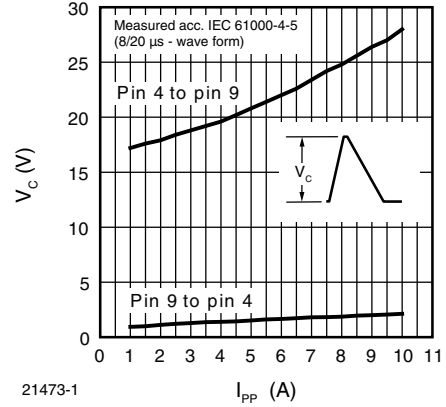
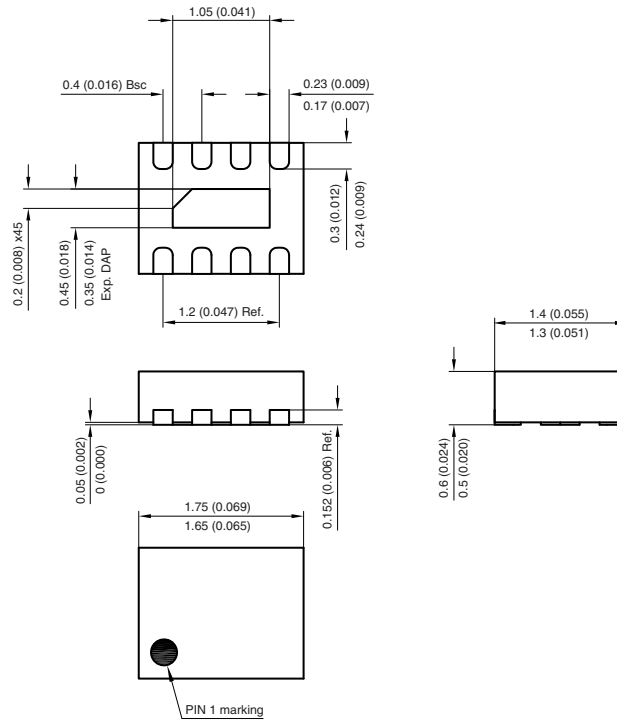
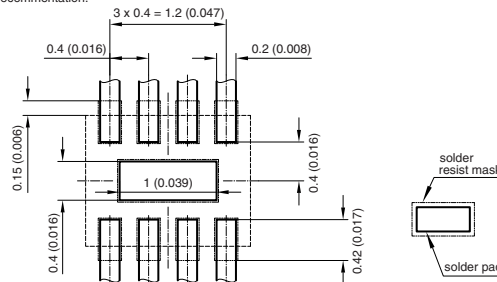


Fig. 8 - Typical Peak Clamping Voltage V_C vs. Peak Pulse Current I_{PP}

PACKAGE DIMENSIONS in millimeters (inches): LLP1713-9L



foot print recommendation:



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 21784



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