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Vishay/Siliconix
SI1308EDL-T1-GE3

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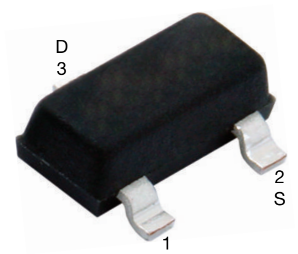
sales@integrated-circuit.com

N-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω) MAX.	I_D (A) [c]	Q_g (TYP.)
30	0.132 at V_{GS} = 10 V	1.5	1.4 nC
	0.144 at V_{GS} = 4.5 V	1.4	
	0.185 at V_{GS} = 2.5 V	1.3	

SOT-323
SC-70 (3 leads)



Top View

Marking Code: KG

Ordering Information:
Si1308EDL-T1-GE3 (Lead (Pb)-free and Halogen-free)

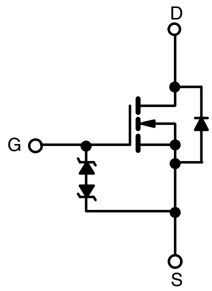
FEATURES

- TrenchFET® power MOSFET
- 100 % R_g tested
- Typical ESD performance 1800 V
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free
RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Smart phones, tablet PC's
  - DC/DC converters
    - Boost converters
  - Load switch, OVP switch



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 12	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	1.4	A
	T_C = 70 °C		1.1	
	T_A = 25 °C		1.5 [a, b]	
	T_A = 70 °C		1.2 [a, b]	
Pulsed Drain Current (t = 300 μs)		I_{DM}	6	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	0.4	
	T_A = 25 °C		0.3	
Maximum Power Dissipation	T_C = 25 °C	P_D	0.5	W
	T_C = 70 °C		0.3	
	T_A = 25 °C		0.4 [a, b]	
	T_A = 70 °C		0.3 [a, b]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +150	°C
Soldering Recommendations (Peak Temperature)			260	

THERMAL RESISTANCE RATINGS					
PARAMETER		**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient [a, d]	t ≤ 10 s	R_{thJA}	250	300	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	225	270	

Notes

a. Surface mounted on 1" x 1" FR4 board.
b. t = 10 s.
c. Based on T_C = 25 °C.
d. Maximum under steady state conditions is 360 °C/W.

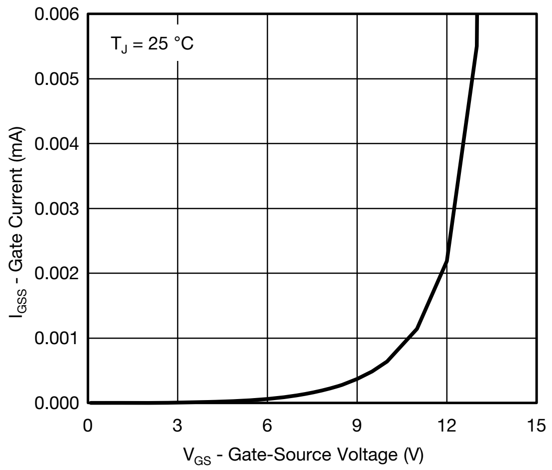
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA	30	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 μA	-	32	-	mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$		-	-3	-	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 μA	0.6	-	1.5	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = 4.5 V	-	-	1	μA
		V_{DS} = 0 V, V_{GS} = ± 12 V	-	-	± 20	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V	-	-	1	
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 55 °C	-	-	10	
On-State Drain Current [a]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = 10 V	2	-	-	A
Drain-Source On-State Resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 1.4 A	-	0.110	0.132	Ω
		V_{GS} = 4.5 V, I_D = 1 A	-	0.120	0.144	
		V_{GS} = 2.5 V, I_D = 0.5 A	-	0.142	0.185	
Forward Transconductance [a]	g_{fs}	V_{DS} = 10 V, I_D = 1.4 A	-	5	-	S
Dynamic [b]						
Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	-	105	-	pF
Output Capacitance	C_{oss}		-	23	-	
Reverse Transfer Capacitance	C_{rss}		-	11	-	
Total Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 1.4 A	-	2.7	4.1	nC
		V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 1.4 A	-	1.4	2.1	
Gate-Source Charge	Q_{gs}		-	0.3	-	
Gate-Drain Charge	Q_{gd}		-	0.5	-	
Gate Resistance	R_g	f = 1 MHz	1.4	7	14	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 13.6 Ω $I_D \cong$ 1.1 A, V_{GEN} = 10 V, R_g = 1 Ω	-	2	4	ns
Rise Time	t_r		-	9	18	
Turn-Off Delay Time	$t_{d(off)}$		-	8	16	
Fall Time	t_f		-	8	16	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 13.6 Ω $I_D \cong$ 1.1 A, V_{GEN} = 4.5 V, R_g = 1 Ω	-	8	16	
Rise Time	t_r		-	13	20	
Turn-Off Delay Time	$t_{d(off)}$		-	15	23	
Fall Time	t_f		-	6	12	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C	-	-	0.4	A
Pulse Diode Forward Current [a]	I_{SM}		-	-	6	
Body Diode Voltage	V_{SD}	I_F = 1.1 A	-	0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = 1.1 A, dI/dt = 100 A/μs, T_J = 25 °C	-	8	16	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	3	6	nC
Reverse Recovery Fall Time	t_a		-	5	-	ns
Reverse Recovery Rise Time	t_b		-	3	-	

Notes

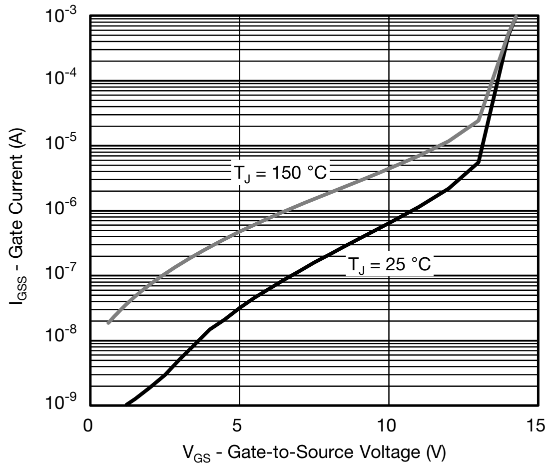
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

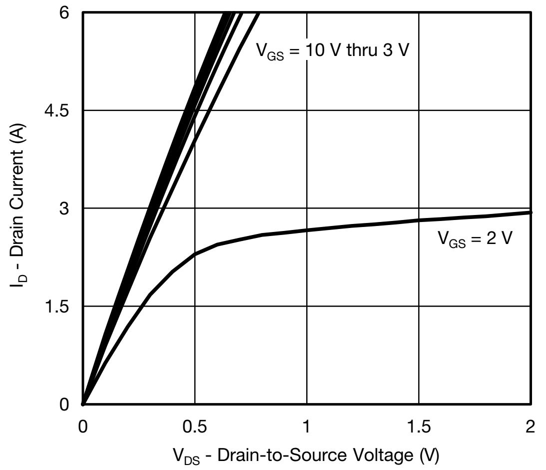
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



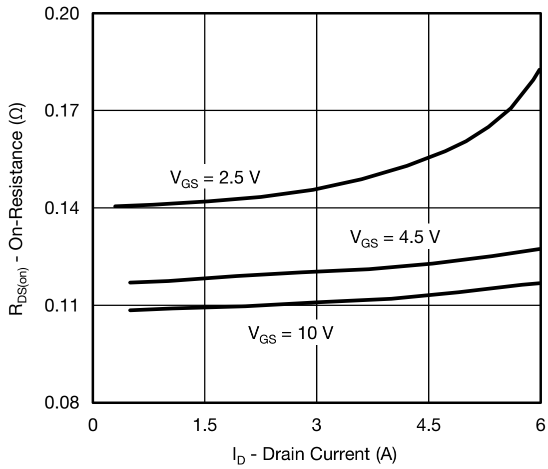
Gate Source Voltage vs. Gate Current



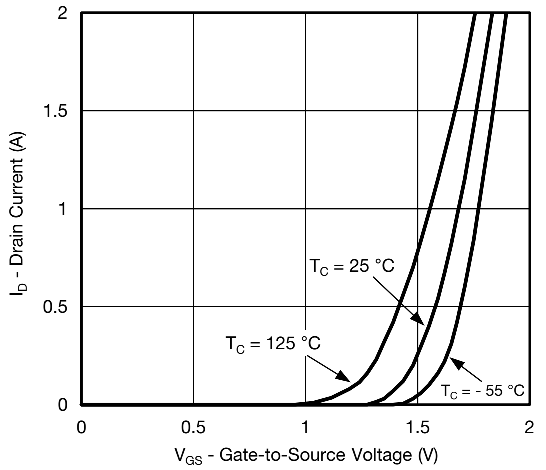
Gate Source Voltage vs. Gate Current



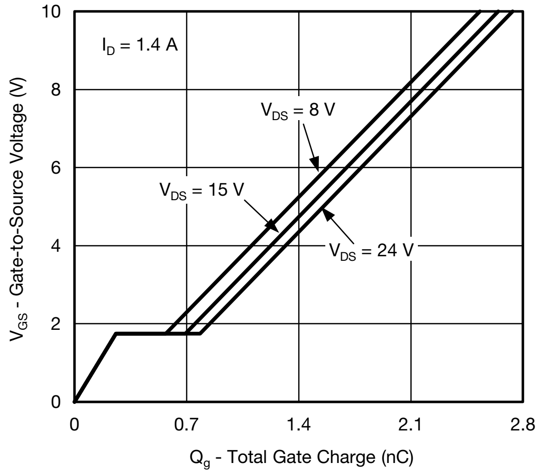
Output Characteristics



On-Resistance vs. Drain Current

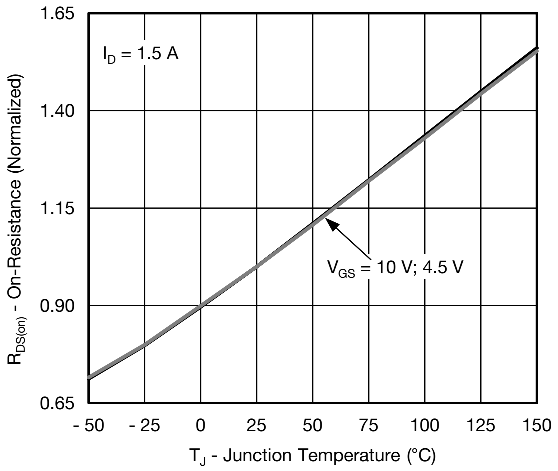


Transfer Characteristics

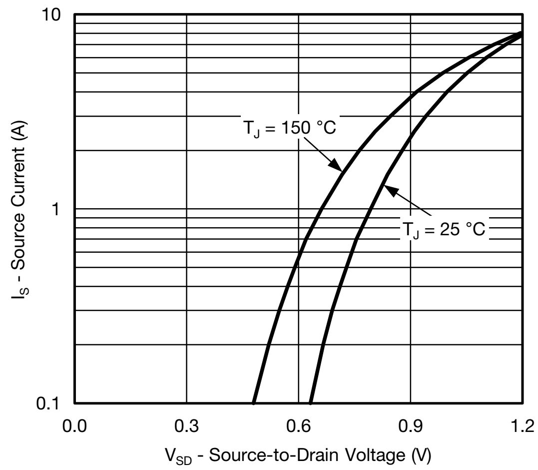


Gate Charge

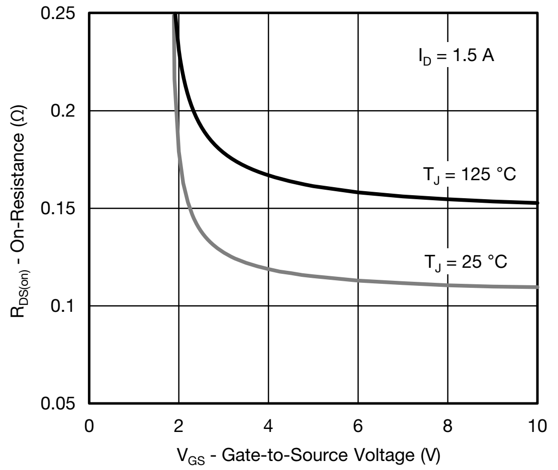
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



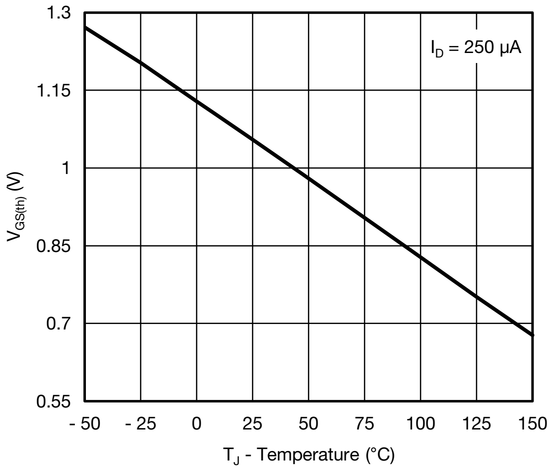
On-Resistance vs. Junction Temperature



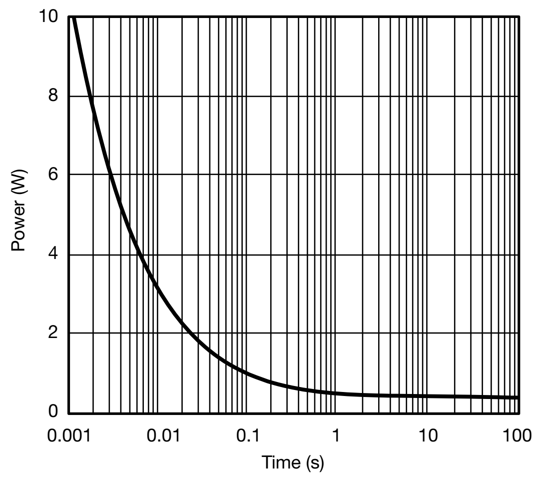
Source-Drain Diode Forward Voltage



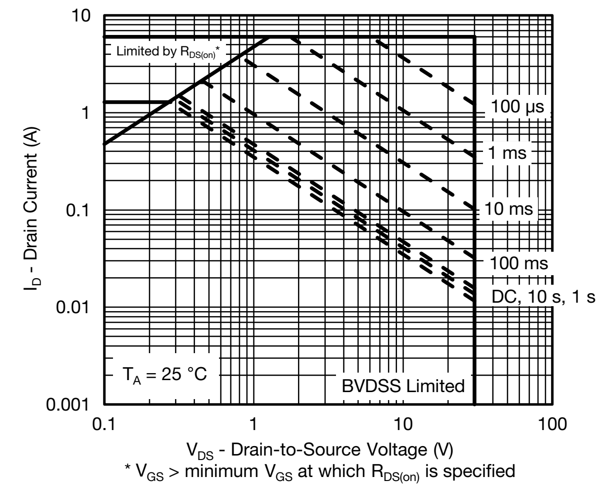
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

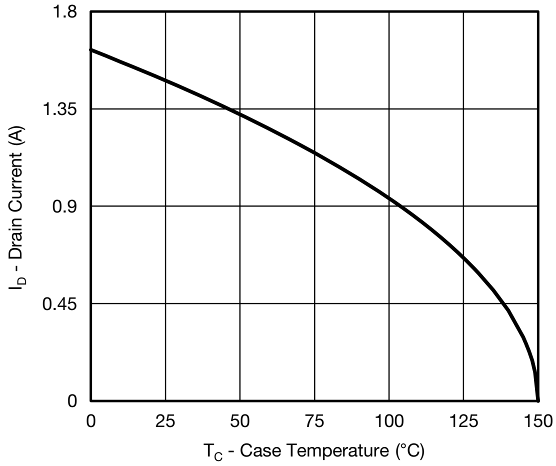


Single Pulse Power, Junction-to-Ambient

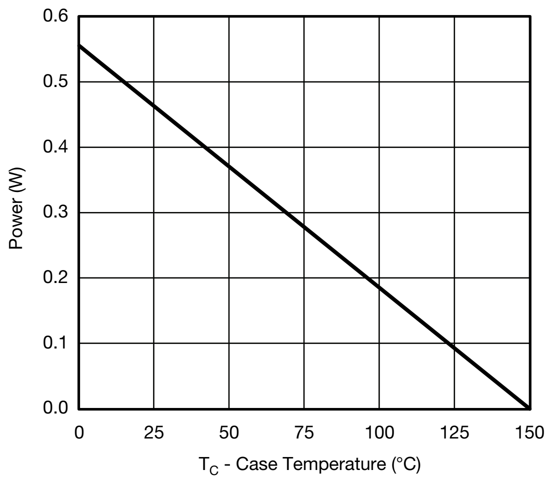


Safe Operating Area, Junction-to-Ambient

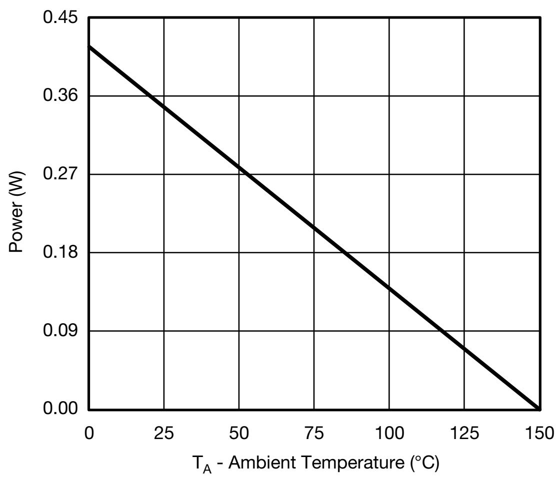
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*



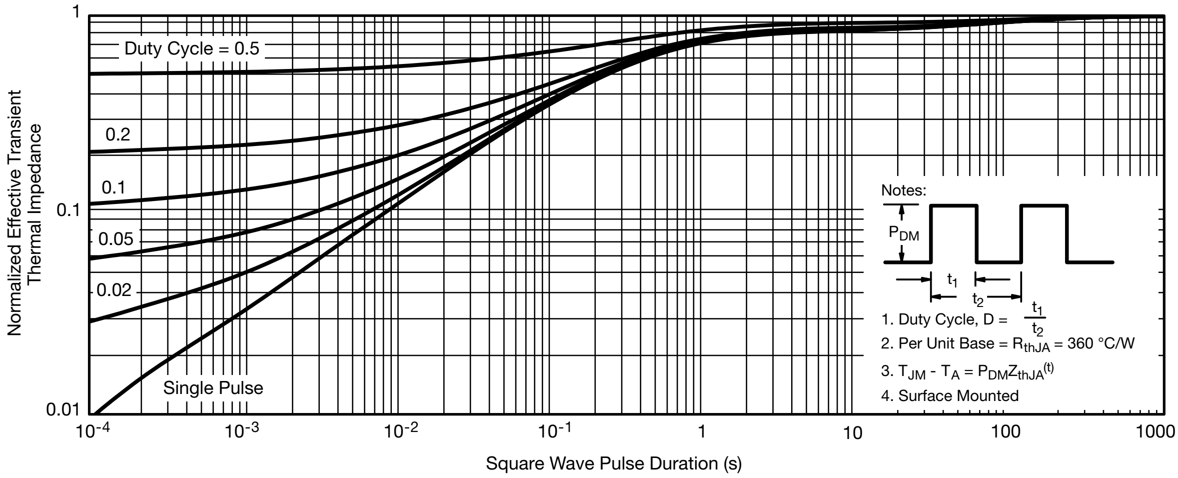
Power, Junction-to-Case



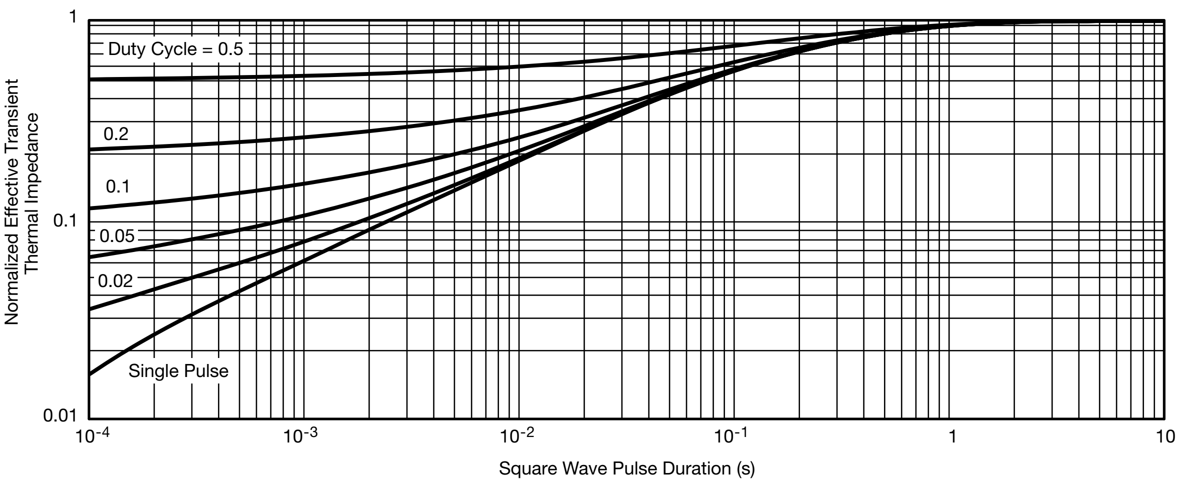
Power, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J\ (max.)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



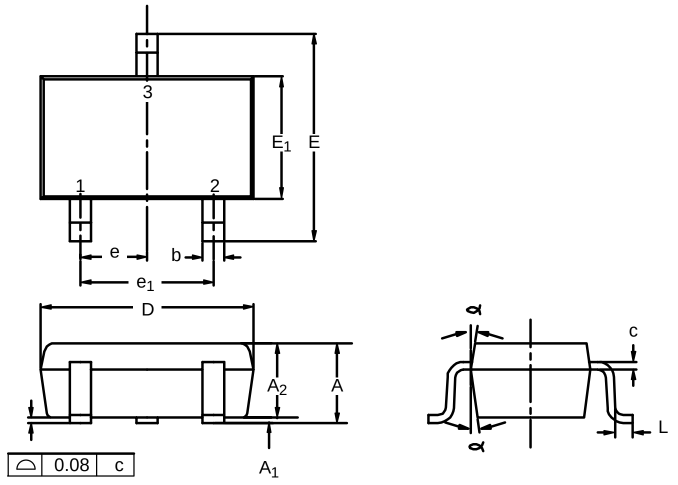
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63399.

SC-70: 3-LEADS



Dim	MILLIMETERS			INCHES		
	Min	**Nom**	**Max**	**Min**	**Nom**	**Max**
A	0.90	–	1.10	0.035	–	0.043
A_1	–	–	0.10	–	–	0.004
A_2	0.80	–	1.00	0.031	–	0.039
b	0.25	–	0.40	0.010	–	0.016
c	0.10	–	0.25	0.004	–	0.010
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E_1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65BSC			0.026BSC		
e_1	1.20	1.30	1.40	0.047	0.051	0.055
L	0.10	0.20	0.30	0.004	0.008	0.012
α	7°Nom			7°Nom		

ECN: S-03946—Rev. C, 09-Jul-01
DWG: 5549

Single-Channel LITTLE FOOT® SC-70 3-Pin and 6-Pin MOSFET Recommended Pad Pattern and Thermal Peformance

INTRODUCTION

This technical note discusses pin-outs, package outlines, pad patterns, evaluation board layout, and thermal performance for single-channel LITTLE FOOT power MOSFETs in the SC-70 package. These new Vishay Siliconix devices are intended for small-signal applications where a miniaturized package is needed and low levels of current (around 350 mA) need to be switched, either directly or by using a level shift configuration. Vishay provides these single devices with a range of on-resistance specifications and in both traditional 3-pin and new 6-pin versions. The new 6-pin SC-70 package enables improved on-resistance values and enhanced thermal performance compared to the 3-pin package.

PIN-OUT

Figure 1 shows the pin-out description and Pin 1 identification for the single-channel SC-70 device in both 3-pin and 6-pin configurations. The pin-out of the 6-pin device allows the use of four pins as drain leads, which helps to reduce on-resistance and junction-to-ambient thermal resistance.

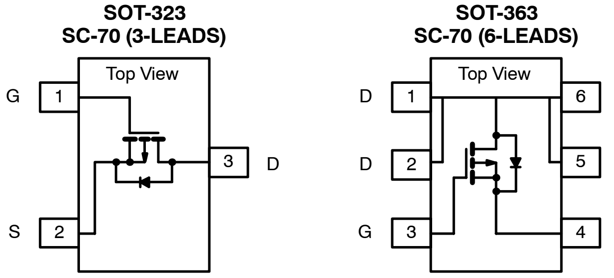


FIGURE 1.

For package dimensions see outline drawings:
SC-70 (3-Leads) (http://www.vishay.com/doc?71153)
SC-70 (6-Leads) (http://www.vishay.com/doc?71154)

BASIC PAD PATTERNS

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (http://www.vishay.com/doc?72286) for the basic pad layout and dimensions for the 3-pin SC-70 and the 6-pin SC-70. These pad patterns are sufficient for the low-power applications for which this package is intended. Increasing the pad pattern has little effect on thermal resistance for the 3-pin device, reducing it by only 10% to 15%. But for the 6-pin device, increasing the pad patterns yields a reduction in thermal resistance on the order of 35% when using a 1-inch square with full copper on both sides of the printed circuit board (PCB). The availability of four drain leads rather than the traditional single drain lead allows a better thermal path from the package to the PCB and external environment.

EVALUATION BOARDS FOR THE SINGLE SC70-3 AND SC70-6

Figure 2 shows the 3-pin and 6-pin SC-70 evaluation boards (EVB). Both measure 0.6 inches by 0.5 inches. Their copper pad traces are the same as described in the previous section, *Basic Pad Patterns*. Both boards allow interrogation from the outer pins to 6-pin DIP connections, permitting test sockets to be used in evaluation testing.

The thermal performance of the single SC-70 has been measured on the EVB for both the 3-pin and 6-pin devices, the results shown in Figures 3 and 4. The minimum recommended footprint on the evaluation board was compared with the industry standard of 1-inch square FR4 PCB with copper on both sides of the board.

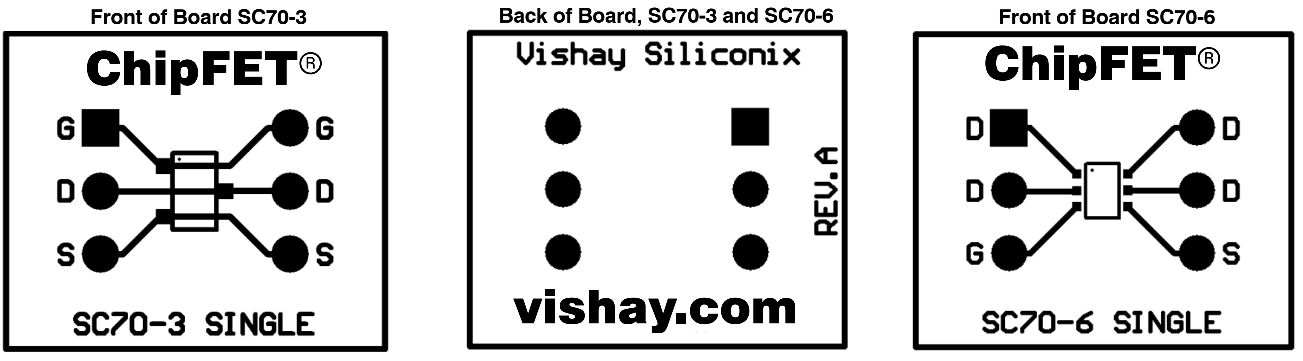


FIGURE 2.

THERMAL PERFORMANCE

Junction-to-Foot Thermal Resistance (the Package Performance)

Thermal performance for the 3-pin SC-70 measured as junction-to-foot thermal resistance is 285°C/W typical, 340°C/W maximum. Junction-to-foot thermal resistance for the 6-pin SC70-6 is 105°C/W typical, 130°C/W maximum — a nearly two-thirds reduction compared with the 3-pin device. The “foot” is the drain lead of the device as it connects with the body. This improved performance is obtained by the increase in drain leads from one to four on the 6-pin SC-70. Note that these numbers are somewhat higher than other LITTLE FOOT devices due to the limited thermal performance of the Alloy 42 lead-frame compared with a standard copper lead-frame.

Junction-to-Ambient Thermal Resistance (dependent on PCB size)

The typical $R\theta_{JA}$ for the single 3-pin SC-70 is 360°C/W steady state, compared with 180°C/W for the 6-pin SC-70. Maximum ratings are 430°C/W for the 3-pin device versus 220°C/W for the 6-pin device. All figures are based on the 1-inch square FR4 test board.The following table shows how the thermal resistance impacts power dissipation for the two different pin-outs at two different ambient temperatures.

SC-70 (3-PIN)	
Room Ambient 25 °C	Elevated Ambient 60 °C
$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$	$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$
$P_D = \frac{150^oC - 25^oC}{360^oC/W}$	$P_D = \frac{150^oC - 60^oC}{360^oC/W}$
$P_D = 347\ mW$	$P_D = 250\ mW$

SC-70 (6-PIN)	
Room Ambient 25 °C	Elevated Ambient 60 °C
$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$	$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$
$P_D = \frac{150^oC - 25^oC}{180^oC/W}$	$P_D = \frac{150^oC - 60^oC}{180^oC/W}$
$P_D = 694\ mW$	$P_D = 500\ mW$

NOTE: Although they are intended for low-power applications, devices in the 6-pin SC-70 will handle power dissipation in excess of 0.5 W.

Testing

To aid comparison further, Figures 3 and 4 illustrate single-channel SC-70 thermal performance on two different board sizes and two different pad patterns. The results display the thermal performance out to steady state and produce a graphic account of the thermal performance variation between the two packages. The measured steady state values of $R\theta_{JA}$ for the single 3-pin and 6-pin SC-70 are as follows:

LITTLE FOOT SC-70		
	3-Pin	6-Pin
1) Minimum recommended pad pattern (see Figure 4) on the EVB.	410.31°C/W	329.7°C/W
2) Industry standard 1” square PCB with maximum copper both sides.	360°C/W	211.8°C/W

The results show that designers can reduce thermal resistance $R\theta_{JA}$ on the order of 20% simply by using the 6-pin device rather than the 3-pin device. In this example, a 80°C/W reduction was achieved without an increase in board area. If increasing board size is an option, a further 118°C/W reduction could be obtained by utilizing a 1-inch square PCB area.

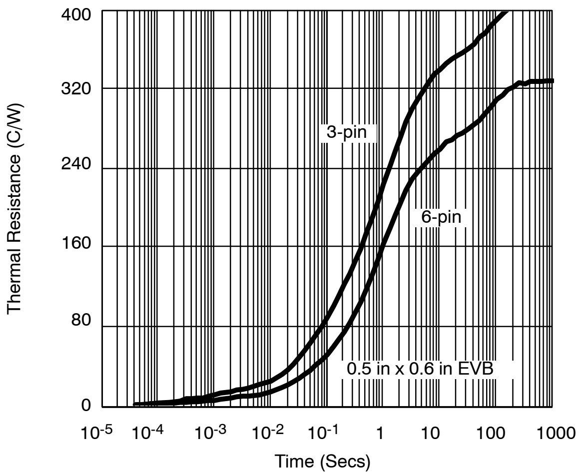


FIGURE 3. Comparison of SC70-3 and SC70-6 on EVB

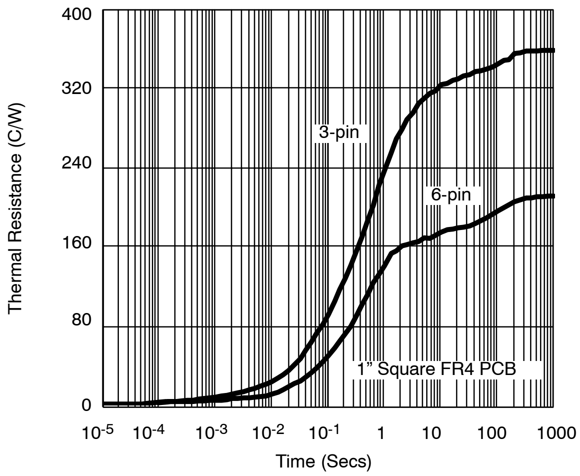
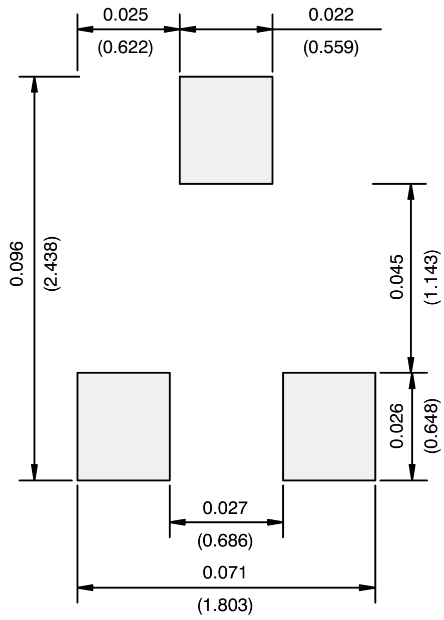


FIGURE 4. Comparison of SC70-3 and SC70-6 on 1” Square FR4 PCB

RECOMMENDED MINIMUM PADS FOR SC-70: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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