Excellent Integrated System Limited

Stocking Distributor

Click to view price, real time Inventory, Delivery & Lifecycle Information:

Texas Instruments
TPD2E2U06DRLR

For any questions, you can email us directly:
sales@integrated-circuit.com

TPD2E2U06 Dual-Channel High-Speed ESD Protection Device

1 Features

- IEC 61000-4-2 Level 4
  - ±25 kV (Contact Discharge)
  - ±30 kV (Air-gap Discharge)
- IEC 61000-4-5 Surge Protection
  - 5.5 A Peak Pulse Current (8/20 µs Pulse)
- IO Capacitance 1.5 pF (Typ)
- DC Breakdown Voltage 6.5 V (Min)
- Ultra-Low Leakage Current 10 nA (Max)
- Low ESD Clamping Voltage
- Industrial Temperature Range: –40°C to +125°C
- Small Easy-to-Route DRL Package

2 Applications

- End Equipment
  - Set Top Box
  - Notebook
  - Server
  - Electronic Point of Sale (EPOS)
- Interfaces
  - USB 2.0
  - Ethernet
  - MIPI Bus
  - LVDS
  - I2C

3 Description

The TPD2E2U06 is a dual-channel low capacitance TVS diode ESD protection device. The device offers ±25-kV contact and ±30-kV air-gap ESD protection in accordance with the IEC 61000-4-2 standard. The 1.5-pF line capacitance of the TPD2E2U06 makes the device suitable for a wide range of applications. Typical application interfaces are USB 2.0, LVDS, and I²C™.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD2E2U06	SOT (5)	1.60 mm × 1.20 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic

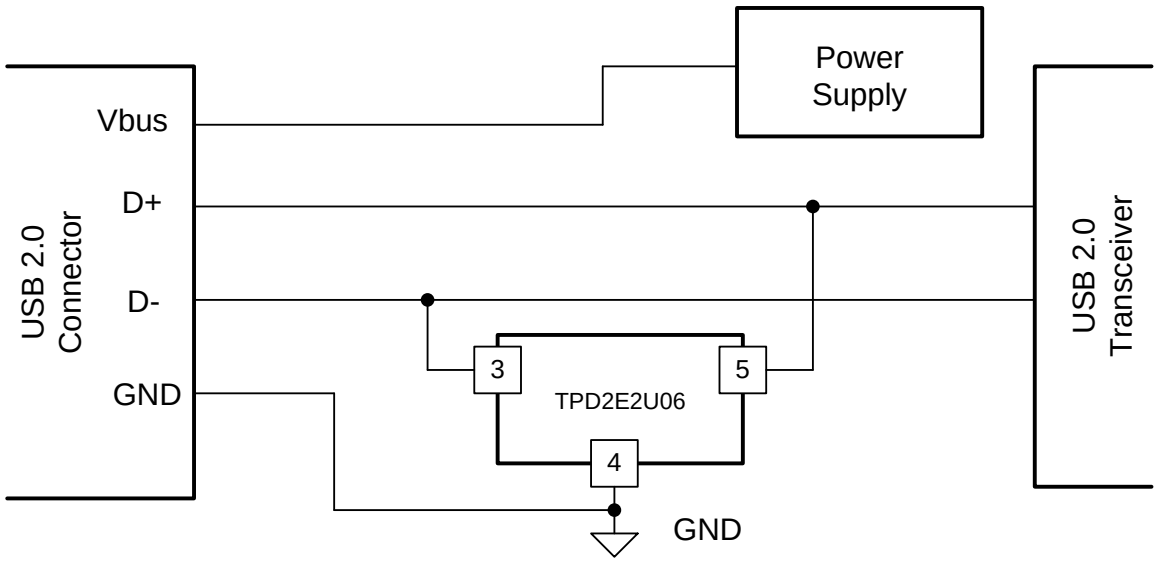


Table of Contents

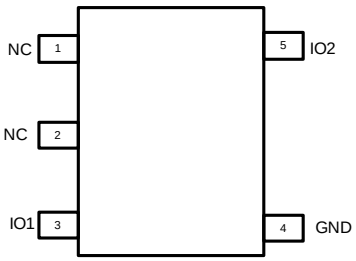
5 Revision History

Changes from Revision A (June 2013) to Revision B **Page**

- Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. ... 1

6 Pin Configuration and Functions

DRL
1.65 mm × 1.2 mm × 0.6 mm
(0.5-mm PITCH)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IO1	3	I/O	The IO1 and IO2 pins are an ESD protected channel. Connect these pins to the data line as close to the connector as possible.
IO2	5	I/O	
NC	1, 2	-	This pin is not connected and is left floating, grounded, or connected to VCC.
GND	4	G	The GND (ground) pin is connected to ground.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
I_{PP}	Peak pulse current (tp = 8/20 µs)		5.5 (1)	A
P_{PP}	Peak pulse power (tp = 8/20 µs)		85 (1)	W
	Operating temperature	–40	125	°C
	Storage temperature	–65	155	°C

(1) Measured at 25°C.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1500	
		EC 61000-4-2 contact	±25000	
		EC 61000-4-2 air-gap	±30000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IO}	Input Pin Voltage	0		5.5	V
T_A	Operating Free Air Temperature	-40		125	°C

7.4 Thermal Information

THERMAL METRIC[1]		TPD2E2U06 DRL 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	286.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	130.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	104.8	
ψ_{JT}	Junction-to-top characterization parameter	25.6	
ψ_{JB}	Junction-to-board characterization parameter	104.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} < 10 µA			5.5	V
V_{CLAMP}	IO to GND	I_{PP} = 1 A, TLP[1]		9.7		V
		I_{PP} = 5 A, TLP[1]		12.4		
V_{CLAMP}	GND to IO	I_{PP} = 1 A, TLP[1]		1.9		V
		I_{PP} = 5 A, TLP[1]		4		
R_{DYN}	Dynamic resistance	IO to GND[2]		0.5		Ω
R_{DYN}	Dynamic resistance	GND to IO[2]		0.25		Ω
CL	Line capacitance	f = 1 MHz, V_{BIAS} = 2.5 V[3]		1.5	1.9	pF
C_{CROSS}	Channel-to-channel input capacitance	Pin 4 = 0 V, f = 1 MHz, V_{BIAS} = 2.5 V, between channel pins[3]		0.02	0.03	pF
$\Delta_{CIO-TO-GND}$	Variation of channel input capacitance	Pin 4 = 0 V, f = 1 MHz, V_{BIAS} = 2.5 V, channel_x pin to GND – channel_y pin to GND[3]		0.03	0.1	pF
V_{BR}	Break-down voltage	I_{IO} = 1 mA	6.5		8.5	V
I_{LEAK}	Leakage current	V_{IO} = 2.5 V		1	10	nA

(1) Transmission Line Pulse with 10-ns rise time, 100-ns width.
(2) Extraction of R_{DYN} Using least squares fit of TLP characteristics between I = 20 A and I = 30 A.
(3) Measured at 25°C.

7.6 Typical Characteristics

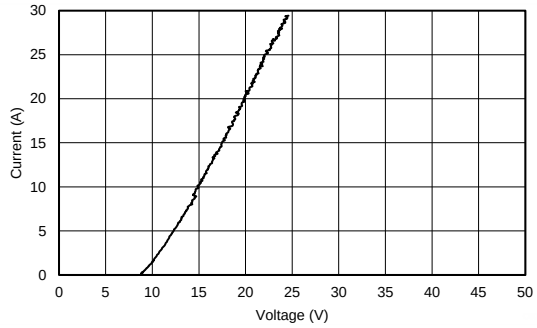


Figure 1. TLP, Data to GND

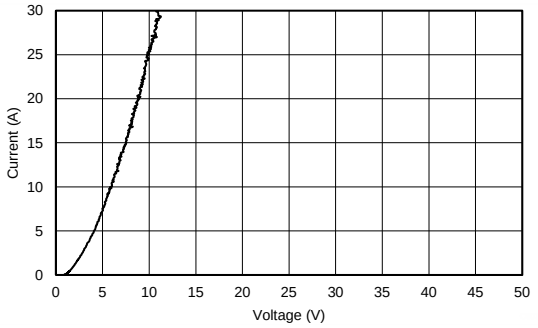


Figure 2. TLP, GND to Data

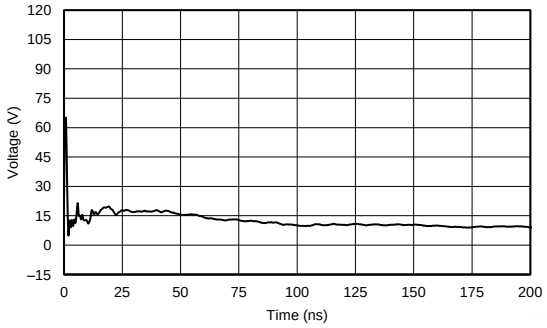


Figure 3. IEC 61000-4-2 Clamping Voltage, +8 kV Contact

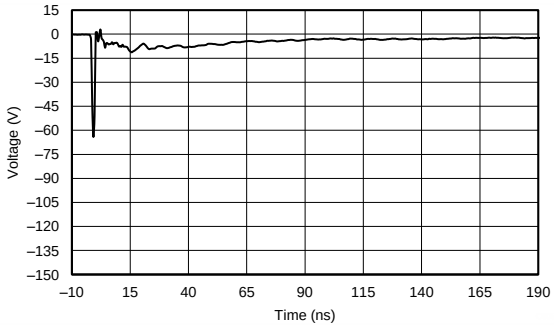
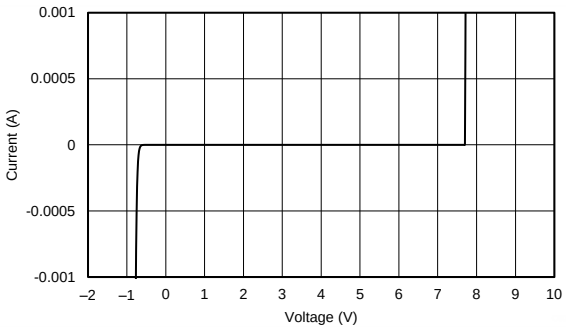
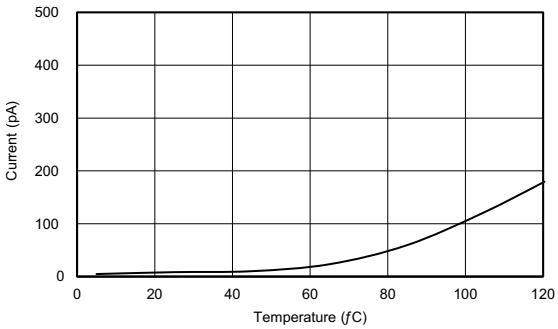


Figure 4. IEC 61000-4-2 Clamping Voltage, –8 kV Contact



T_A = 25°C

Figure 5. IV Curve



V_{IN} 2.5 V

Figure 6. I_{LEAK} vs Temperature

Typical Characteristics (continued)

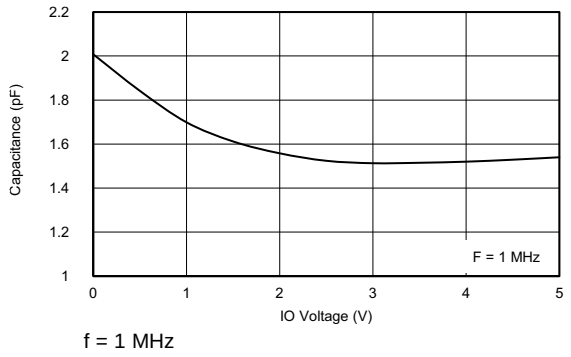


Figure 7. Capacitance Across V_{BIAS}

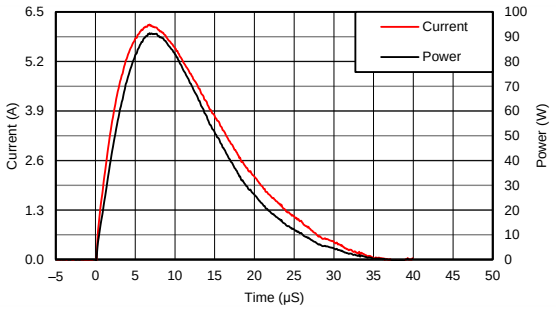


Figure 8. Surge Curve (tp = 8/20 µs) IO to GND

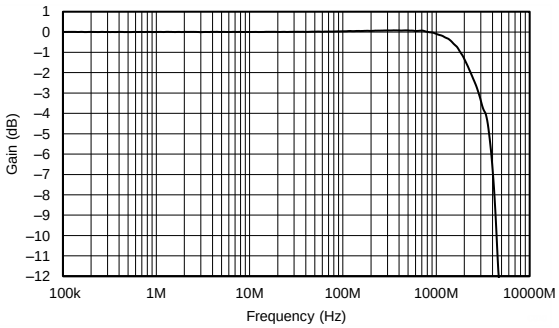


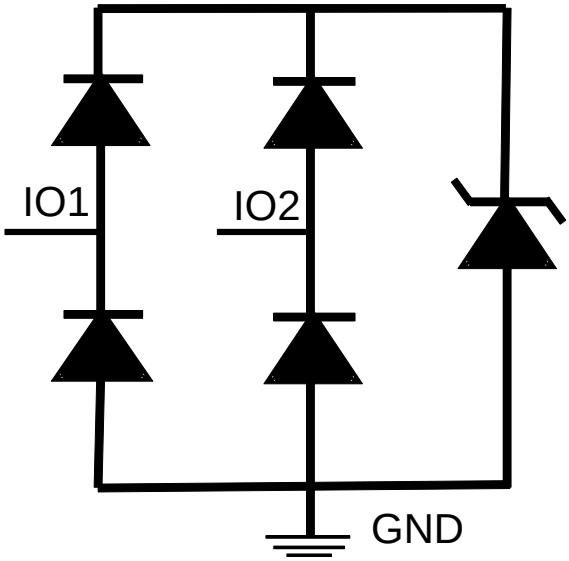
Figure 9. Insertion Loss

8 Detailed Description

8.1 Overview

The TPD2E2U06 is a dual-channel low capacitance TVS diode ESD protection device. The device offers ±25-kV contact and ±30-kV air-gap ESD protection in accordance with the IEC 61000-4-2 standard. The 1.5-pF line capacitance of the TPD2E2U06 makes the device suitable for a wide range of applications. Typical application interfaces are USB 2.0, LVDS, and I2C.

8.2 Functional Block Diagram



8.3 Feature Description

The TPD2E2U06 is a dual-channel low capacitance TVS diode ESD protection device. The device offers ±25-kV contact and ±30-kV air-gap ESD protection in accordance with the IEC 61000-4-2 standard. The 1.5-pF line capacitance of the TPD2E2U06 makes the device suitable for a wide range of applications. Typical application interfaces are USB 2.0, LVDS, and I2C.

8.3.1 IEC 61000-4-2 Level 4

The I/O pins can withstand ESD events up to ±25-kV contact and ±30-kV air. An ESD/surge clamp diverts the current to ground.

8.3.2 IO Capacitance

The capacitance between each I/O pin to ground is 1.5 pF. These capacitances support data rates in excess of 1.5 Gbps.

8.3.3 DC Breakdown Voltage

The DC breakdown voltage of each I/O pin is a minimum of 6.5 V. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of 5.5 V.

8.3.4 Ultra-Low Leakage Current

The I/O pins feature an ultra-low leakage current of 10 nA (Max) with a bias of 2.5 V.

8.3.5 Low ESD Clamping Voltage

The I/O pins feature an ESD clamp that is capable of clamping the voltage to 9.7 V (I_{PP} = 1 A).

Feature Description (continued)

8.3.6 Industrial Temperature Range

This device is designed to operate from –40°C to 125°C.

8.3.7 Small Easy-to-Route Package

The layout of this device makes it simple and easy to add protection to an existing layout. The packages offers flow-through routing, requiring minimal modification to an existing layout.

8.4 Device Functional Modes

TPD2E2U06 is a passive integrated circuit that triggers when voltages are above V_{BR} or below the lower diodes V_f (–0.6 V). During ESD events, voltages as high as ±30 kV (air) can be directed to ground via the internal diode network. Once the voltages on the protected line fall below the trigger levels of TPD2E2U06 (usually within 10's of nano-seconds) the device reverts to passive.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

TPD2E2U06 is a diode type TVS which is typically used to provide a path to ground for dissipating ESD events on hi-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

9.2 Typical Application

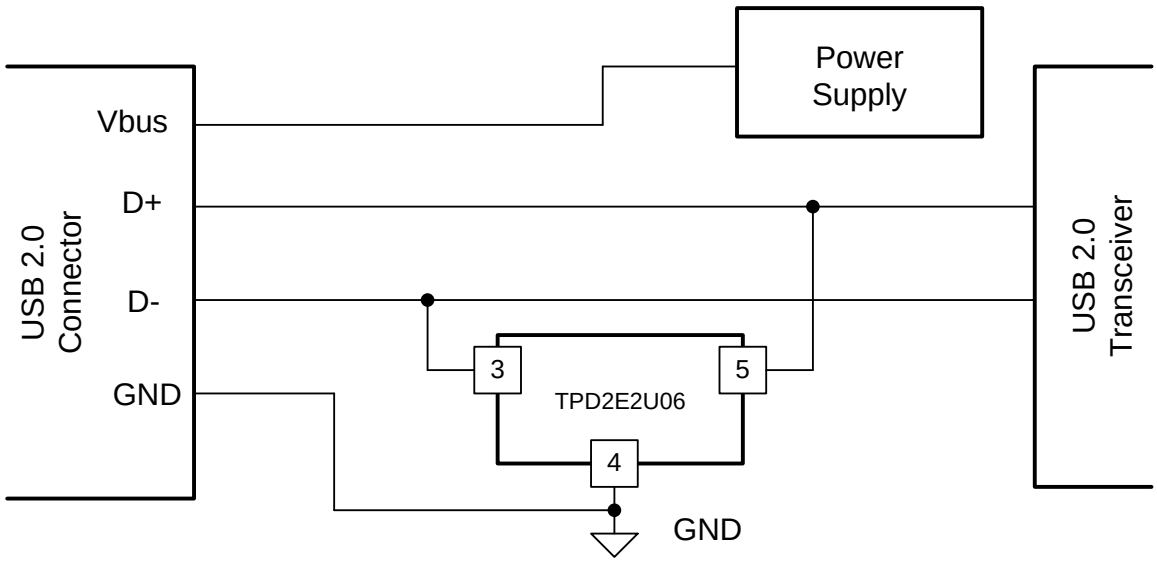


Figure 10. Typical USB Application Diagram

9.2.1 Design Requirements

For this design example, one TPD2E2U06 device will be used in a USB 2.0 application. This will provide complete port protection.

Given the USB 2.0 application, the following parameters are known.

DESIGN PARAMETER	VALUE
Signal range on Pins 3 or 5	0 V to 3.3 V
Operating Frequency	240 MHz

9.2.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon; the designer needs to know the following:

- Signal range of all the protected lines
- Operating frequency

9.2.2.1 Signal Range

The TPD2E2U06 has 2 identical protection channels for signal lines. The symmetry of the device provides flexibility when selecting which of the 2 I/O channels will protect which signal lines. Any I/O will support a signal range of 0 to 5.5 V.

9.2.2.2 Operating Frequency

The TPD2E2U06 has a capacitance of 1.5 pF (Typ), supporting USB 2.0 data rates.

9.2.3 Application Curves

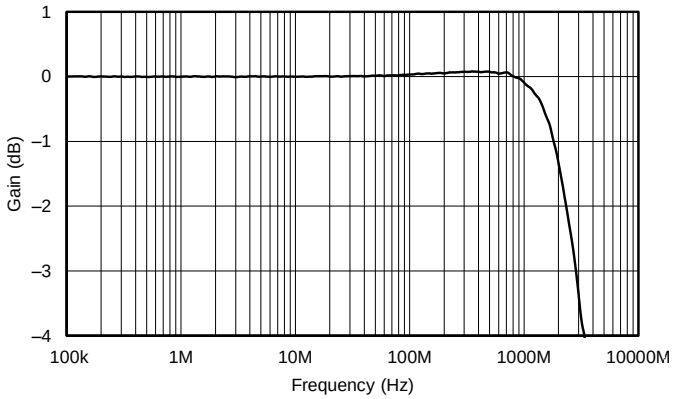


Figure 11. Insertion Loss Graph

10 Power Supply Recommendations

This device is a passive ESD protection device and there is no need to power it. Care should be taken to make sure that the maximum voltage specifications for each line are not violated.

11 Layout

11.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

11.2 Layout Example

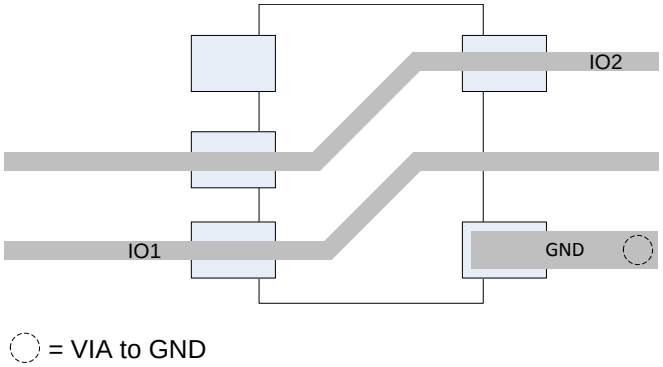


Figure 12. Routing with DRL Package

12 Device and Documentation Support

12.1 Trademarks

I^2C is a trademark of NXP Semiconductors.
All other trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD2E2U06DRLR	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	DT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPD2E2U06 :

- Automotive: TPD2E2U06-Q1

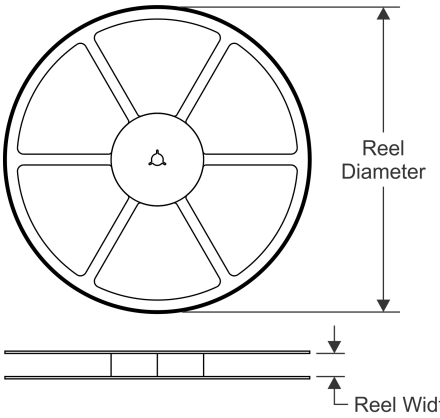
NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

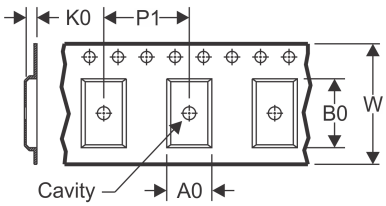
PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

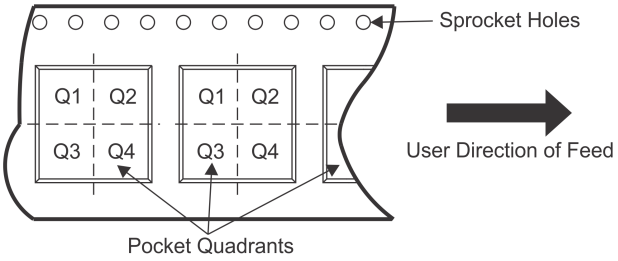


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

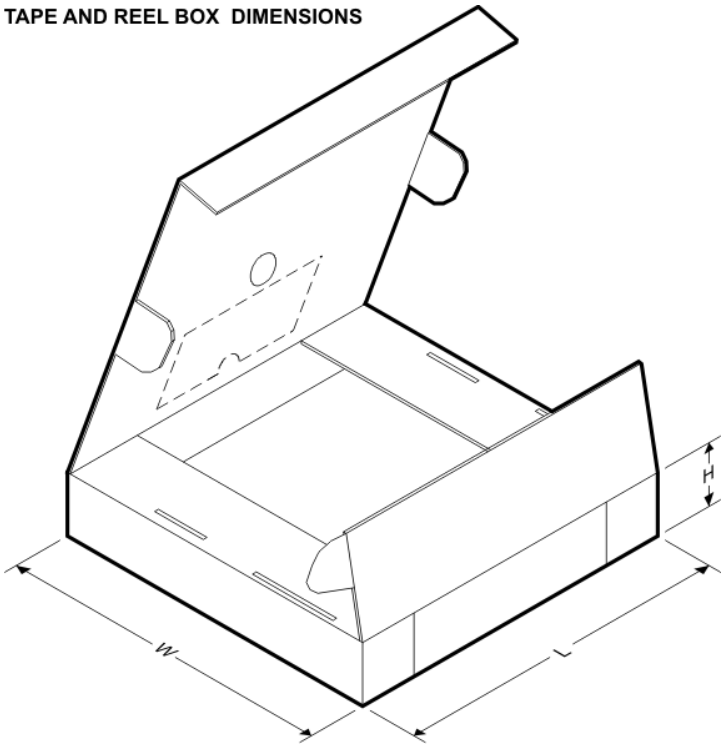


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD2E2U06DRLR	SOT	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3

PACKAGE MATERIALS INFORMATION

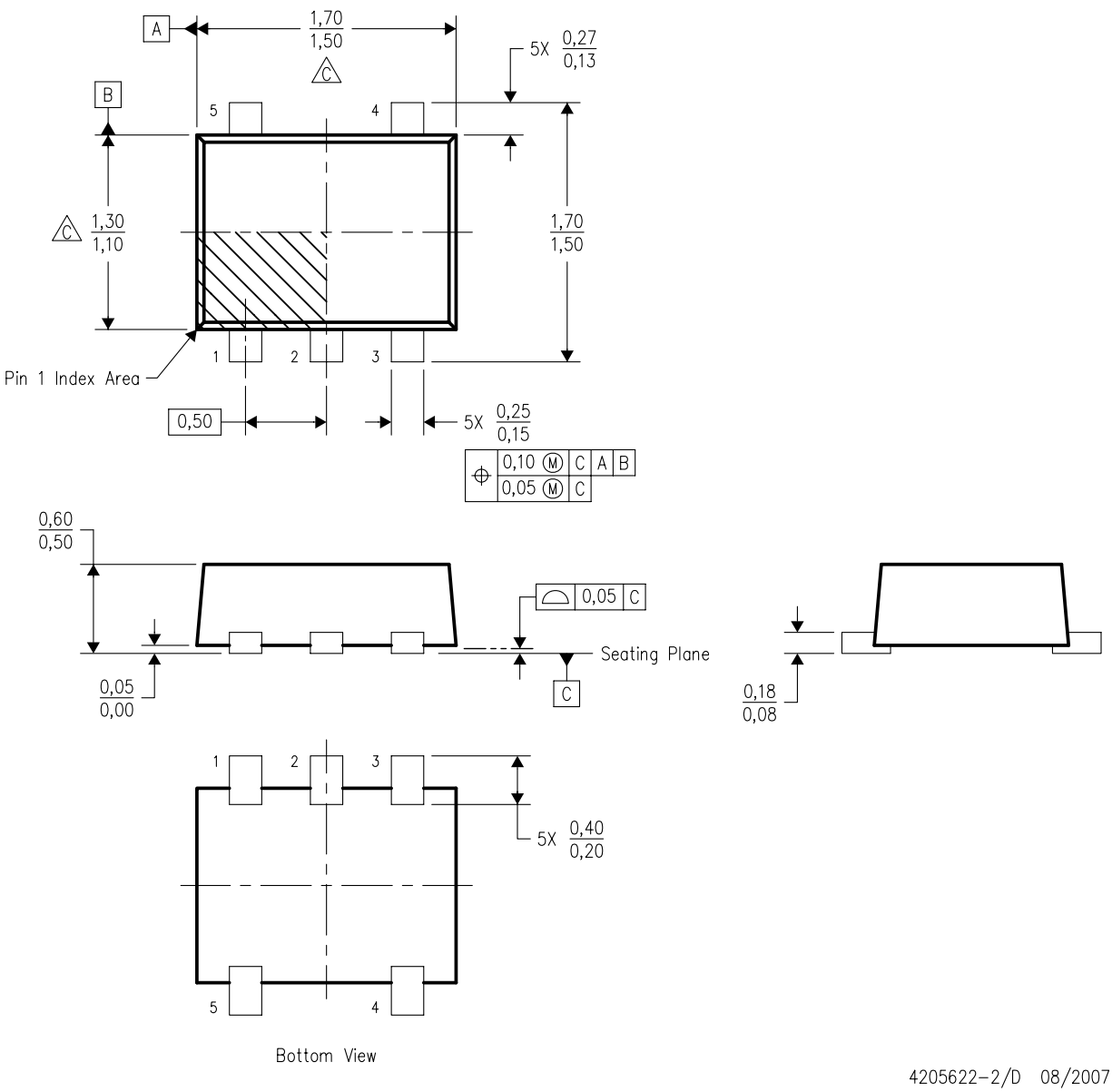
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD2E2U06DRLR	SOT	DRL	5	4000	202.0	201.0	28.0

DRL (R–PDSO–N5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
D. JEDEC package registration is pending.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265