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STK554U362A-E

Thick-Film Hybrid IC

Inverter Power H-IC for 3-phase Motor Drive

Overview

This “Inverter Power H-IC” is highly integrated device containing all High Voltage (HV) control from HV-DC to 3-phase outputs in a single small SIP module. Output stage uses IGBT/FRD technology and implements Under Voltage Protection (UVP) and Over Current Protection (OCP) with a Fault Detection output flag. Internal Boost diodes are provided for high side gate boost drive.

Function

- Single control power supply due to Internal bootstrap circuit for high side pre-driver circuit
- All control inputs and status outputs are at low voltage levels directly compatible with microcontrollers.
- A single power supply drive is enabled through the use of bootstrap circuits for upper power supplies
- Built-in dead-time for shoot-thru protection
- Having open emitter output for low side IGBTs; individual shunt resistor per phase for OCP
- Externally accessible embedded thermistor for substrate temperature measurement
- Shutdown function ‘ITRIP’ to disable all operations of the 6 phase output stage by external input

Certification

- UL1557 (File number: E339285).

Specifications

Absolute Maximum Ratings at T_c = 25°C

| Parameter | Symbol | Remarks | Ratings | Unit |
|----------------------------|------------------|---|-------------|------|
| Supply voltage | VCC | V+ to U-, V-, W-, surge<500V *1 | 450 | V |
| Collector-emitter voltage | VCE | V+ to U, V, W or U, V, W, to U-, V-, W- | 600 | V |
| Output current | I _o | V+,U-,V-,W-,U,V,W terminal current | ±10 | A |
| | | V+,U-,V-,W-,U,V,W terminal current, T _c =100°C | ±7 | A |
| Output peak current | I _{op} | V+,U-,V-,W-,U,V,W terminal current, P.W.=1ms | ±20 | A |
| Pre-driver voltage | VD1,2,3,4 | VB1 to U, VB2 to V, VB3 to W, VDD to VSS *2 | 20 | V |
| Input signal voltage | VIN | HIN1, 2, 3, LIN1, 2, 3 | -0.3 to VDD | V |
| FLTEN terminal voltage | VFLTEN | FLTEN terminal | -0.3 to VDD | V |
| Maximum power dissipation | P _d | IGBT per 1 channel | 30 | W |
| Junction temperature | T _j | IGBT, FRD, Pre-Driver IC | 150 | °C |
| Storage temperature | T _{stg} | | -40 to +125 | °C |
| Operating case temperature | T _c | H-IC case | -40 to +100 | °C |
| Tightening torque | | A screw part *3 | 0.9 | Nm |
| Withstand voltage | V _{is} | 50Hz sine wave AC 1 minute *4 | 2000 | VRMS |

Reference voltage is “VSS” terminal voltage unless otherwise specified.

*1: Surge voltage developed by the switching operation due to the wiring inductance between + and U-(V-, W-) terminal.

*2: VD1=VB1 to U, VD2=VB2 to V, VD3=VB3 to W, VD4=VDD to VSS terminal voltage.

*3: Flatness of the heat-sink should be less than -50μm to +100μm.

*4: Test conditions : AC2500V, 1 second

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ORDERING INFORMATION

See detailed ordering and shipping information on page 15 of this data sheet.

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Electrical Characteristics at Tc = 25°C, VD1, VD2, VD3, VD4 = 15V

| Parameter | Symbol | Conditions | Test circuit | MIN | TYP | MAX | Unit |
|--|------------------|---------------------------------------|--------------|------|------|------|-------|
| Power output section | | | | | | | |
| Collector-emitter cut-off current | ICE | VCE = 600V | Fig.1 | - | - | 100 | μA |
| Bootstrap diode reverse current | IR(BD) | VR(BD) = 600V | | - | - | 100 | μA |
| Collector to emitter saturation voltage | VCE(SAT) | Ic = 10A, Tj=25°C | Fig.2 | - | 1.6 | 2.2 | V |
| | | Ic = 5A, Tj=100°C | | - | 1.35 | - | |
| Diode forward voltage | VF | IF = -10A, Tj=25°C | Fig.3 | - | 1.6 | 2.1 | V |
| | | IF = -5A, Tj=100°C | | - | 1.3 | - | |
| Junction to case thermal resistance | θj-c(T) | IGBT | - | - | - | 4 | °C /W |
| | θj-c(D) | FWD | | - | - | 5 | |
| Control (Pre-driver) section | | | | | | | |
| Pre-driver power dissipation | ID | VD1,2,3 = 15V | Fig.4 | - | 0.08 | 0.4 | mA |
| | | VD4 = 15V | | - | 1.6 | 4 | |
| High level Input voltage | Vin H | HIN1,HIN2,HIN3, | - | 2.5 | - | - | V |
| Low level Input voltage | Vin L | LIN1,LIN2,LIN3 to VSS | - | - | - | 0.8 | V |
| Logic 1 input leakage current | IIN+ | VIN=+3.3V | - | - | 100 | 143 | μA |
| Logic 0 input leakage current | IIN- | VIN=0V | - | - | - | 2 | μA |
| FLTEN terminal sink current | IoSD | FAULT:ON / VFLTEN=0.1V | - | - | 2 | - | mA |
| FLTEN clearance delay time | FLTCLR | From time fault condition clear | - | 1.3 | 1.65 | 2 | ms |
| FLTEN Threshold | VEN+ | VEN rising | - | - | - | 2.5 | V |
| | VEN- | VEN falling | - | 0.8 | - | - | V |
| ITRIP threshold voltage | VITRIP | ITRIP(16) to VSS(29) | - | 0.44 | 0.49 | 0.54 | V |
| ITRIP to shutdown propagation delay | tITRIP | | - | 340 | 550 | 800 | ns |
| ITRIP blanking time | tITRIPBL | | - | 250 | 350 | - | ns |
| VCC and VBS supply undervoltage protection reset | VCCUV+ VBSUV+ | | - | 10.5 | 11.1 | 11.7 | V |
| VCC and VBS supply undervoltage protection set | VCCUV- VBSUV- | | - | 10.3 | 10.9 | 11.5 | V |
| VCC and VBS supply undervoltage hysteresis | VCCUVH VBSUVH | | - | 0.14 | 0.2 | - | V |
| Thermistor for substrate temperature Monitor | Rt | Resistance between TH(27) and VSS(29) | - | 42.3 | 47 | 51.7 | kΩ |

Reference voltage is "VSS" terminal voltage unless otherwise specified.

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| Parameter | Symbol | Conditions | Test circuit | MIN | TYP | MAX | Unit |
|------------------------------------|------------------|---|--------------|--------------|------|-----|------|
| Switching Character | | | | | | | |
| Switching time | t ON | I _o = 10A | Fig.5 | - | 0.4 | - | μs |
| | t OFF | Inductive load | | - | 0.65 | - | |
| Turn-on switching loss | E _{on} | I _o =5A, V ⁺ =300V, | Fig.5 | - | 130 | - | μJ |
| Turn-off switching loss | E _{off} | V _{DD} =15V, L=650uH | | - | 122 | - | μJ |
| Total switching loss | E _{tot} | T _c =25°C | | - | 252 | - | μJ |
| Turn-on switching loss | E _{on} | I _o =5A, V ⁺ =300V, | Fig.5 | - | 156 | - | μJ |
| Turn-off switching loss | E _{off} | V _{DD} =15V, L=650uH | | - | 154 | - | μJ |
| Total switching loss | E _{tot} | T _c =100°C | | - | 310 | - | μJ |
| Diode reverse recovery energy | E _{rec} | I _o =5A, V ⁺ =400V, V _{DD} =15V, | - | - | 6.9 | - | μJ |
| Diode reverse recovery time | T _{rr} | L=650uH, T _c =100°C | - | - | 57 | - | ns |
| Reverse bias safe operating area | RBSOA | I _o = 20A, VCE = 450V | - | Full square- | | | - |
| Short circuit safe operating area | SCSOA | VCE = 400V, T _c =100°C | - | 4 | - | - | μs |
| Allowable offset voltage slew rate | dv/dt | Between U(V,W) to U-(V-,W-) | - | -50 | - | 50 | V/ns |

Reference voltage is "VSS" terminal voltage unless otherwise specified.

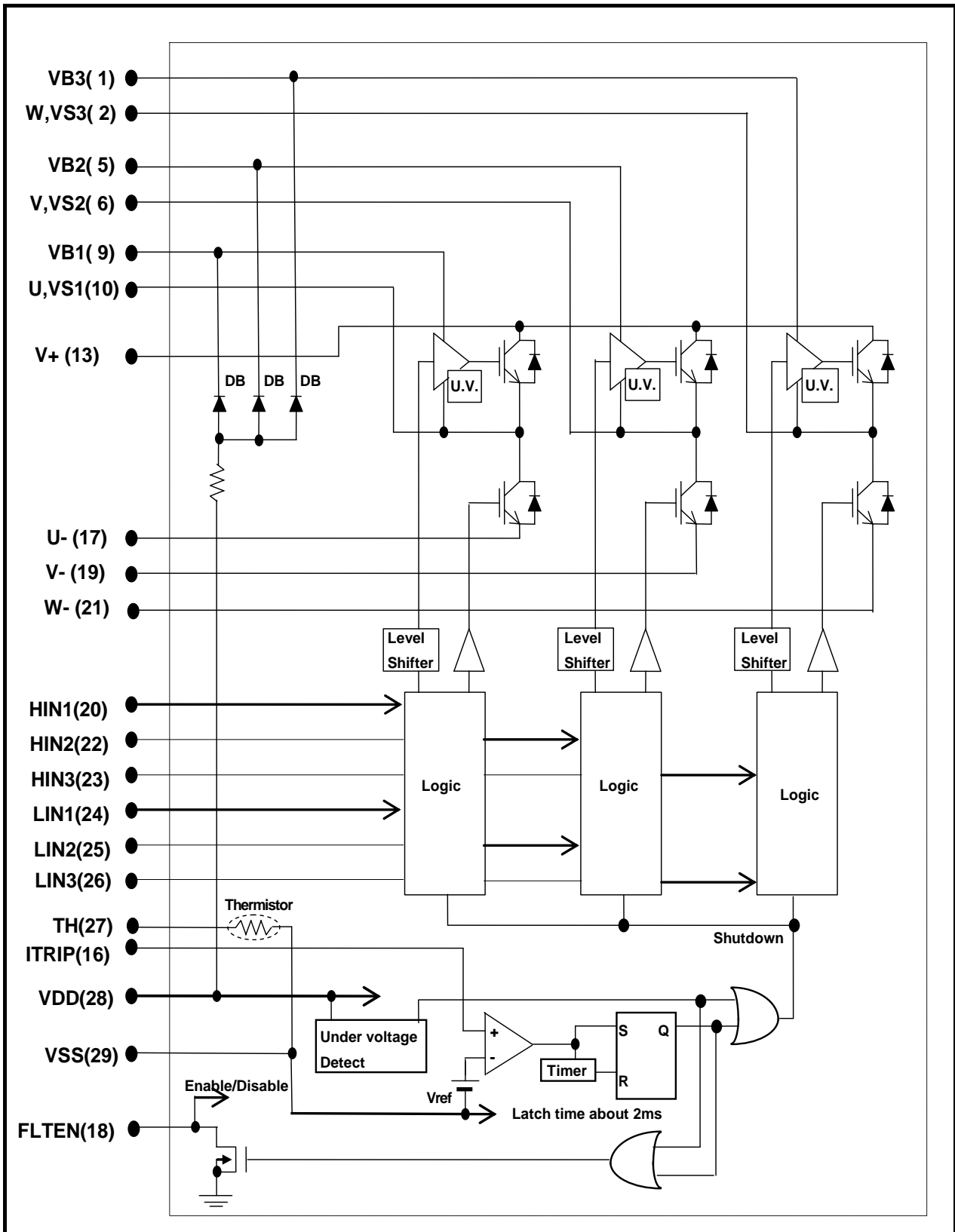
Notes

- The pre-drive power supply low voltage protection has approximately 200mV of hysteresis and operates as follows.
 - Upper side : The gate is turned off and will return to regular operation when recovering to the normal voltage, but the latch will continue till the input signal will turn 'low'.
 - Lower side : The gate is turned off and will automatically reset when recovering to normal voltage. It does not depend on input signal voltage.
- When assembling the H-IC on the heat sink the tightening torque range is 0.6Nm to 0.9Nm.
- The pre-drive low voltage protection protects the device when the pre-drive supply voltage falls due to an operating malfunction.
- When use the over-current protection with external shunt resistor, please set the current protection level to be equal to or less than the rating of output peak current (I_{op}).

Module Pin-Out Description

| Pin | Name | Description |
|-----|--------|---|
| 1 | VB3 | High Side Floating Supply Voltage 3 |
| 2 | W, VS3 | Output 3 - High Side Floating Supply Offset Voltage |
| 3 | - | Without pin |
| 4 | - | Without pin |
| 5 | VB2 | High Side Floating Supply voltage 2 |
| 6 | V,VS2 | Output 2 - High Side Floating Supply Offset Voltage |
| 7 | - | Without pin |
| 8 | - | Without pin |
| 9 | VB1 | High Side Floating Supply voltage 1 |
| 10 | U,VS1 | Output 1 - High Side Floating Supply Offset Voltage |
| 11 | - | Without pin |
| 12 | - | Without pin |
| 13 | V+ | Positive Bus Input Voltage |
| 14 | - | Without pin |
| 15 | - | Without pin |
| 16 | ITRIP | Current protection pin |
| 17 | U- | Low Side Emitter Connection - Phase U |
| 18 | FLTEN | Enable input / Fault output |
| 19 | V- | Low Side Emitter Connection - Phase V |
| 20 | HIN1 | Logic Input High Side Gate Driver - Phase U |
| 21 | W- | Low Side Emitter Connection - Phase W |
| 22 | HIN2 | Logic Input High Side Gate Driver - Phase V |
| 23 | HIN3 | Logic Input High Side Gate Driver - Phase W |
| 24 | LIN1 | Logic Input Low Side Gate Driver - Phase U |
| 25 | LIN2 | Logic Input Low Side Gate Driver - Phase V |
| 26 | LIN3 | Logic Input Low Side Gate Driver - Phase W |
| 27 | TH | Thermistor output |
| 28 | VDD | +15V Main Supply |
| 29 | VSS | Negative Main Supply |

Equivalent Block Diagram



Test Circuit

(The tested phase : U+ shows the upper side of the U phase and U- shows the lower side of the U phase.)

■ ICE / IR(BD)

| | | | | | | |
|---|----|----|----|----|----|----|
| | U+ | V+ | W+ | U- | V- | W- |
| M | 13 | 13 | 13 | 10 | 6 | 2 |
| N | 10 | 6 | 2 | 17 | 19 | 21 |

| | | | |
|---|-------|-------|-------|
| | U(BD) | V(BD) | W(BD) |
| M | 9 | 5 | 1 |
| N | 29 | 29 | 29 |

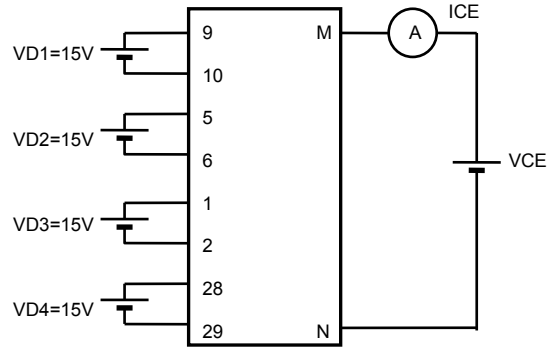


Fig.1

■ VCE(SAT) (Test by pulse)

| | | | | | | |
|---|----|----|----|----|----|----|
| | U+ | V+ | W+ | U- | V- | W- |
| M | 13 | 13 | 13 | 10 | 6 | 2 |
| N | 10 | 6 | 2 | 17 | 19 | 21 |
| m | 20 | 22 | 23 | 24 | 25 | 26 |

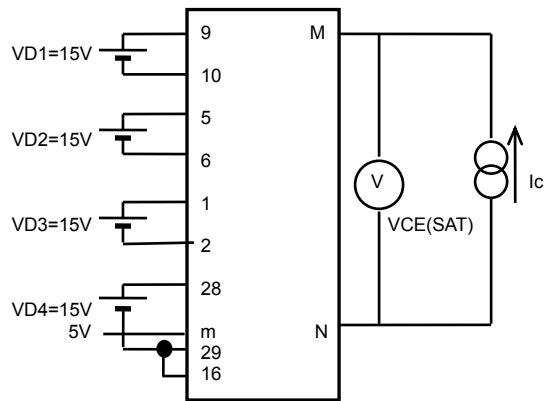


Fig.2

■ VF (Test by pulse)

| | | | | | | |
|---|----|----|----|----|----|----|
| | U+ | V+ | W+ | U- | V- | W- |
| M | 13 | 13 | 13 | 10 | 6 | 2 |
| N | 10 | 6 | 2 | 17 | 19 | 21 |

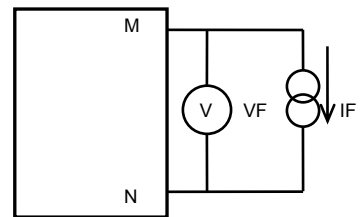


Fig.3

■ ID

| | | | | |
|---|-----|-----|-----|-----|
| | VD1 | VD2 | VD3 | VD4 |
| M | 9 | 5 | 1 | 28 |
| N | 10 | 6 | 2 | 29 |

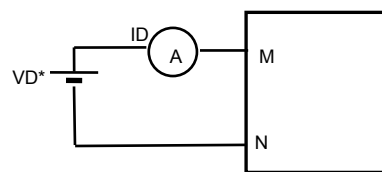


Fig.4

■ Switching time (The circuit is a representative example of the lower side U phase.)

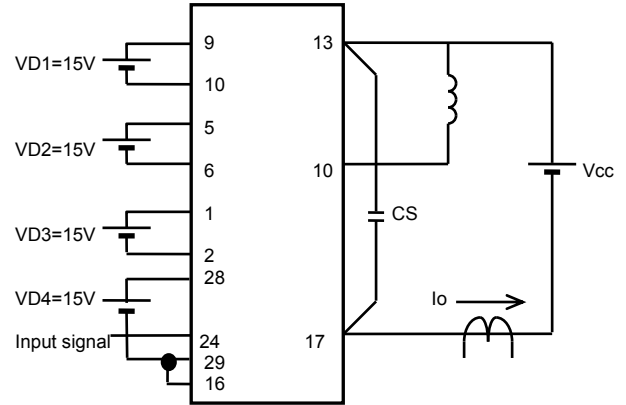
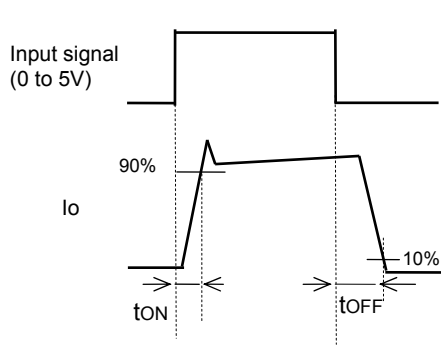


Fig.5

■ RB-SOA (The circuit is a representative example of the lower side U phase.)

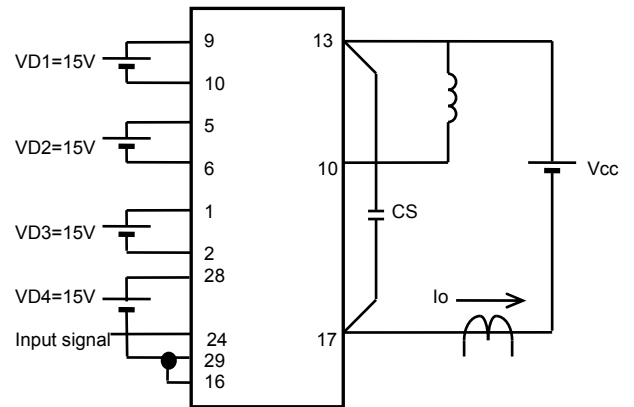
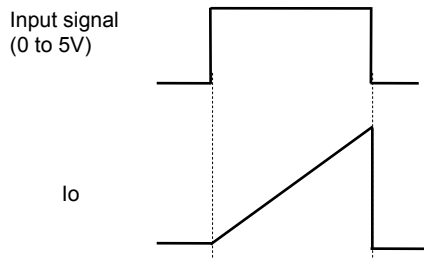


Fig.6

Input / Output Timing Chart

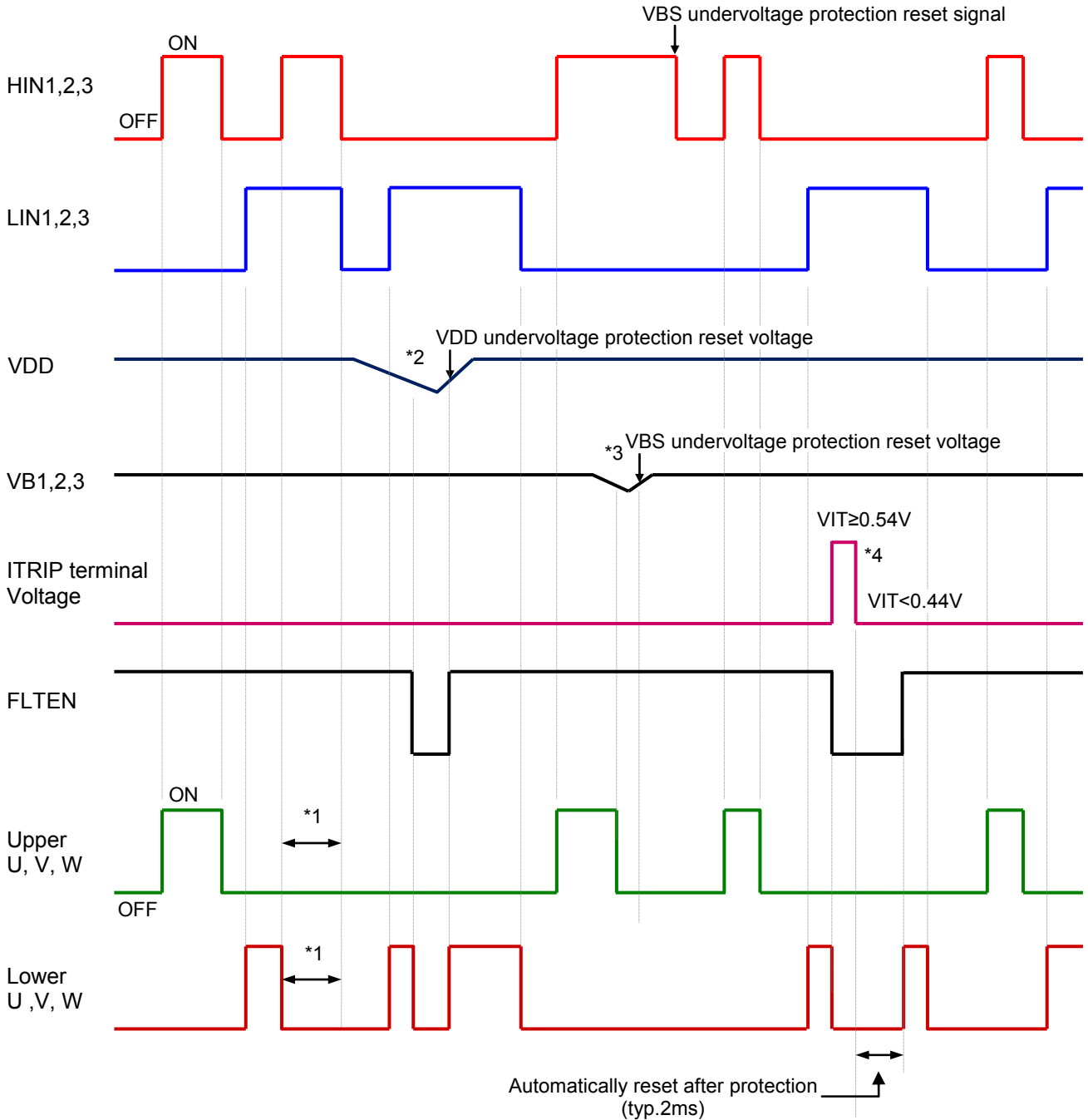


Fig. 7

Notes:

- *1 shows the prevention of shoot-thru via control logic, however, more dead time must be added to account for switching delay externally.
- *2 when VDD decreases all gate output signals will go low and cut off all 6 IGBT outputs. When VDD rises the operation will resume immediately.
- *3 when the upper side voltage at VB1, VB2 and VB3 drops only the corresponding upper side output is turned off. The outputs return to normal operation immediately after the upper side gate voltage rises.
- *4 when VITRIP exceeds threshold all IGBT's are turned off and normal operation resumes 2ms (typ) after over current condition is removed.

Logic level table

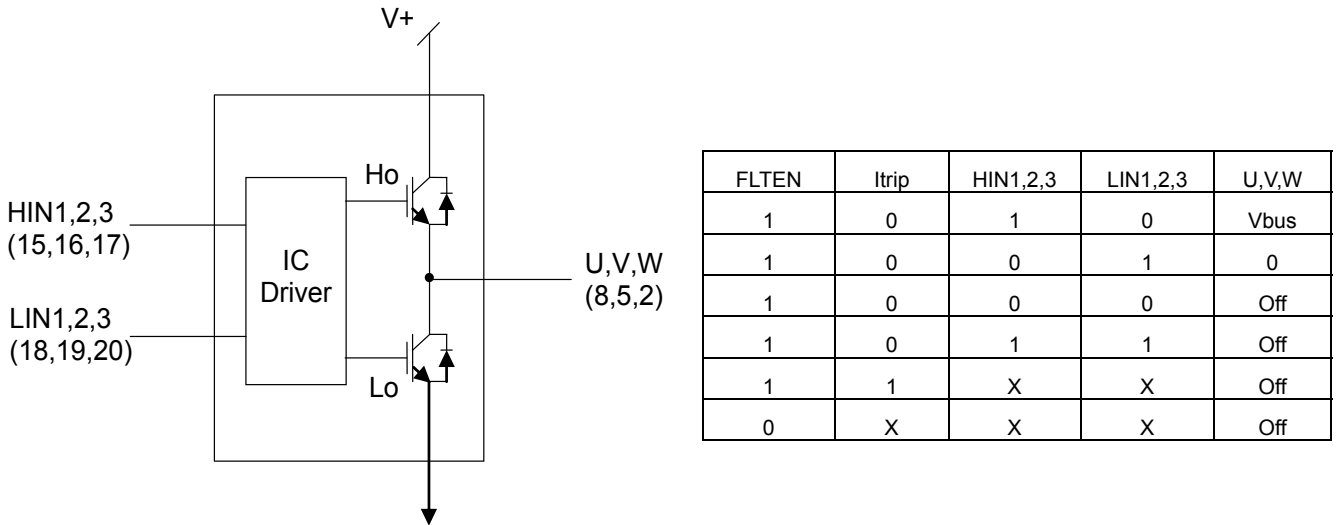


Fig. 8

Sample Application Circuit

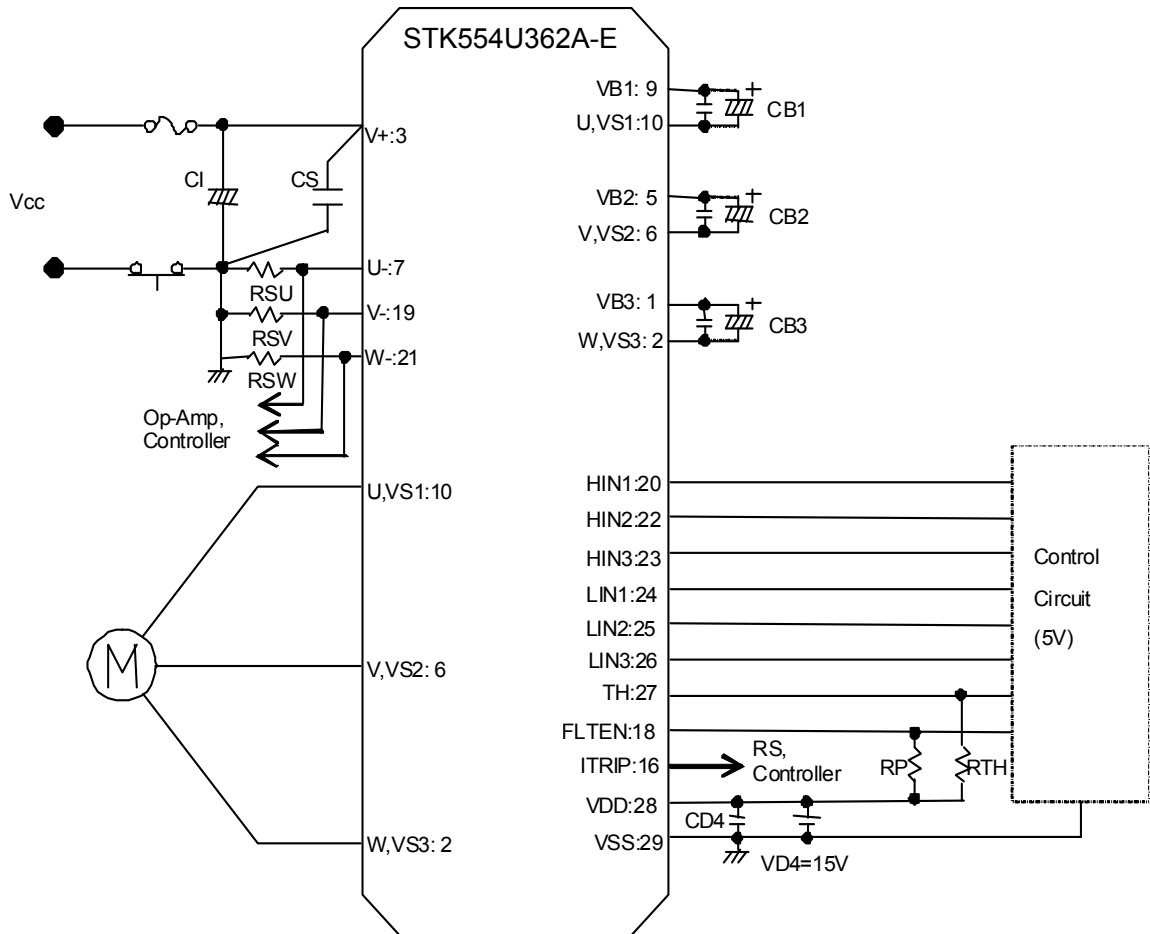


Fig.9

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Recommended Operating Condition at $T_c = 25^\circ\text{C}$

| Item | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|-----------------------------|----------|--------------------------------|------|------|------|---------------|
| Supply voltage | VCC | V+ to U-(V-,W-) | 0 | 280 | 450 | V |
| Pre-driver supply voltage | VD1,2,3 | VB1 to U,VB2 to V,VB3 to W | 12.5 | 15 | 17.5 | V |
| | VD4 | VDD to VSS *1 | 13.5 | 15 | 16.5 | |
| ON-state input voltage | VIN(ON) | HIN1,HIN2,HIN3, | 3.0 | - | 5.0 | V |
| OFF-state input voltage | VIN(OFF) | LIN1,LIN2,LIN3 | 0 | - | 0.3 | |
| PWM frequency | fPWM | | 1 | - | 20 | kHz |
| Dead time | DT | Turn-off to turn-on (external) | 0.5 | - | - | μs |
| Allowable input pulse width | PWIN | ON and OFF | 1 | - | - | μs |
| Tightening torque | | 'M3' type screw | 0.6 | - | 0.9 | Nm |

*1 Pre-drive power supply (VD4=15±1.5V) must have the capacity of $I_o=20\text{mA}$ (DC), 0.5A (Peak).

Usage Precaution

- This H-IC includes internal bootstrap diode and resistor. By adding a bootstrap capacitor "CB", a high side drive voltage is generated; each phase requires an individual bootstrap capacitor. The recommended value of CB is in the range of 1 to 47 μF , however, this value needs to be verified prior to production. If selecting the capacitance more than 47 μF ($\pm 20\%$), connect a resistor (about 20 Ω) in series between each 3-phase upper side power supply terminals (VB1,2,3) and each bootstrap capacitor.
When not using the bootstrap circuit, each upper side pre-drive power supply requires an external independent power supply.
- It is essential that wiring length between terminals in the snubber circuit be kept as short as possible to reduce the effect of surge voltages. Recommended value of "CS" is in the range of 0.1 to 10 μF .
- The "FLTEN" terminal (Pin 18) is I/O terminal; Fault output / Enable input. It is used to indicate an internal fault condition of the module and also can be used to disable the module operation.
- Inside the H-IC, a thermistor used as the temperature monitor for internal substrate is connected between VSS terminal and TH terminal, therefore, an external pull up resistor connected between the TH terminal and an external power supply should be used. The temperature monitor example application is as follows, please refer the Fig.10, and Fig.11 below.
- The pull-down resistor (:33k Ω (typ)) is connected with the inside of the signal input terminal, but please connect the pull-down resistor(about 2.2 to 3.3k Ω) outside to decrease the influence of the noise by wiring etc.
- As protection of H-IC to the unusual current by a short circuit etc., it recommends installing shunt resistors and an over-current protection circuit outside. Moreover, for safety, a fuse on Vcc line is recommended.
- Disconnection of terminals U, V, or W during normal motor operation will cause damage to H-IC, use caution with this connection.
- The "ITRIP" terminal (Pin 16) is the input terminal to shut down. When VITRIP exceeds threshold (0.44V to 0.54V) all IGBT's are turned off. And normal operation resumes 2ms (typ) after over current condition is removed. Therefore, please turn all the input signals off (Low) in case of detecting error at the "FLTEN" terminal.
- When input pulse width is less than 1 μs , an output may not react to the pulse. (Both ON signal and OFF signal)

- This data shows the example of the application circuit; and does not guarantee a design as the mass production set.

The characteristic of thermistor

| Parameter | Symbol | Condition | Min | Typ. | Max | Unit |
|---------------------|-----------|---------------------------|------|------|------|--------------------|
| Resistance | R_{25} | $T = 25^{\circ}\text{C}$ | 44.6 | 47.0 | 49.4 | k Ω |
| Resistance | R_{125} | $T = 125^{\circ}\text{C}$ | 1.28 | 1.41 | 1.53 | k Ω |
| B-Constant(25-50°C) | B | | 4010 | 4050 | 4091 | K |
| Temperature Range | | | -40 | | +125 | $^{\circ}\text{C}$ |

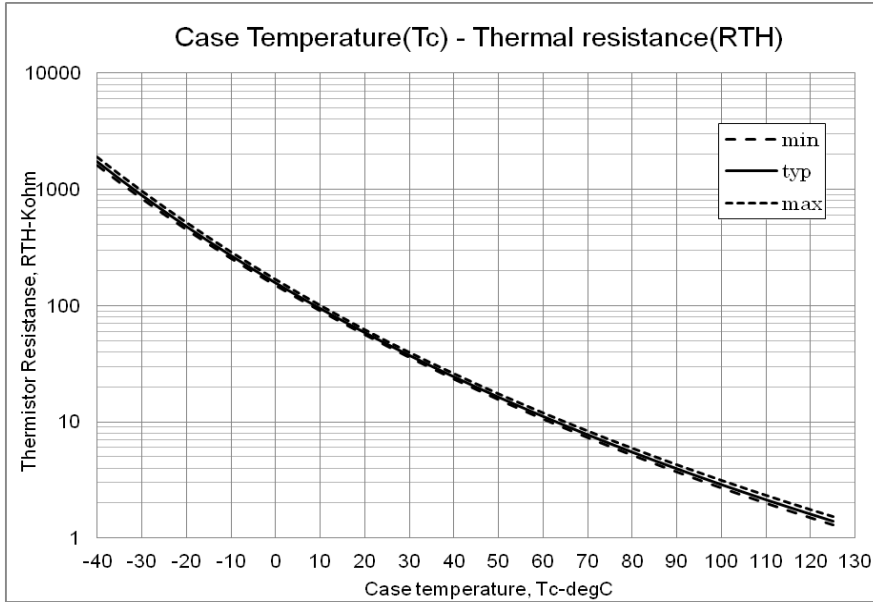


Fig.10 Variation of thermistor resistance with temperature

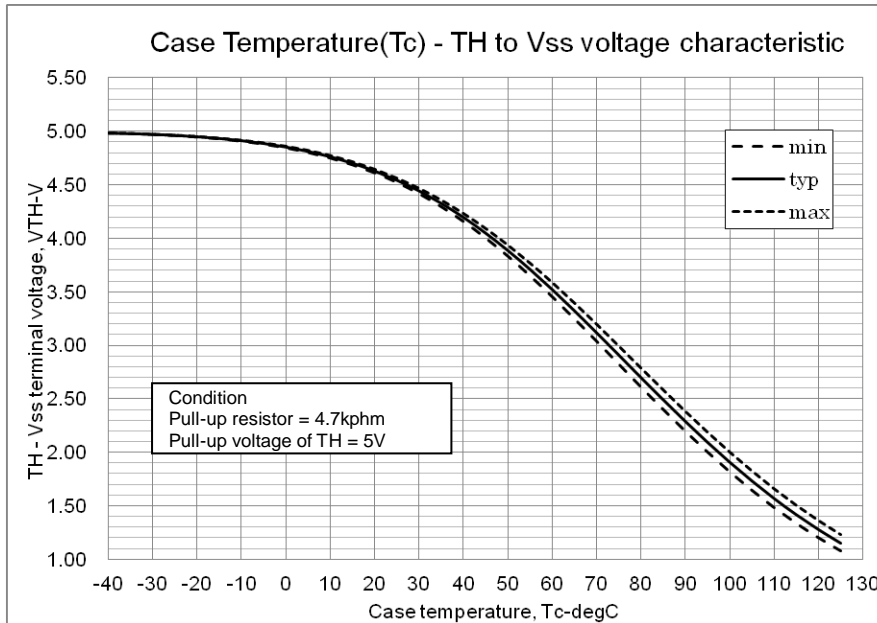


Fig.11 Variation of temperature sense voltage with thermistor temperature

Maximum Phase current

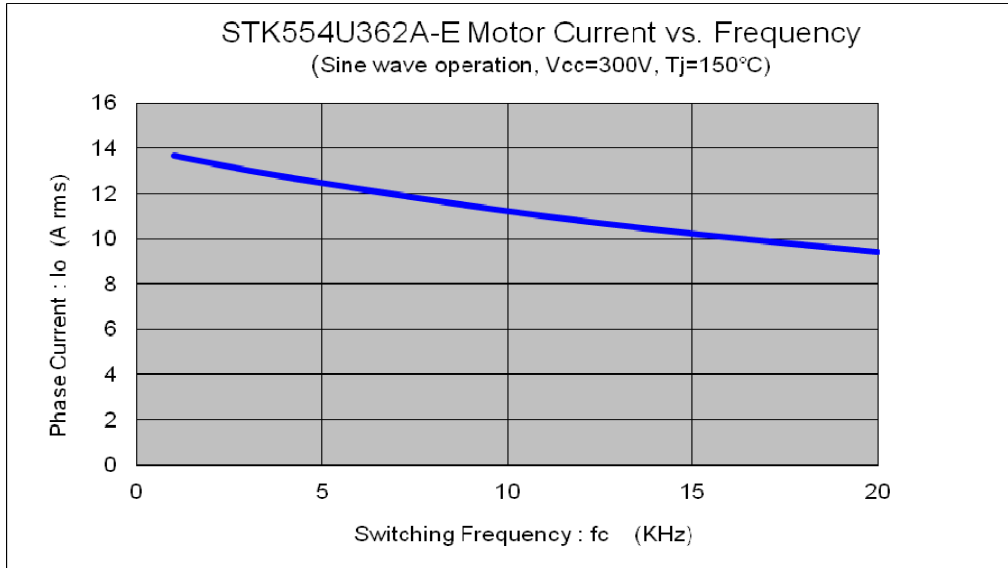


Fig.12 Maximum sinusoidal phase current as function of switching frequency at $T_c=100^{\circ}C$, $V_{cc}=300V$

Switching waveform

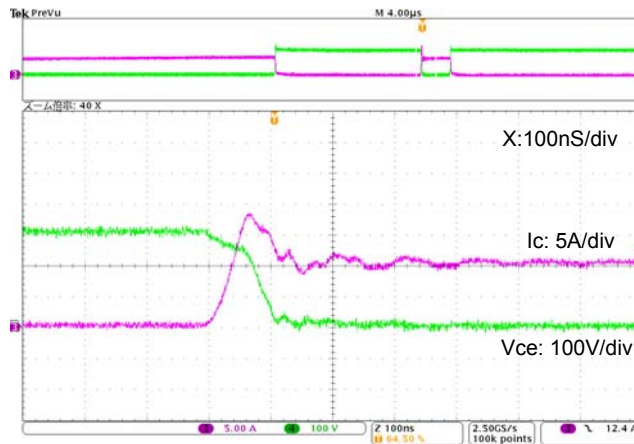


Fig. 13 IGBT Turn-on. Typical turn-on waveform at $T_c=100^{\circ}C$, $V_{cc}=300V$, $I_c=10A$

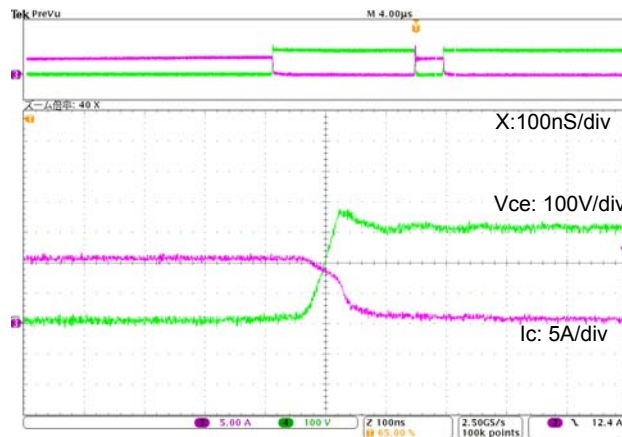


Fig. 14 IGBT Turn-off. Typical turn-off waveform $T_c=100^{\circ}C$, $V_{cc}=300V$, $I_c=10A$

CB capacitor value calculation for bootstrap circuit

Calculate condition

| Item | Symbol | Value | Unit |
|--|---------|-------|------|
| Upper side power supply. | VBS | 15 | V |
| Total gate charge of output power IGBT at 15V. | Qg | 89 | nC |
| Upper side power supply low voltage protection. | UVLO | 12 | V |
| Upper side power dissipation. | IDmax | 400 | μA |
| ON time required for CB voltage to fall from 15V to UVLO | Ton-max | - | s |

Capacitance calculation formula

CB must not be discharged below to the upper limit of the UVLO - the maximum allowable on-time (Ton-max) of the upper side is calculated as follows:

$$VBS * CB - Qg - IDmax * Ton-max = UVLO * CB$$

$$CB = (Qg + IDmax * Ton-max) / (VBS - UVLO)$$

The relationship between Ton-max and CB becomes as follows. CB is recommended to be approximately 3 times the value calculated above. The recommended value of CB is in the range of 1 to 47μF, however, the value needs to be verified prior to production.

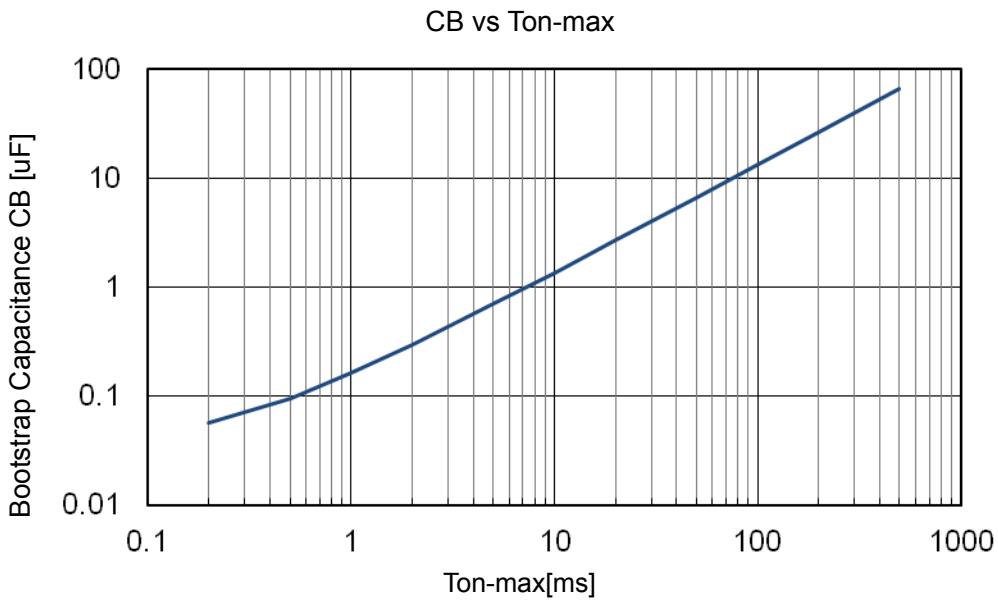


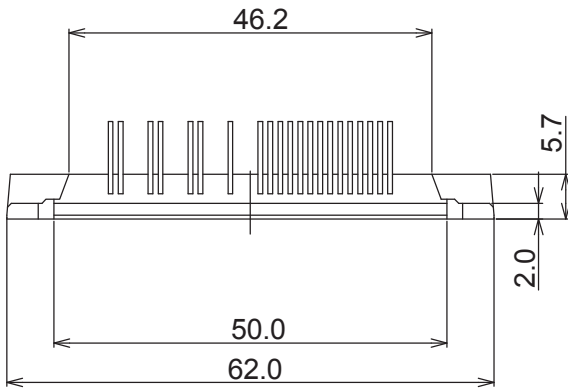
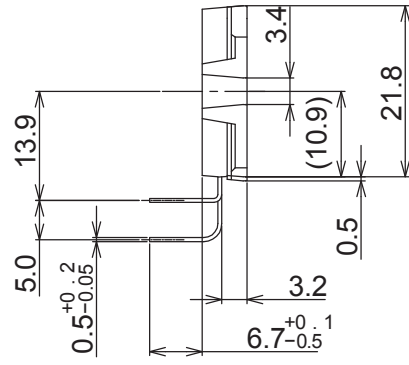
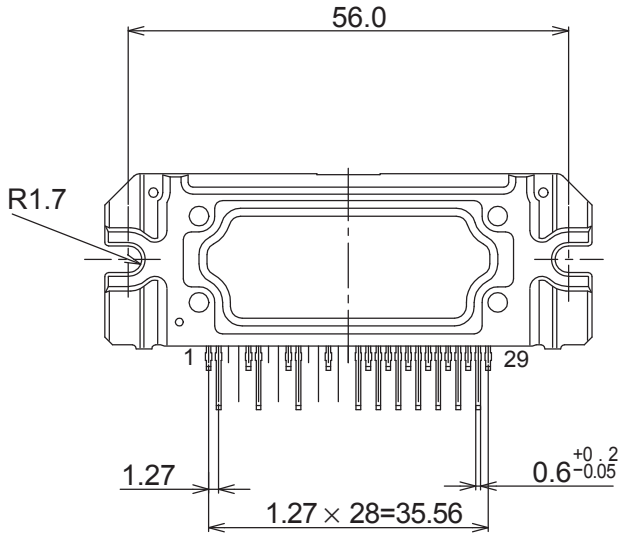
Fig.15 Ton-max vs CB characteristic

Package Dimensions

(unit : mm)

SIP29 56x21.8
CASE 127BW
ISSUE O

missing pin : 3,4,7,8,11,12,14,15



STK554U362A-E

ORDERING INFORMATION

| Device | Package | Shipping (Qty / Packing) |
|---------------|----------------------------|--------------------------|
| STK554U362A-E | SIP29 56x21.8 (Pb-Free) | 8 / Tube |

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