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CSD18540Q5B 60-V, N-Channel NexFET™ Power MOSFETs

1 Features

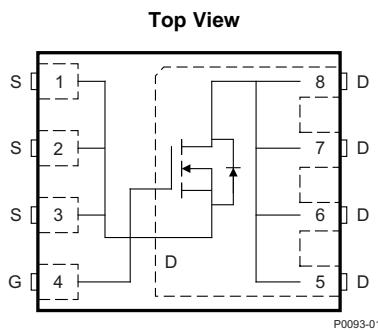
- Ultra-Low Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Lead-Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm × 6-mm Plastic Package

2 Applications

- DC-DC Conversion
- Secondary Side Synchronous Rectifier
- Isolated Converter Primary Side Switch
- Motor Control

3 Description

This 1.8-mΩ, 60-V NexFET™ power MOSFET is designed to minimize losses in power conversion applications with a SON 5-mm × 5-mm package.



$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	60		V
Q_g	Gate Charge Total (10 V)	41		nC
Q_{gd}	Gate Charge Gate-to-Drain	6.7		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 4.5\text{ V}$ $V_{GS} = 10\text{ V}$	2.6 1.8	$\text{m}\Omega$
$V_{GS(th)}$	Threshold Voltage	1.9		V

Product Summary

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD18540Q5B	2500	13-Inch Reel	SON 5.00-mm × 6.00-mm Plastic Package	Tape and Reel
CSD18540Q5BT	250	7-Inch Reel		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

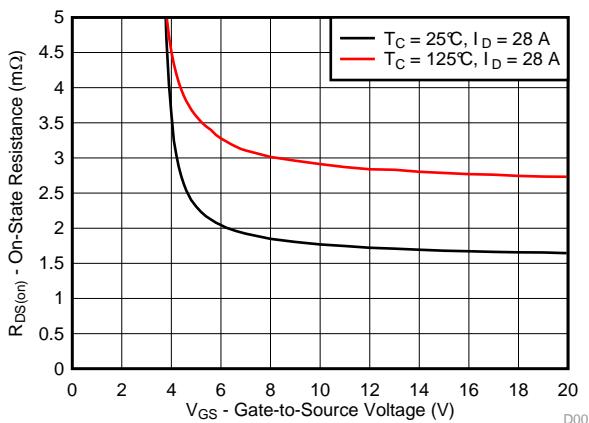
Ordering Information⁽¹⁾

$T_A = 25^\circ\text{C}$	VALUE	UNIT	
V_{DS}	Drain-to-Source Voltage	60	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D	Continuous Drain Current (Package Limited)	100	
	Continuous Drain Current (Silicon Limited), $T_C = 25^\circ\text{C}$	205	A
	Continuous Drain Current ⁽¹⁾	29	
I_{DM}	Pulsed Drain Current, $T_A = 25^\circ\text{C}$ ⁽²⁾	400	A
P_D	Power Dissipation ⁽¹⁾	3.8	
	Power Dissipation, $T_C = 25^\circ\text{C}$	188	W
T_J, T_{stg}	Operating Junction, Storage Temperature	-55 to 175	°C
E_{AS}	Avalanche Energy, Single Pulse $I_D = 80\text{ A}$, $L = 0.1\text{ mH}$, $R_G = 25\text{ }\Omega$	320	mJ

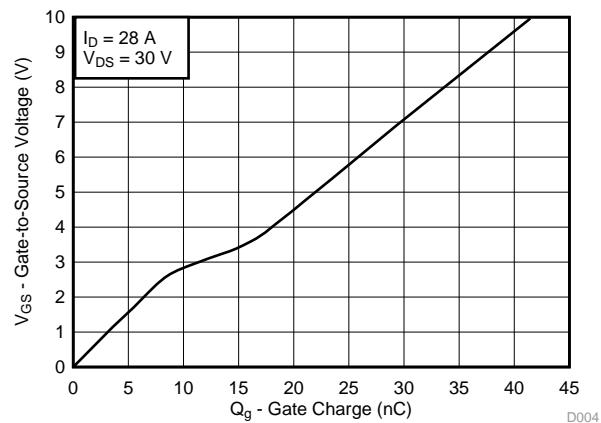
(1) Typical $R_{DS(on)} = 40^\circ\text{C}/\text{W}$ on a 1-in², 2-oz Cu pad on a 0.06-in thick FR4 PCB.

(2) Max $R_{\theta JC} = 0.8^\circ\text{C}/\text{W}$, pulse duration $\leq 100\text{ }\mu\text{s}$, duty cycle $\leq 1\%$.

$R_{DS(on)}$ vs V_{GS}



Gate Charge



An **IMPORTANT NOTICE** at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. **PRODUCTION DATA**.

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4 Revision History**Changes from Original (June 2014) to Revision A**

		Page
• Updated I_D values		1
• Updated P_D values		1
• Increased maximum temperature to 175°C		1
• Updated Figure 2		5
• Changed Figure 6 to extend temperature to 175°C		5
• Changed Figure 8 to extend temperature to 175°C		6
• Replotted Figure 10 using 175°C data		6
• Changed Figure 12 to extend temperature to 175°C		6
• Added Receiving Notification of Documentation Updates and Community Resources to Device and Documentation Support section		7
• Updated the mechanical drawing		8

5 Specifications

5.1 Electrical Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS					
BV_{DSS}	Drain-to-source voltage	$\text{V}_{\text{GS}} = 0 \text{ V}$, $\text{I}_D = 250 \mu\text{A}$	60		V
I_{DSS}	Drain-to-source leakage current	$\text{V}_{\text{GS}} = 0 \text{ V}$, $\text{V}_{\text{DS}} = 48 \text{ V}$		1	μA
I_{GSS}	Gate-to-source leakage current	$\text{V}_{\text{DS}} = 0 \text{ V}$, $\text{V}_{\text{GS}} = 20 \text{ V}$		100	nA
$\text{V}_{\text{GS}(\text{th})}$	Gate-to-source threshold voltage	$\text{V}_{\text{DS}} = \text{V}_{\text{GS}}$, $\text{I}_D = 250 \mu\text{A}$	1.5	1.9	2.3
$\text{R}_{\text{DS}(\text{on})}$	Drain-to-source on resistance	$\text{V}_{\text{GS}} = 4.5 \text{ V}$, $\text{I}_D = 28 \text{ A}$		2.6	3.3
		$\text{V}_{\text{GS}} = 10 \text{ V}$, $\text{I}_D = 28 \text{ A}$		1.8	2.2
g_{fs}	Transconductance	$\text{V}_{\text{DS}} = 6 \text{ V}$, $\text{I}_D = 28 \text{ A}$	116		S
DYNAMIC CHARACTERISTICS					
C_{iss}	Input capacitance	$\text{V}_{\text{GS}} = 0 \text{ V}$, $\text{V}_{\text{DS}} = 30 \text{ V}$, $f = 1 \text{ MHz}$	3250	4230	pF
C_{oss}	Output capacitance		622	808	pF
C_{rss}	Reverse transfer capacitance		15	20	pF
R_G	Series gate resistance		0.8	1.6	Ω
Q_g	Gate charge total (4.5 V)	$\text{V}_{\text{DS}} = 30 \text{ V}$, $\text{I}_D = 28 \text{ A}$	20	26	nC
Q_g	Gate charge total (10 V)		41	53	nC
Q_{gd}	Gate charge gate-to-drain		6.7		nC
Q_{gs}	Gate charge gate-to-source		8.8		nC
$\text{Q}_{\text{g}(\text{th})}$	Gate charge at V_{th}		6.3		nC
Q_{oss}	Output charge		83		nC
$\text{t}_{\text{d}(\text{on})}$	Turnon delay time	$\text{V}_{\text{DS}} = 30 \text{ V}$, $\text{V}_{\text{GS}} = 10 \text{ V}$, $\text{I}_{\text{DS}} = 28 \text{ A}$, $\text{R}_G = 0 \Omega$	6		ns
t_r	Rise time		9		ns
$\text{t}_{\text{d}(\text{off})}$	Turnoff delay time		20		ns
t_f	Fall time		3		ns
DIODE CHARACTERISTICS					
V_{SD}	Diode forward voltage	$\text{I}_{\text{SD}} = 28 \text{ A}$, $\text{V}_{\text{GS}} = 0 \text{ V}$	0.8	1	V
Q_{rr}	Reverse recovery charge	$\text{V}_{\text{DS}} = 30 \text{ V}$, $\text{I}_F = 28 \text{ A}$,	145		nC
t_{rr}	Reverse recovery time	$\text{dI}/\text{dt} = 300 \text{ A}/\mu\text{s}$	82		ns

5.2 Thermal Information

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$\text{R}_{\text{θJC}}$	Junction-to-case thermal resistance ⁽¹⁾			0.8	$^\circ\text{C}/\text{W}$
$\text{R}_{\text{θJA}}$	Junction-to-ambient thermal resistance ⁽¹⁾⁽²⁾			50	

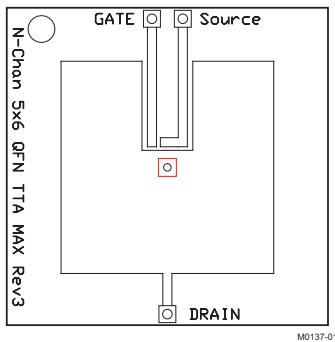
(1) $\text{R}_{\text{θJC}}$ is determined with the device mounted on a 1-in² (6.45-cm²), 2-oz (0.071-mm) thick Cu pad on a 1.5-in \times 1.5-in (3.81-cm \times 3.81-cm), 0.06-in (1.52-mm) thick FR4 PCB. $\text{R}_{\text{θJC}}$ is specified by design, whereas $\text{R}_{\text{θJA}}$ is determined by the user's board design.

(2) Device mounted on FR4 material with 1-in² (6.45-cm²), 2-oz (0.071-mm) thick Cu.

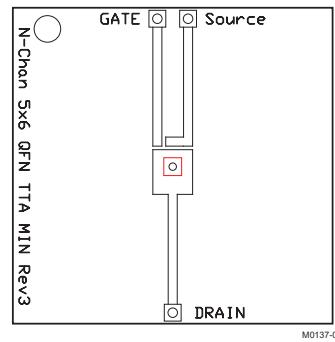
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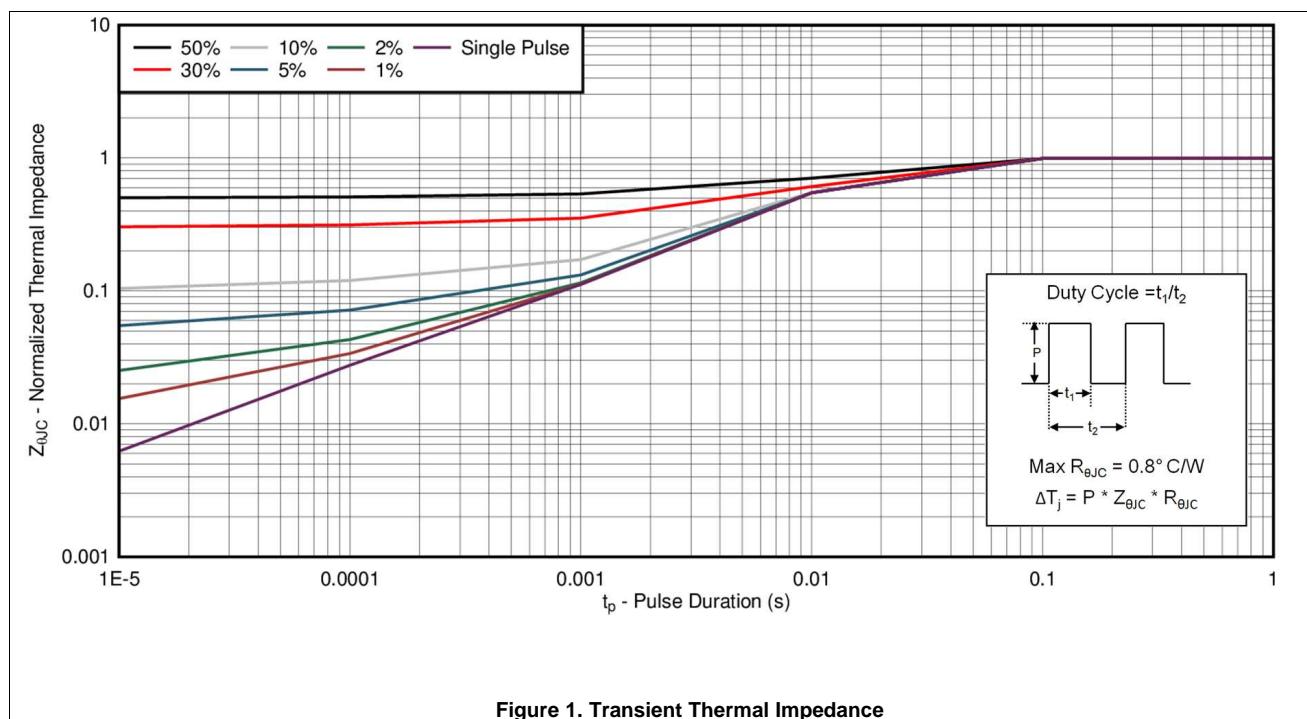
Max $R_{\theta JA} = 50^{\circ}\text{C}/\text{W}$
when mounted on 1-in²
(6.45-cm²) of
2-oz (0.071-mm) thick
Cu.



Max $R_{\theta JA} = 125^{\circ}\text{C}/\text{W}$
when mounted on a
minimum pad area of
2-oz (0.071-mm) thick
Cu.

5.3 Typical MOSFET Characteristics

$T_A = 25^{\circ}\text{C}$ (unless otherwise stated)



Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

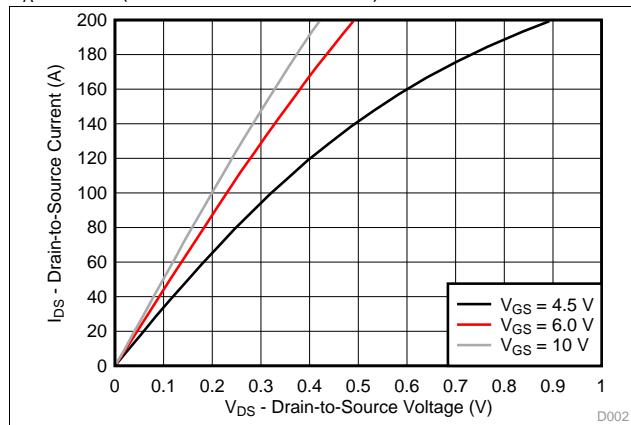


Figure 2. Saturation Characteristics

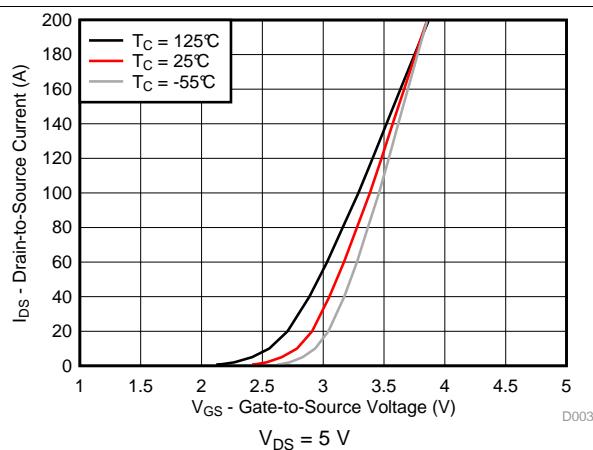


Figure 3. Transfer Characteristics

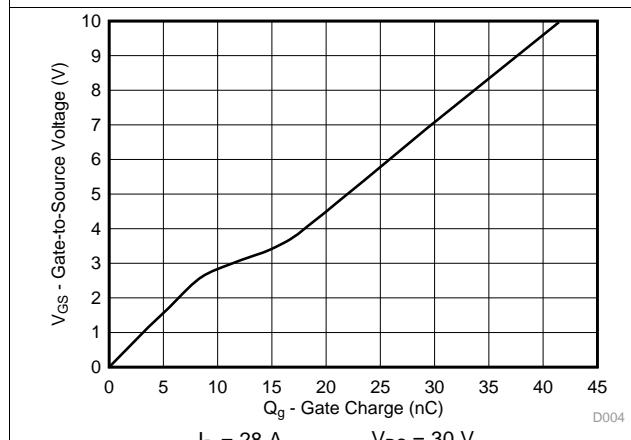


Figure 4. Gate Charge

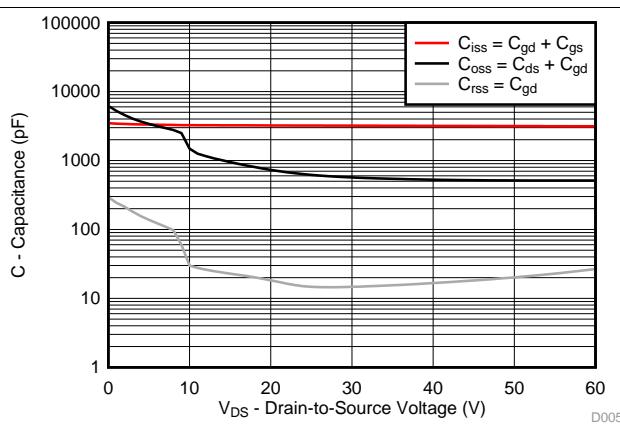


Figure 5. Capacitance

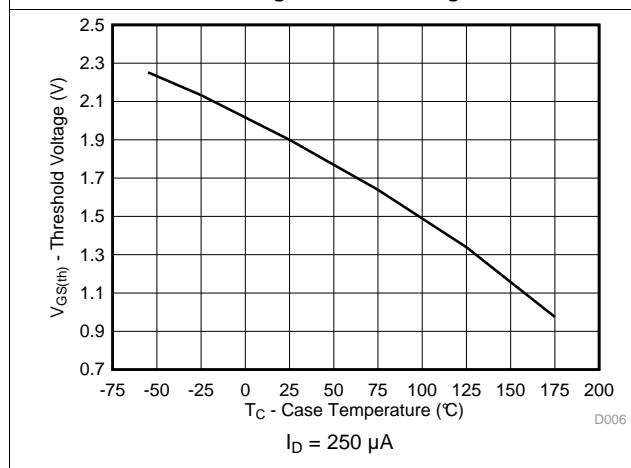


Figure 6. Threshold Voltage vs Temperature

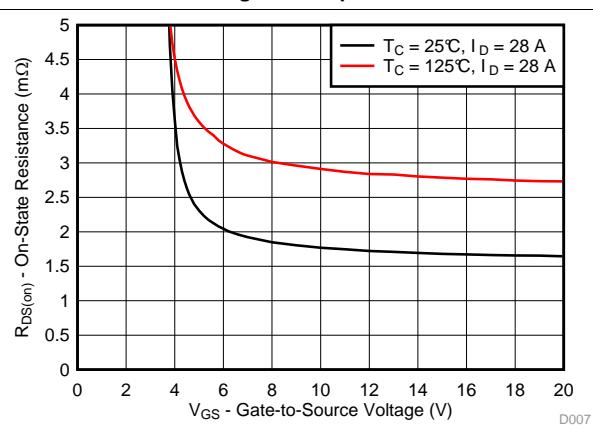


Figure 7. On-State Resistance vs Gate-to-Source Voltage

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Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

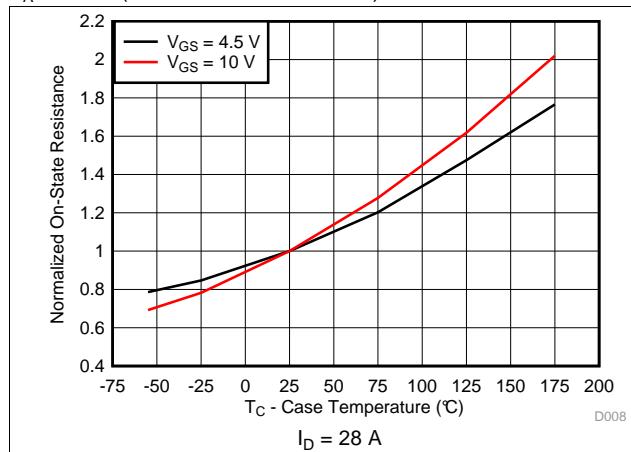


Figure 8. Normalized On-State Resistance vs Temperature

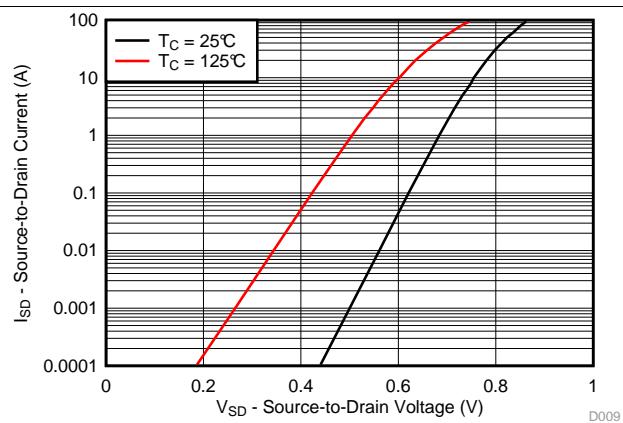


Figure 9. Typical Diode Forward Voltage

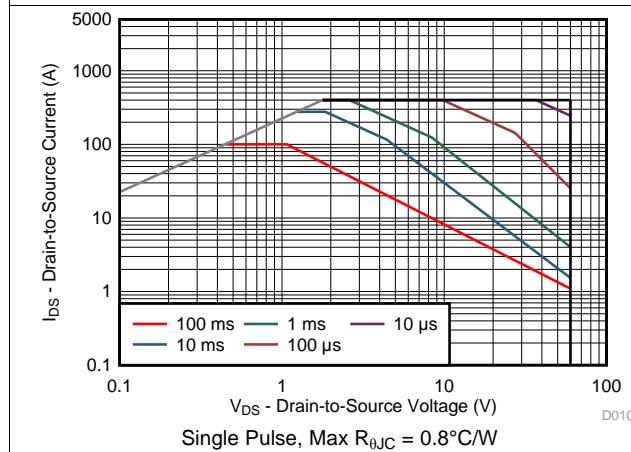


Figure 10. Maximum Safe Operating Area

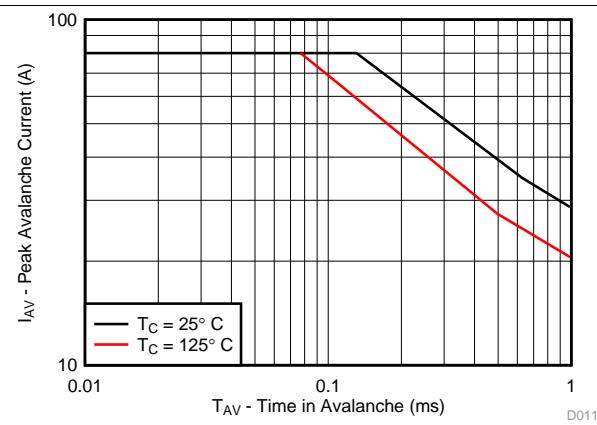


Figure 11. Single Pulse Unclamped Inductive Switching

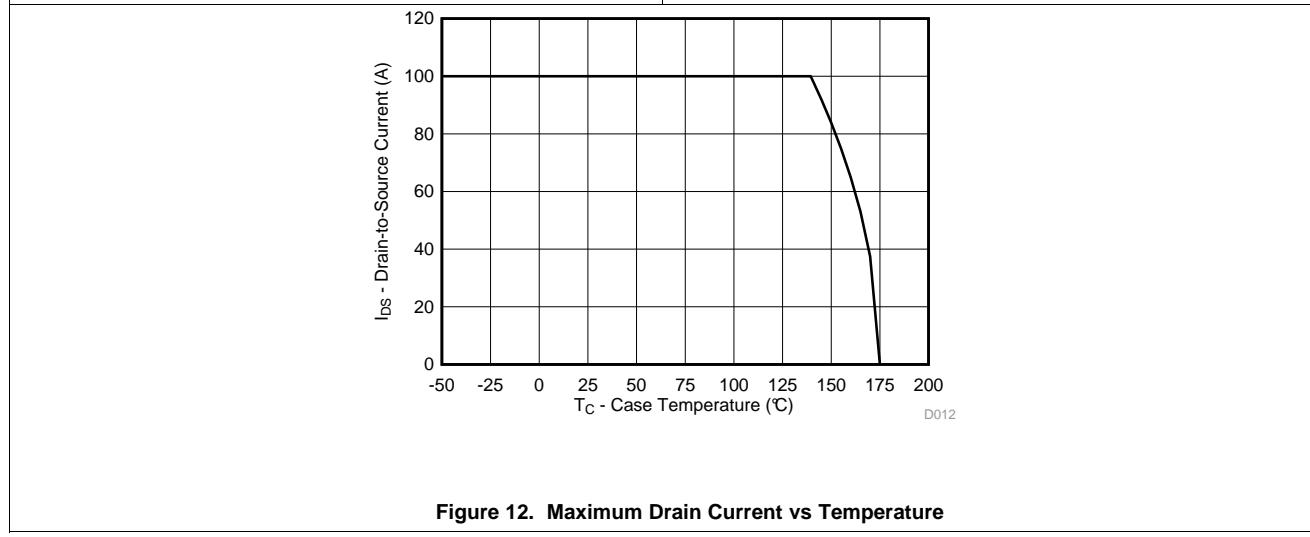


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 Trademarks

NexFET, E2E are trademarks of Texas Instruments.

All other trademarks are the property of their respective owners.

6.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.5 Glossary

[SLYZ022 — TI Glossary](#).

This glossary lists and explains terms, acronyms, and definitions.

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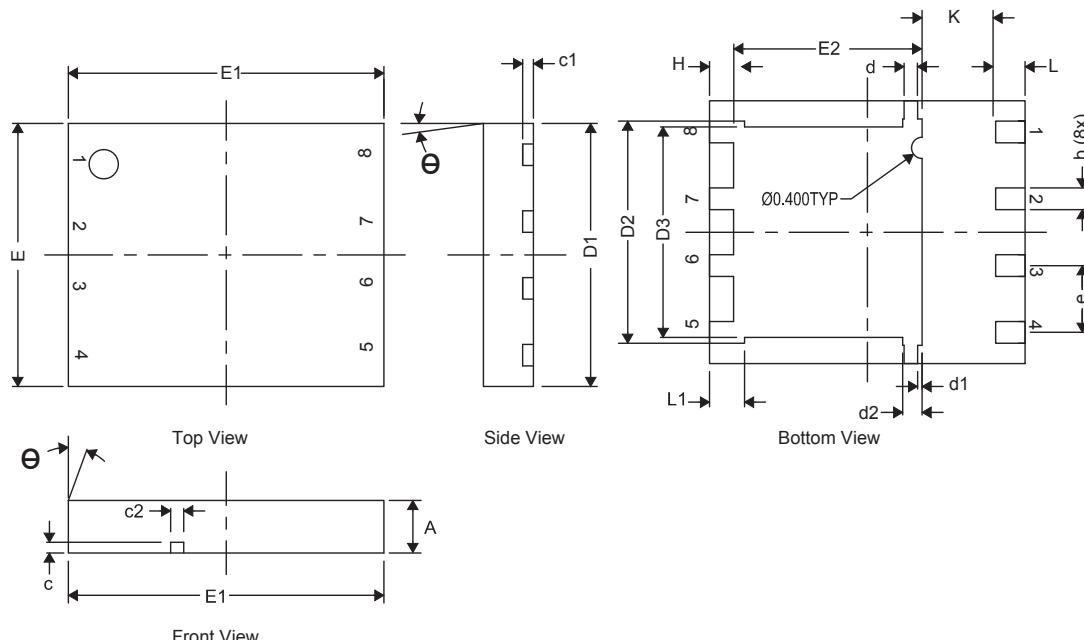
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7 Mechanical, Packaging, and Orderable Information

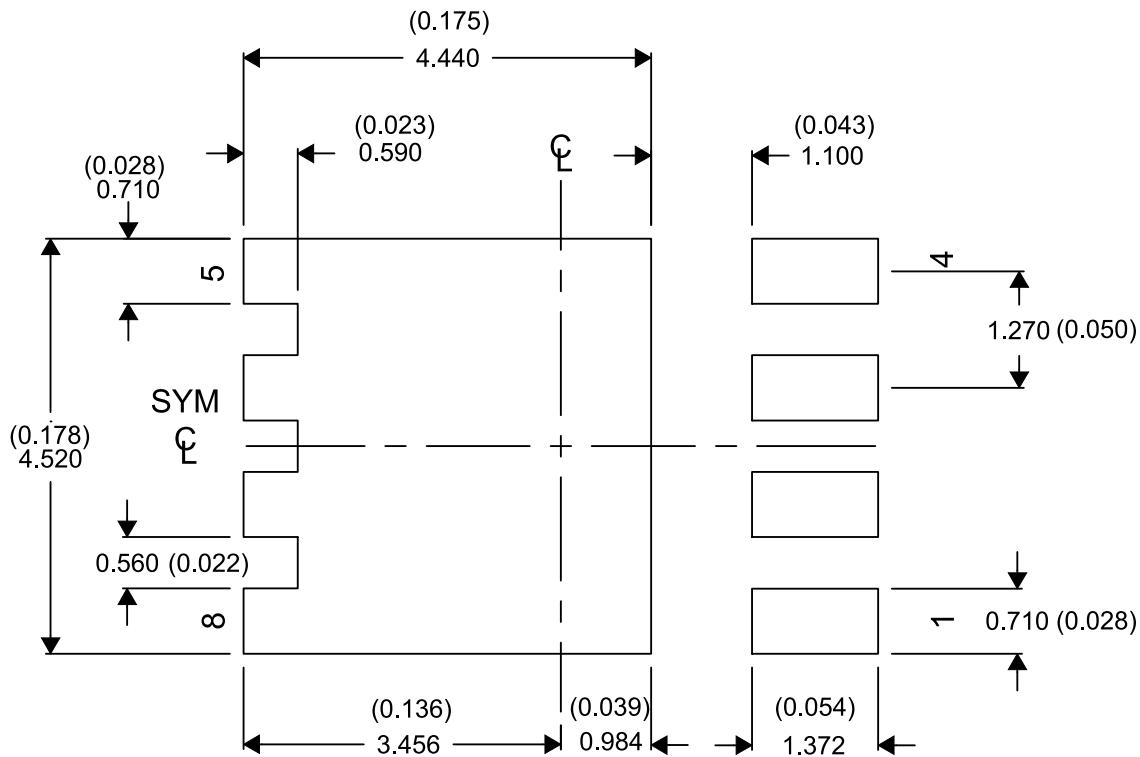
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Q5B Package Dimensions



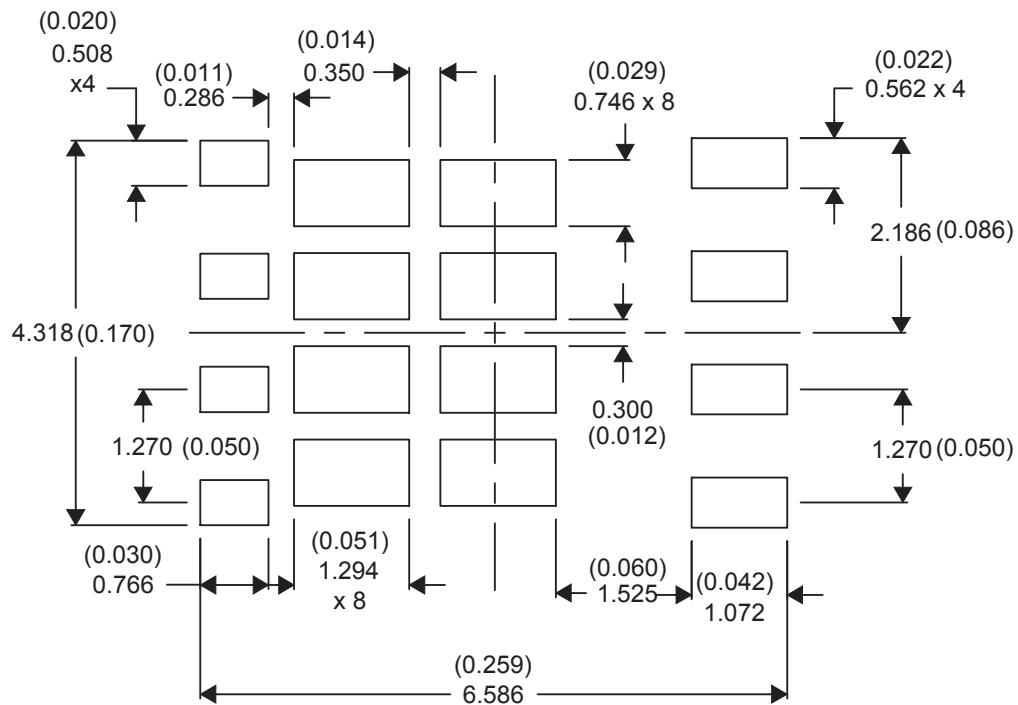
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.80	1.00	1.05
b	0.36	0.41	0.46
c	0.15	0.20	0.25
c1	0.15	0.20	0.25
c2	0.20	0.25	0.30
D1	4.90	5.00	5.10
D2	4.12	4.22	4.32
D3	3.90	4.00	4.10
d	0.20	0.25	0.30
d1	0.085 TYP		
d2	0.319	0.369	0.419
E	4.90	5.00	5.10
E1	5.90	6.00	6.10
E2	3.48	3.58	3.68
e	1.27 TYP		
H	0.36	0.46	0.56
L	0.46	0.56	0.66
L1	0.57	0.67	0.77
θ	0°	—	—
K	1.40 TYP		

7.2 Recommended PCB Pattern



For recommended circuit layout for PCB designs, see application note [SLPA005 – Reducing Ringing Through PCB Layout Techniques](#).

7.3 Recommended Stencil Pattern

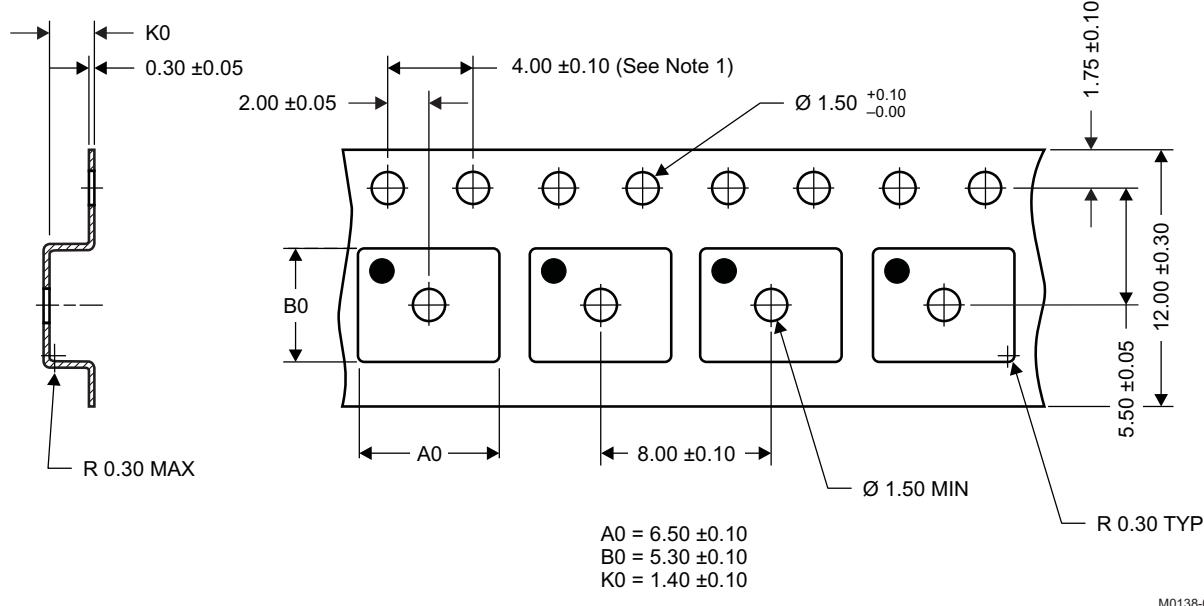


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7.4 Q5B Tape and Reel Information



Notes:

1. 10-sprocket hole-pitch cumulative tolerance ±0.2
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified).
5. A0 and B0 measured on a plane 0.3 mm above the bottom of the pocket

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD18540Q5B	ACTIVE	VSON-CLIP	DNK	8	2500	Pb-Free (RoHS Exempt)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-55 to 150	CSD18540	Samples
CSD18540Q5BT	ACTIVE	VSON-CLIP	DNK	8	250	Pb-Free (RoHS Exempt)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-55 to 150	CSD18540	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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