Excellent Integrated System Limited

Stocking Distributor

Click to view price, real time Inventory, Delivery & Lifecycle Information:

Vishay Semiconductor/Diodes Division
VS-20CWT10FNTR

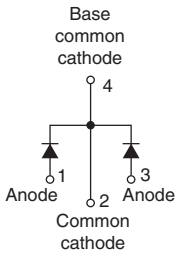
For any questions, you can email us directly:
sales@integrated-circuit.com

VS-20CUT10, VS-20CWT10FN

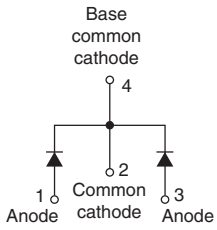
High Performance Schottky Generation 5.0, 2 x 10 A

I-PAK (TO-251AA)

D-PAK (TO-252AA)



VS-20CUT10



VS-20CWT10FN

FEATURES

- 175 °C high performance Schottky diode
- Very low forward voltage drop
- Extremely low reverse leakage
- Optimized V_F vs. I_R trade off for high efficiency
- Increased ruggedness for reverse avalanche capability
- RBSOA available
- Negligible switching losses
- Submicron trench technology
- Compliant to RoHS Directive 2002/95/EC

Pb e3 RoHS COMPLIANT

APPLICATIONS

- High efficiency SMPS
- High frequency switching
- Output rectification
- Reverse battery protection
- Freewheeling
- DC/DC systems
- Increased power density systems

PRODUCT SUMMARY	
Package	D-PAK (TO-252AA), I-PAK (TO-251AA)
$I_{F(AV)}$	2 x 10 A
V_R	100 V
V_F at I_F	0.66 V
I_{RM} max.	4 mA at 125 °C
T_J max.	175 °C
Diode variation	Common cathode
E_{AS}	54 mJ

MAJOR RATINGS AND CHARACTERISTICS			
SYMBOL	CHARACTERISTICS	VALUES	UNITS
V_{RRM}		100	V
V_F	10 Apk, T_J = 125 °C (typical, per leg)	0.615	V
T_J	Range	- 55 to 175	°C

VOLTAGE RATINGS				
PARAMETER	SYMBOL	TEST CONDITIONS	VS-20CUT10 VS-20CWT10FN	UNITS
Maximum DC reverse voltage	V_R	T_J = 25 °C	100	V

ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum average forward current	per leg	$I_{F(AV)}$	50 % duty cycle at T_C = 159 °C, rectangular waveform		10	A
	per device				20	
Maximum peak one cycle non-repetitive surge current per leg		I_{FSM}	5 µs sine or 3 µs rect. pulse	Following any rated load condition and with rated V_{RRM} applied	610	A
			10 ms sine or 6 ms rect. pulse		110	
Non-repetitive avalanche energy per leg		E_{AS}	T_J = 25 °C, I_{AS} = 3 A, L = 12 mH		54	mJ
Repetitive avalanche current per leg		I_{AR}	Limited by frequency of operation and time pulse duration so that $T_J < T_J$ max. I_{AS} at T_J max. as a function of time pulse (see fig. 8)		I_{AS} at T_J max.	A

ELECTRICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS		TYP.	MAX.	UNITS
Forward voltage drop per leg	V_{FM} (1)	10 A	T_J = 25 °C	0.735	0.810	V
		20 A		0.840	0.890	
		10 A	T_J = 125 °C	0.615	0.660	
		20 A		0.730	0.770	
Reverse leakage current per leg	I_{RM} (1)	T_J = 25 °C	V_R = Rated V_R	-	50	µA
		T_J = 125 °C		-	4	mA
Junction capacitance per leg	C_T	V_R = 5 V_{DC} (test signal range 100 kHz to 1 MHz), 25 °C		400	-	pF
Series inductance per leg	L_S	Measured lead to lead 5 mm from package body		8.0	-	nH
Maximum voltage rate of change	dV/dt	Rated V_R		-	10 000	V/µs

Note

(1) Pulse width < 300 µs, duty cycle < 2 %

THERMAL - MECHANICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction and storage temperature range	T_J, T_{Stg}		- 55 to 175	°C
Maximum thermal resistance, junction to case per leg	R_{thJC}	DC operation	2	°C/W
Maximum thermal resistance, junction to case per device			1	
Typical thermal resistance, case to heatsink	R_{thCS}		0.3	
Approximate weight			0.3	g
			0.01	oz.
Marking device		Case style I-PAK	20CUT10	
		Case style D-PAK	20CWT10FN	

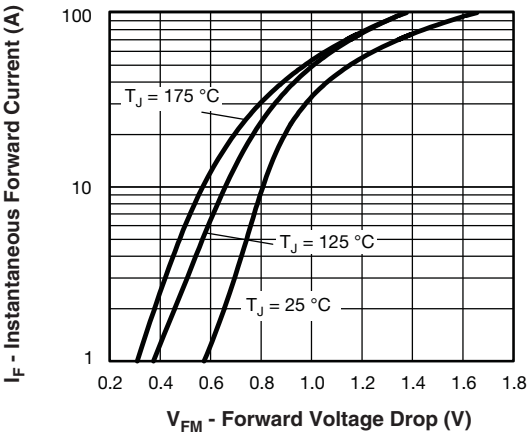


Fig. 1 - Maximum Forward Voltage Drop Characteristics

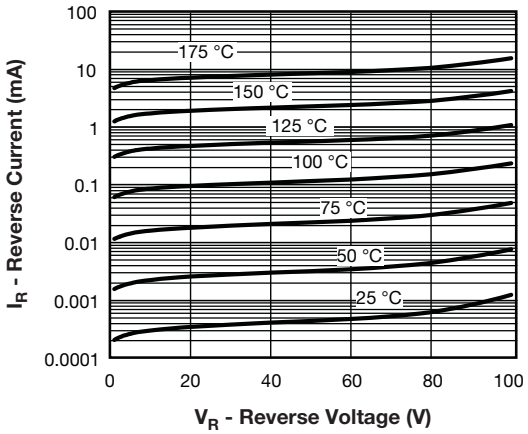


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage

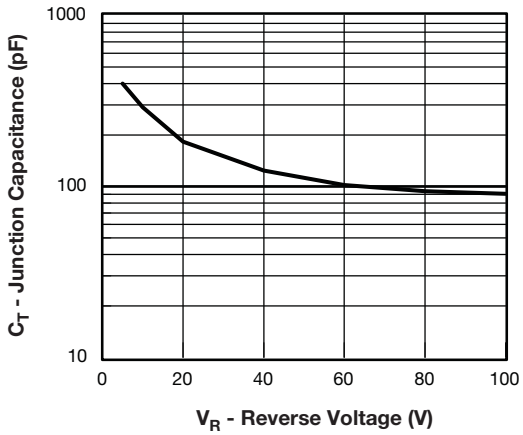


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage

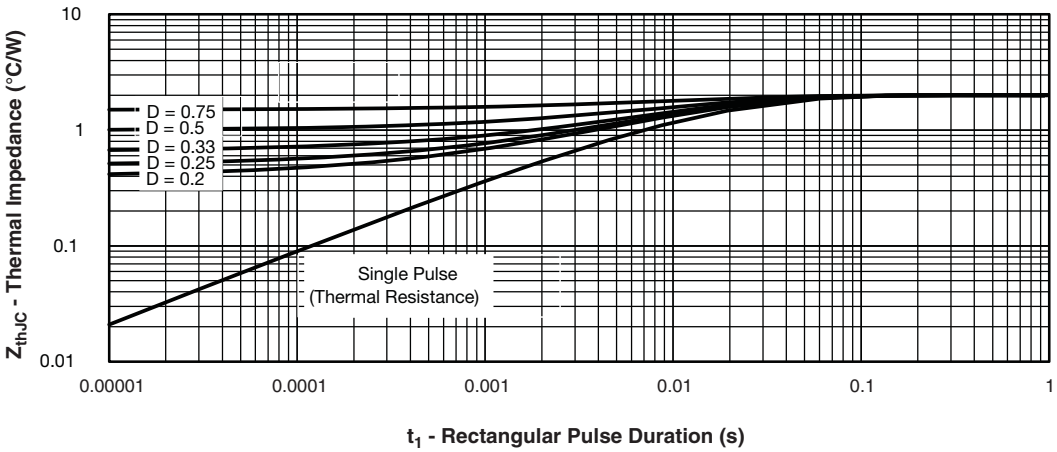


Fig. 4 - Maximum Thermal Impedance Z_{thJC} Characteristics

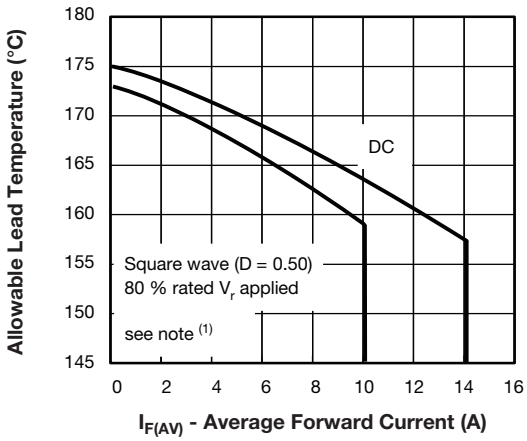


Fig. 5 - Maximum Allowable Case Temperature vs. Average Forward Current

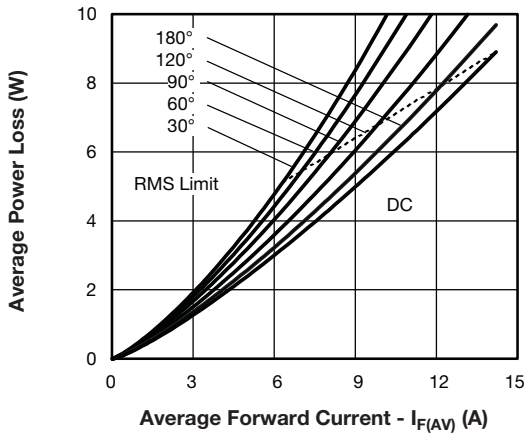


Fig. 6 - Forward Power Loss Characteristics

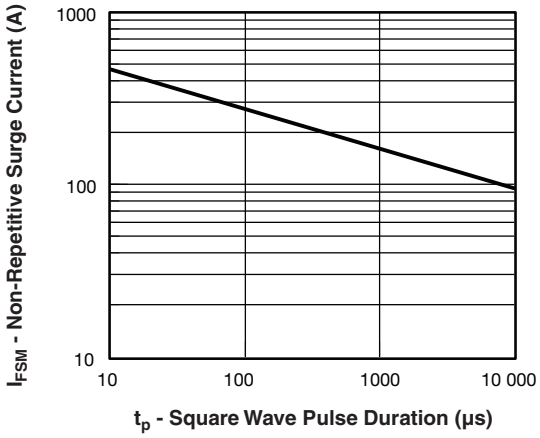


Fig. 7 - Maximum Non-Repetitive Surge Current

Note

(1) Formula used: $T_C = T_J - (Pd + Pd_{REV}) \times R_{thJC}$;
Pd = Forward power loss = $I_{F(AV)} \times V_{FM}$ at ($I_{F(AV)}$/D) (see fig. 6);
Pd_{REV} = Inverse power loss = $V_{R1} \times I_R (1 - D)$; I_R at V_{R1} = 80 % rated V_R

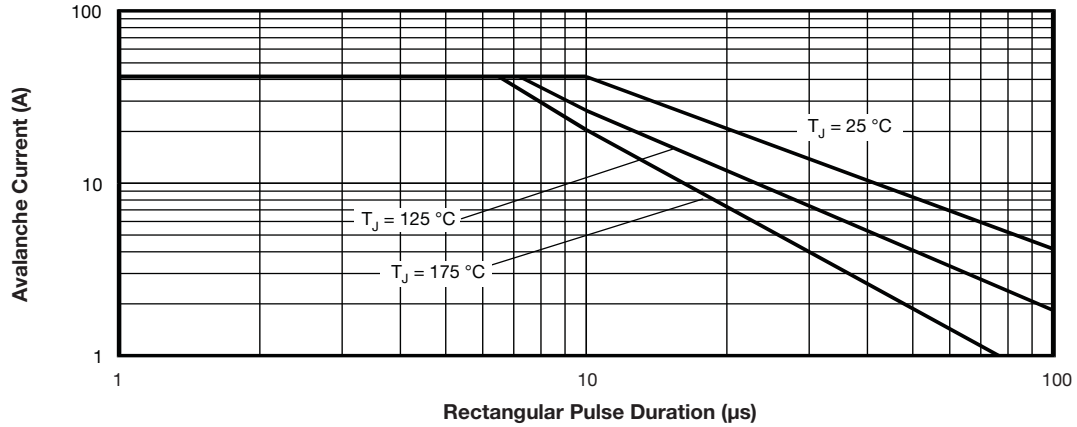


Fig. 8 - Reverse Bias Safe Operating Area (Avalanche Current vs. Rectangular Pulse Duration)

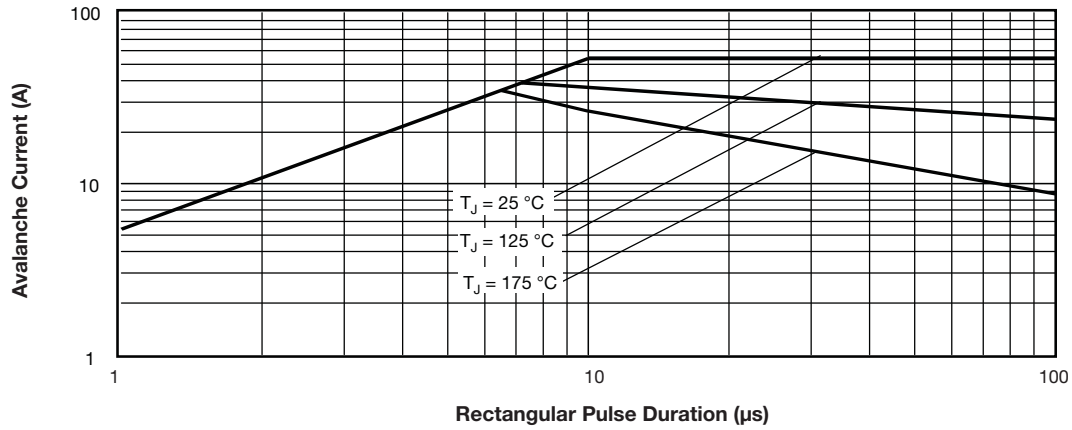


Fig. 9 - Reverse Bias Safe Operating Area (Avalanche Energy vs. Rectangular Pulse Duration)

ORDERING INFORMATION TABLE

Device code

VS-	20	C	U	T	10	FN	TRL
1	2	3	4	5	6	7	8

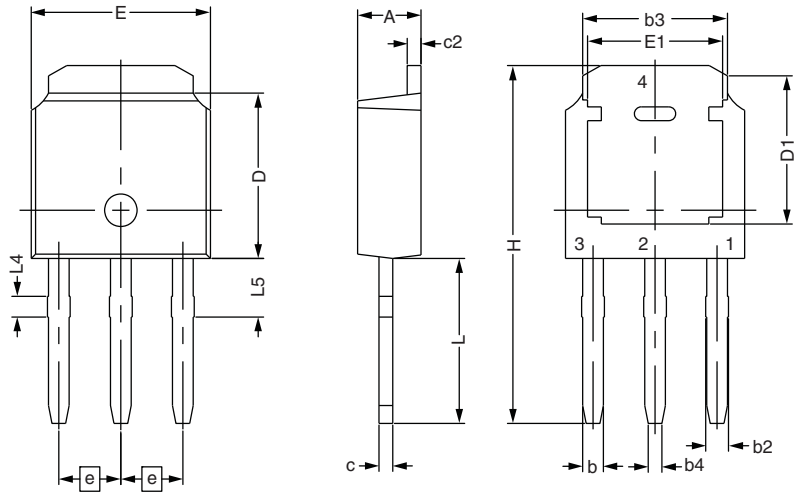
1 - Vishay Semiconductors product
2 - Current rating (20 A)
3 - Circuit configuration:
C = Common cathode
4 - Package:
- U = I-PAK
- W = D-PAK

5 - T = Trench
6 - Voltage rating (10 = 100 V)
7 - TO-252AA (D-PAK)
8 - D-PAK, I-PAK:
None = Tube (75 pieces)
D-PAK only:
- TR = Tape and reel
- TRL = Tape and reel (left oriented)
- TRR = Tape and reel (right oriented)

LINKS TO RELATED DOCUMENTS		
Dimensions	I-PAK (TO-251AA)	www.vishay.com/doc?95024
	D-PAK (TO-252AA)	www.vishay.com/doc?95448
Part marking information	I-PAK (TO-251AA)	www.vishay.com/doc?95025
	D-PAK (TO-252AA)	www.vishay.com/doc?95059
Packaging information		www.vishay.com/doc?95033
SPICE model		www.vishay.com/doc?95041

I-PAK - S

DIMENSIONS FOR I-PAK - S in millimeters



SYMBOL	DIMENSIONAL REQUIREMENTS		
	MIN.	NOM.	MAX.
E	6.40	6.60	6.70
L	3.98	4.13	4.28
L4	0.66	0.76	0.86
L5	1.96	2.16	2.36
D	6.00	6.10	6.20
H	11.05	11.25	11.45
b	0.64	0.76	0.88
b2	0.77	0.84	1.14
b3	5.21	5.34	5.46
b4	0.41	0.51	0.61
e	2.286 BSC		
A	2.20	2.30	2.38
c	0.40	0.50	0.60
c2	0.40	0.50	0.60
D1	5.30	-	-
E1	4.40	-	-

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