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[Vishay Semiconductor/Diodes Division](#)
[VS-20TT100](#)

For any questions, you can email us directly:

sales@integrated-circuit.com



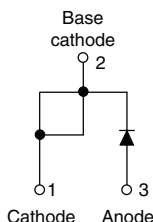
20TT100

Vishay High Power Products

High Performance Schottky Generation 5.0, 20 A



TO-220AC



FEATURES

- 175 °C high performance Schottky diode
- Very low forward voltage drop
- Extremely low reverse leakage
- Optimized V_F vs. I_R trade off for high efficiency
- Increased ruggedness for reverse avalanche capability
- RBSOA available
- Negligible switching losses
- Submicron trench technology
- Full lead (Pb)-free and RoHS compliant devices
- Designed and qualified for industrial level



RoHS
COMPLIANT

PRODUCT SUMMARY

$I_{F(AV)}$	20 A
V_R	100 V
V_F at 20 A at 125 °C	0.67 V

APPLICATIONS

- High efficiency SMPS
- Automotive
- High frequency switching
- Output rectification
- Reverse battery protection
- Freewheeling
- Dc-to-dc systems
- Increased power density systems

MAJOR RATINGS AND CHARACTERISTICS

SYMBOL	CHARACTERISTICS	VALUES	UNITS
V_{RRM}		100	V
V_F	20 Apk, $T_J = 125$ °C (typical)	0.63	
T_J	Range	- 55 to 175	°C

VOLTAGE RATINGS

PARAMETER	SYMBOL	TEST CONDITIONS	20TT100	UNITS
Maximum DC reverse voltage	V_R	$T_J = 25$ °C	100	V

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum average forward current	$I_{F(AV)}$	50 % duty cycle at $T_C = 160$ °C, rectangular waveform	20	A
Maximum peak one cycle non-repetitive surge current	I_{FSM}	5 μ s sine or 3 μ s rect. pulse	900	
		10 ms sine or 6 ms rect. pulse	300	
Non-repetitive avalanche energy	E_{AS}	$T_J = 25$ °C, $I_{AS} = 1.5$ A, $L = 60$ mH	67.5	mJ
Repetitive avalanche current	I_{AR}	Limited by frequency of operation and time pulse duration so that $T_J < T_{J \text{ max.}}$. I_{AS} at $T_J \text{ max.}$ as a function of time pulse See fig. 8	I_{AS} at $T_J \text{ max.}$	A

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ELECTRICAL SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CONDITIONS		TYP.	MAX.	UNITS
Forward voltage drop	V _{FM} ⁽¹⁾	20 A	T _J = 25 °C	-	0.8	V
		40 A		-	0.95	
		20 A	T _J = 125 °C	-	0.67	
		40 A		-	0.8	
Reverse leakage current	I _{RM} ⁽¹⁾	T _J = 25 °C	V _R = Rated V _R	-	150	μA
		T _J = 125 °C		-	6	mA
Junction capacitance	C _T	V _R = 5 V _{DC} (test signal range 100 kHz to 1 MHz) 25 °C		850	-	pF
Series inductance	L _S	Measured lead to lead 5 mm from package body		8.0	-	nH
Maximum voltage rate of change	dV/dt	Rated V _R		-	10 000	V/μs

Note

(1) Pulse width < 300 μs , duty cycle < 2 %

THERMAL - MECHANICAL SPECIFICATIONS					
PARAMETER		SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction and storage temperature range		T _J , T _{Stg}		- 55 to 175	°C
Maximum thermal resistance, junction to case		R _{thJC}	DC operation	2	°C/W
Typical thermal resistance, case to heatsink		R _{thCS}	Mounting surface, smooth and greased	0.5	
Approximate weight				2	g
				0.07	oz.
Mounting torque	minimum			6 (5)	kgf · cm (lbf · in)
	maximum			12 (10)	
Marking device			Case style TO-220AC	20TT100	



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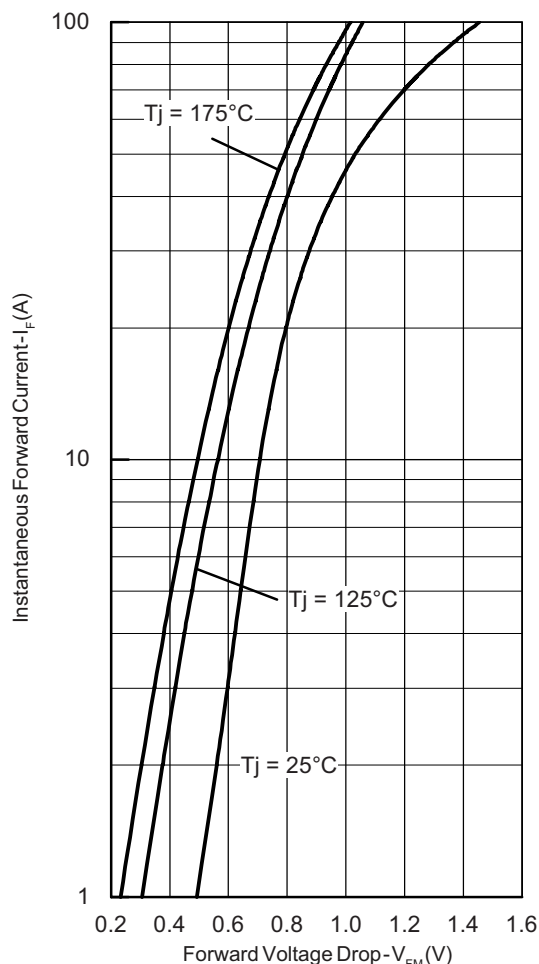


Fig. 1 - Maximum Forward Voltage Drop Characteristics

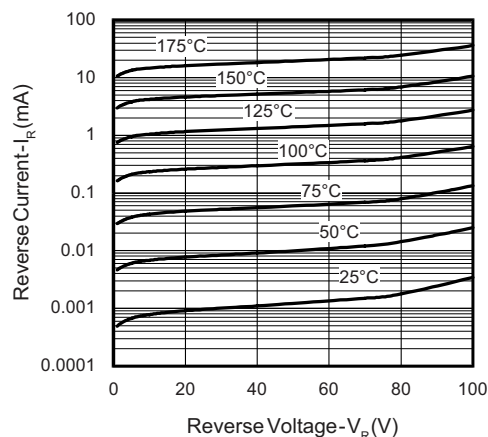


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage

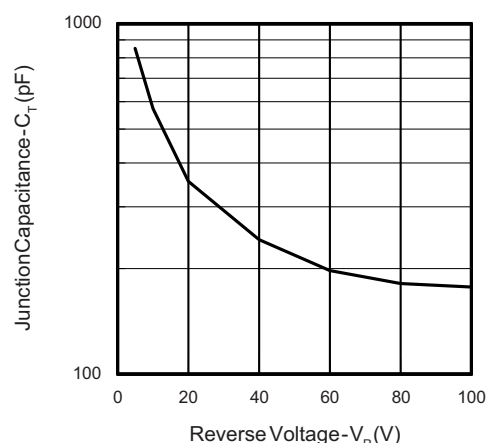


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage

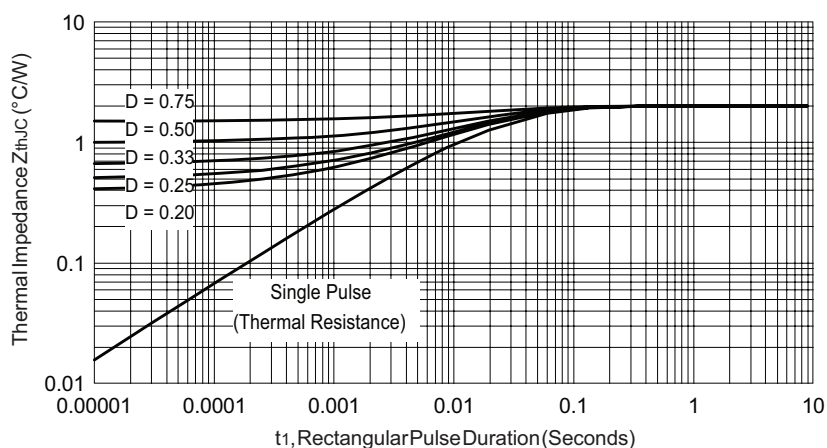


Fig. 4 - Maximum Thermal Impedance Z_{thJC} Characteristics

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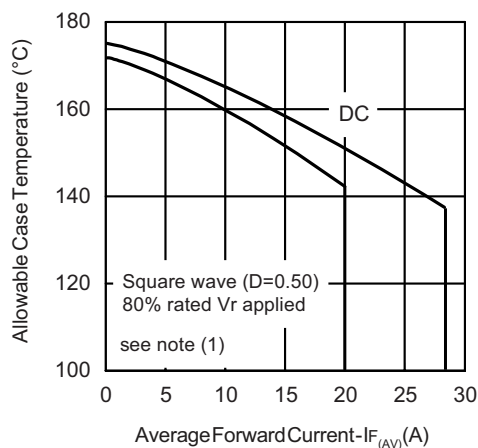


Fig. 5 - Maximum Allowable Case Temperature vs. Average Forward Current

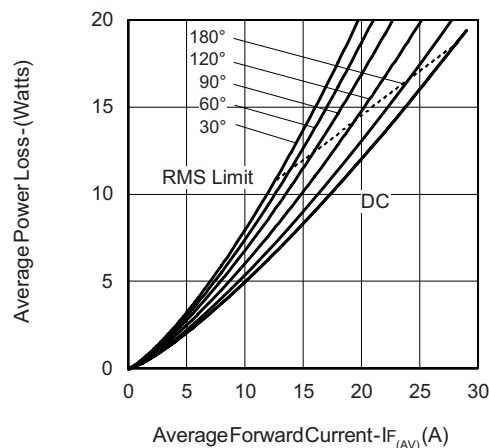


Fig. 6 - Forward Power Loss Characteristics

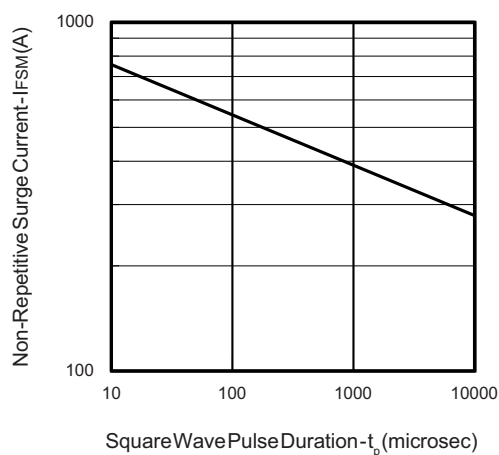


Fig. 7 - Maximum Non-Repetitive Surge Current

Note

(1) Formula used: $T_C = T_J - (P_d + P_{dREV}) \times R_{thJC}$;

P_d = Forward power loss = $I_{F(AV)} \times V_{FM}$ at $(I_{F(AV)}/D)$ (see fig. 6);

P_{dREV} = Inverse power loss = $V_{R1} \times I_R (1 - D)$; I_R at $V_{R1} = 80\%$ rated V_R



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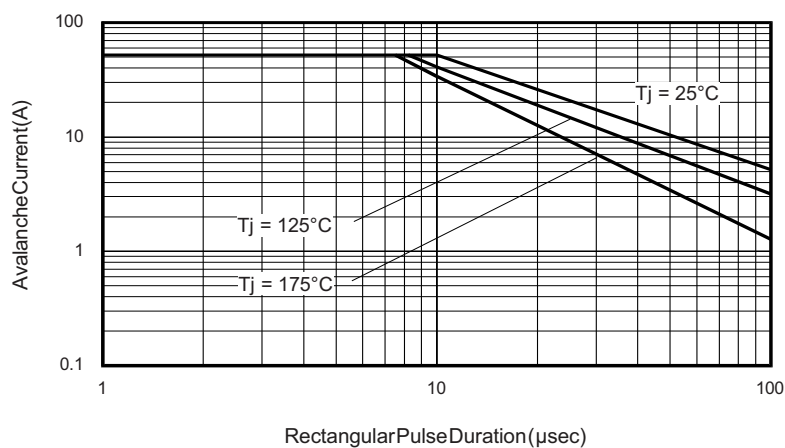


Fig. 8 - Reverse Bias Safe Operating Area (Avalanche Current vs. Rectangular Pulse Duration)

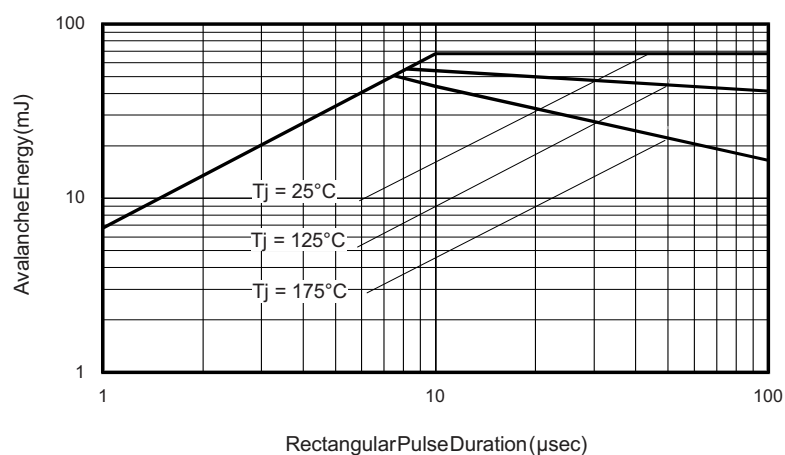


Fig. 9 - Reverse Bias Safe Operating Area (Avalanche Energy vs. Rectangular Pulse Duration)

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ORDERING INFORMATION TABLE

Device code	20	T	T	100
	1	2	3	4
	1	-	-	-
	2	-	-	-
	3	-	-	-
	4	-	-	-

Tube standard pack quantity: 50 pieces

LINKS TO RELATED DOCUMENTS	
Dimensions	http://www.vishay.com/doc?95221
Part marking information	http://www.vishay.com/doc?95224
SPICE model	http://www.vishay.com/doc?95228

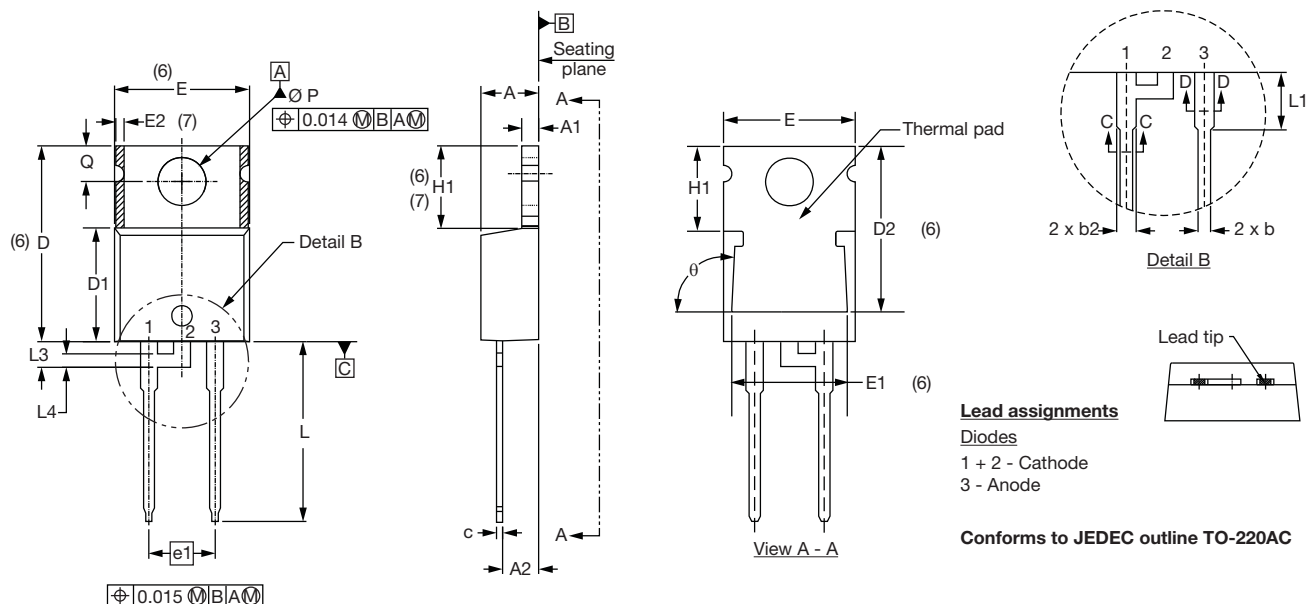


Outline Dimensions

Vishay Semiconductors

TO-220AC

DIMENSIONS in millimeters and inches



SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	4.25	4.65	0.167	0.183	
A1	1.14	1.40	0.045	0.055	
A2	2.56	2.92	0.101	0.115	
b	0.69	1.01	0.027	0.040	
b1	0.38	0.97	0.015	0.038	4
b2	1.20	1.73	0.047	0.068	
b3	1.14	1.73	0.045	0.068	4
c	0.36	0.61	0.014	0.024	
c1	0.36	0.56	0.014	0.022	4
D	14.85	15.25	0.585	0.600	3
D1	8.38	9.02	0.330	0.355	
D2	11.68	12.88	0.460	0.507	6
E	10.11	10.51	0.398	0.414	3, 6

SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
E1	6.86	8.89	0.270	0.350	6
E2	-	0.76	-	0.030	7
e	2.41	2.67	0.095	0.105	
e1	4.88	5.28	0.192	0.208	
H1	6.09	6.48	0.240	0.255	6, 7
L	13.52	14.02	0.532	0.552	
L1	3.32	3.82	0.131	0.150	2
L3	1.78	2.13	0.070	0.084	
L4	0.76	1.27	0.030	0.050	2
Ø P	3.54	3.73	0.139	0.147	
Q	2.60	3.00	0.102	0.118	
θ	90° to 93°		90° to 93°		

Notes

- (1) Dimensioning and tolerancing as per ASME Y14.5M-1994
- (2) Lead dimension and finish uncontrolled in L1
- (3) Dimension D, D1 and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Dimension b1, b3 and c1 apply to base metal only
- (5) Controlling dimension: inches
- (6) Thermal pad contour optional within dimensions E, H1, D2 and E1
- (7) Dimension E2 x H1 define a zone where stamping and singulation irregularities are allowed
- (8) Outline conforms to JEDEC TO-220, D2 (minimum) where dimensions are derived from the actual package outline



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