



May 2014

# FDD9409\_F085

## N-Channel PowerTrench<sup>®</sup> MOSFET

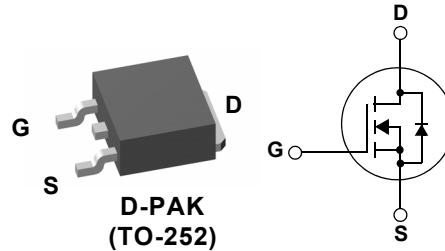
40 V, 90 A, 3.2 mΩ

### Features

- Typ  $R_{DS(on)}$  = 2.3mΩ at  $V_{GS} = 10V$ ,  $I_D = 80A$
- Typ  $Q_{g(tot)}$  = 42nC at  $V_{GS} = 10V$ ,  $I_D = 80A$
- UIS Capability
- RoHS Compliant
- Qualified to AEC Q101

### Applications

- Automotive Engine Control
- Powertrain Management
- Solenoid and Motor Drivers
- Electronic Steering
- Integrated Starter/Alternator
- Distributed Power Architectures and VRM
- Primary Switch for 12V Systems



For current package drawing, please refer to the Fairchild website at [www.fairchildsemi.com/packaging](http://www.fairchildsemi.com/packaging)

### MOSFET Maximum Ratings $T_J = 25^\circ C$ unless otherwise noted.

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-to-Source Voltage	40	V
$V_{GS}$	Gate-to-Source Voltage	±20	V
$I_D$	Drain Current - Continuous ( $V_{GS}=10$ ) (Note 1)	$T_C = 25^\circ C$	90
	Pulsed Drain Current	$T_C = 25^\circ C$	See Figure 4
$E_{AS}$	Single-Pulse Avalanche Energy (Note 2)	101	mJ
$P_D$	Power Dissipation	150	W
	Derate Above 25°C	1	W/°C
$T_J, T_{STG}$	Operating and Storage Temperature	-55 to + 175	°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient (Note 3)	52	°C/W

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD9409	FDD9409_F085	D-PAK(TO-252)	13"	12mm	2500 units

#### Notes:

- 1: Current is limited by bondwire configuration.
- 2: Starting  $T_J = 25^\circ C$ ,  $L = 0.1mH$ ,  $I_{AS} = 44A$ ,  $V_{DD} = 40V$  during inductor charging and  $V_{DD} = 0V$  during time in avalanche.
- 3:  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design. The maximum rating presented here is based on mounting on a 1 in<sup>2</sup> pad of 2oz copper.

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**Electrical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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**Off Characteristics**

$B_{V_{DSS}}$	Drain-to-Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	40	-	-	V
$I_{DSS}$	Drain-to-Source Leakage Current	$V_{DS} = 40\text{V}, T_J = 25^\circ\text{C}$	-	-	1	$\mu\text{A}$
		$V_{GS} = 0\text{V}, T_J = 175^\circ\text{C}(\text{Note } 4)$	-	-	1	$\text{mA}$
$I_{GSS}$	Gate-to-Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	$\text{nA}$

**On Characteristics**

$V_{GS(th)}$	Gate-to-Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2.0	3.2	4.0	V
$R_{DS(on)}$	Drain-to-Source On Resistance	$I_D = 80\text{A}, T_J = 25^\circ\text{C}$	-	2.3	3.2	$\text{m}\Omega$
		$V_{GS} = 10\text{V}, T_J = 175^\circ\text{C}(\text{Note } 4)$	-	4.1	5.7	$\text{m}\Omega$

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	-	3130	-	$\text{pF}$
$C_{oss}$	Output Capacitance		-	756	-	$\text{pF}$
$C_{riss}$	Reverse Transfer Capacitance		-	48	-	$\text{pF}$
$R_g$	Gate Resistance	$f = 1\text{MHz}$	-	2	-	$\Omega$
$Q_{g(ToT)}$	Total Gate Charge at 10V	$V_{GS} = 0 \text{ to } 10\text{V}$	-	42	46	$\text{nC}$
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0 \text{ to } 2\text{V}$				
$Q_{gs}$	Gate-to-Source Gate Charge					
$Q_{gd}$	Gate-to-Drain "Miller" Charge		-	7.7	-	$\text{nC}$

**Switching Characteristics**

$t_{on}$	Turn-On Time	$V_{DD} = 20\text{V}, I_D = 80\text{A}, V_{GS} = 10\text{V}, R_{GEN} = 6\Omega$	-	-	72	$\text{ns}$
$t_{d(on)}$	Turn-On Delay		-	23	-	$\text{ns}$
$t_r$	Rise Time		-	22	-	$\text{ns}$
$t_{d(off)}$	Turn-Off Delay		-	41	-	$\text{ns}$
$t_f$	Fall Time		-	15	-	$\text{ns}$
$t_{off}$	Turn-Off Time		-	-	76	$\text{ns}$

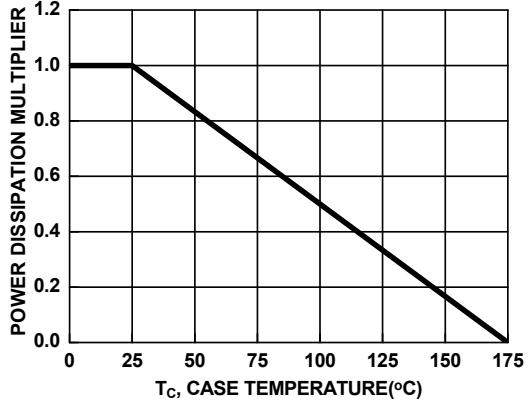
**Drain-Source Diode Characteristics**

$V_{SD}$	Source-to-Drain Diode Voltage	$I_{SD} = 80\text{A}, V_{GS} = 0\text{V}$	-	-	1.25	V
		$I_{SD} = 40\text{A}, V_{GS} = 0\text{V}$	-	-	1.2	V
$t_{rr}$	Reverse-Recovery Time	$I_F = 80\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	54	73	$\text{ns}$
$Q_{rr}$	Reverse-Recovery Charge	$V_{DD} = 32\text{V}$	-	42	61	$\text{nC}$

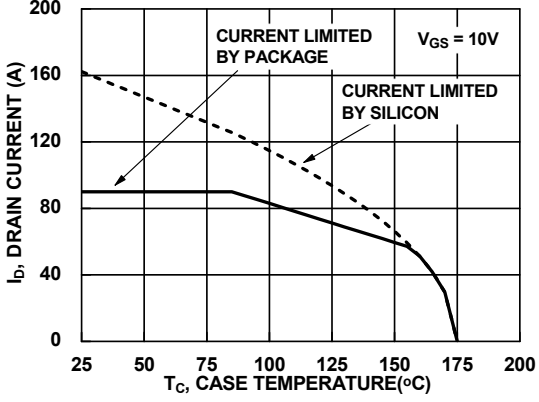
**Note:**

4: The maximum value is specified by design at  $T_J = 175^\circ\text{C}$ . Product is not tested to this condition in production.

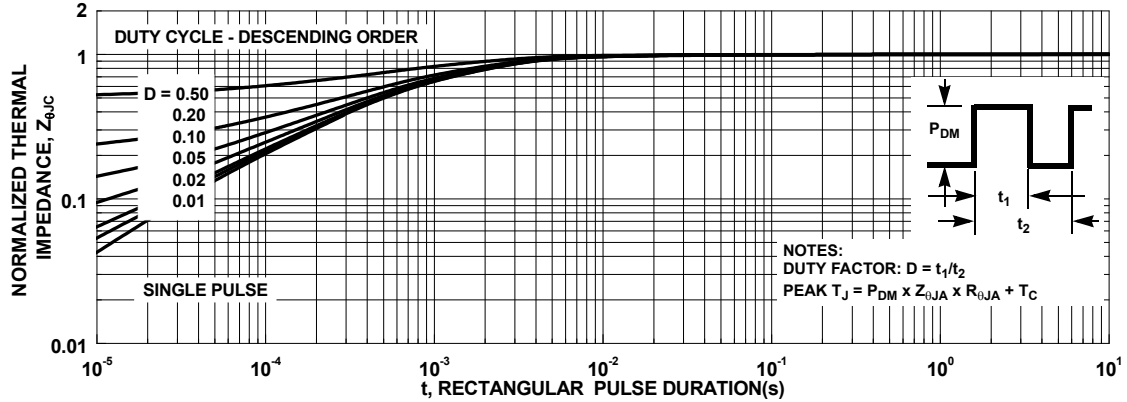
**Typical Characteristics**



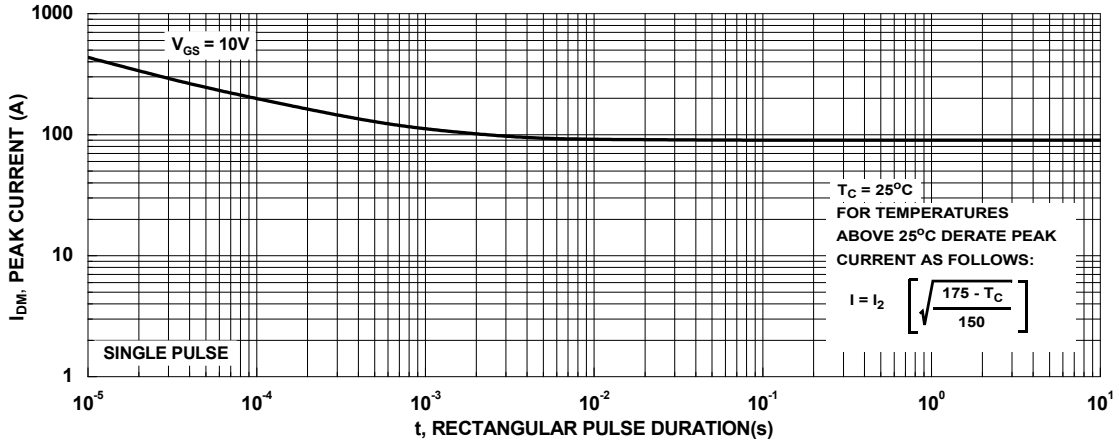
**Figure 1. Normalized Power Dissipation vs. Case Temperature**



**Figure 2. Maximum Continuous Drain Current vs. Case Temperature**



**Figure 3. Normalized Maximum Transient Thermal Impedance**



**Figure 4. Peak Current Capability**

## Typical Characteristics

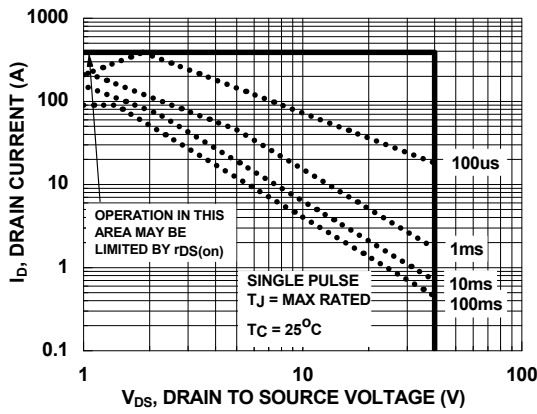
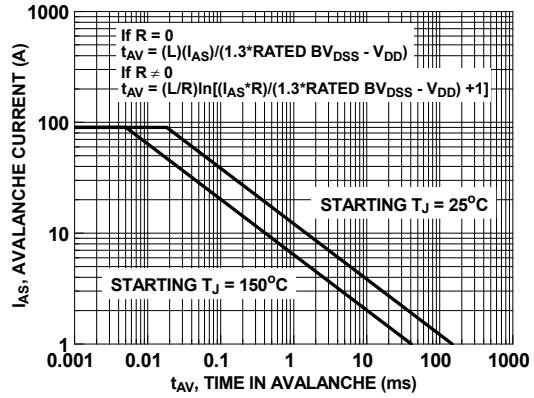


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

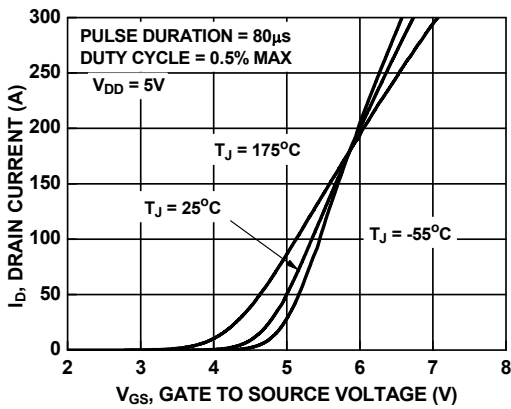


Figure 7. Transfer Characteristics

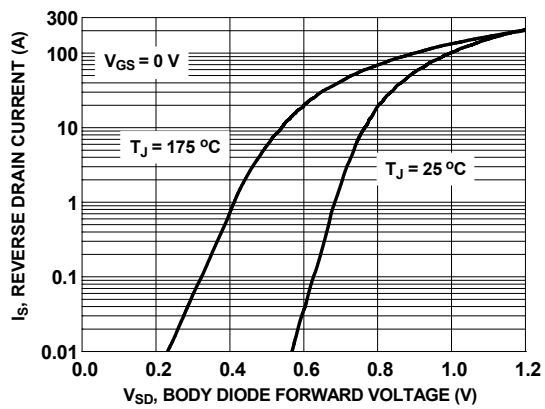


Figure 8. Forward Diode Characteristics

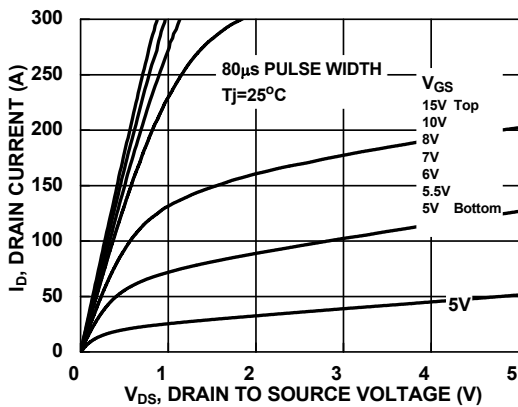


Figure 9. Saturation Characteristics

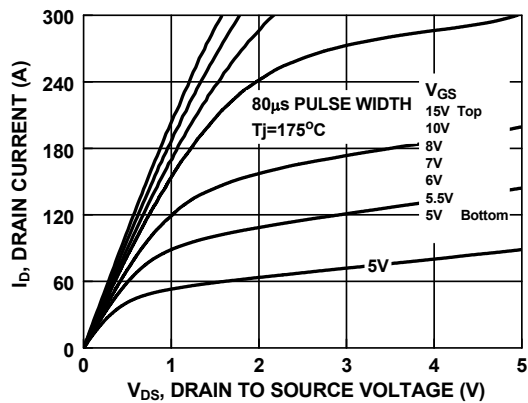


Figure 10. Saturation Characteristics

### Typical Characteristics

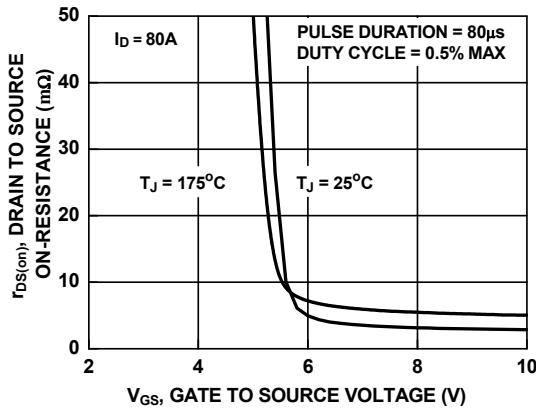


Figure 11.  $R_{DS(on)}$  vs. Gate Voltage

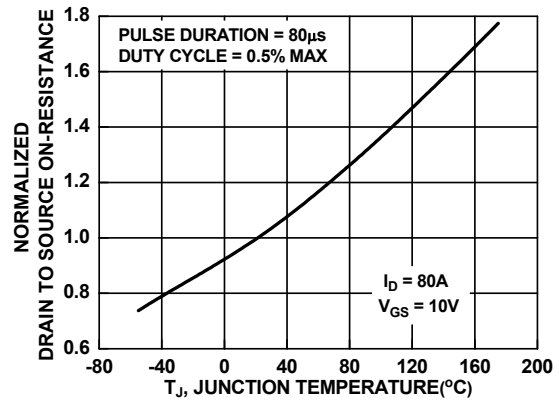


Figure 12. Normalized  $R_{DS(on)}$  vs. Junction Temperature

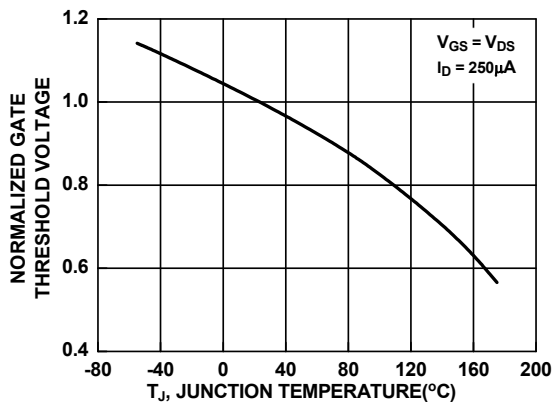


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

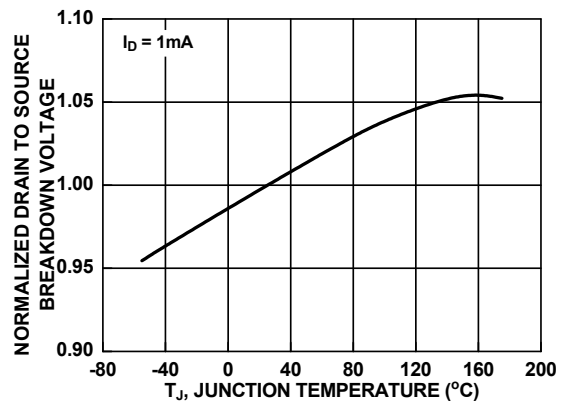


Figure 14. Normalized Drain-Source Breakdown Voltage vs. Junction Temperature

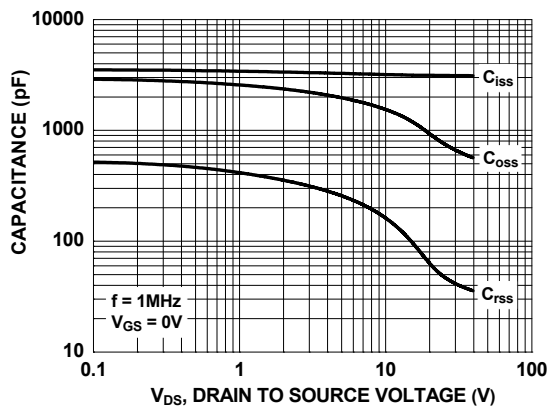


Figure 15. Capacitance vs. Drain-Source Voltage

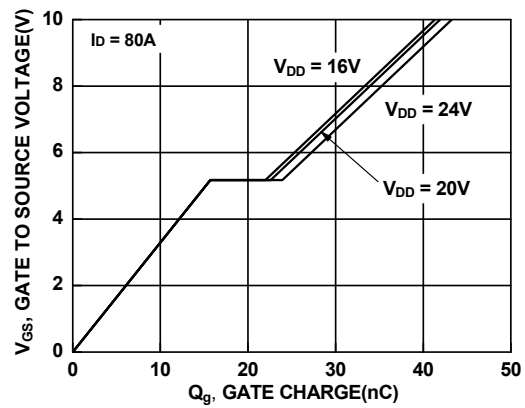







Figure 16. Gate Charge vs. Gate-Source Voltage



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