July 2014

FSA8039A
Audio Jack Interface Solution with Moisture Sensing

Features

- Detection:
  - Accessory Plug-In
  - Send / End Key Press
  - Prevents False Detection due to Moisture
- V_{DD}: 2.5 V to 4.5 V
- V_{IO}: 1.6 V to V_{DD}
- THD (MIC): 0.01% Typical
- 15 kV Air Gap ESD
- MIC Switch Removes Audio Jack “Pop” and “Click” Caused by MIC Bias

Applications

- Any Device with 3.5 mm and 2.5 mm Audio Jack
- Cellular Phones, Smart Phones, and Tablets
- MP3, GPS, and PMP

Description

The FSA8039A is a detection switch for an audio jack that employs a normally open detect pin. The FSA8039A works with 3-pole and 4-pole accessories. The FSA8039A features moisture sensing that prevents false detection of accessories in the audio jack. The integrated MIC switch allows a processor to configure attached accessories. The architecture is designed to allow common third-party headphones to be used for listening to music from mobile handsets, personal media players, and portable peripheral devices.

Related Resources

- FSA8039A Evaluation Board
- *For samples and questions, please contact: Analog.Switch@fairchildsemi.com*

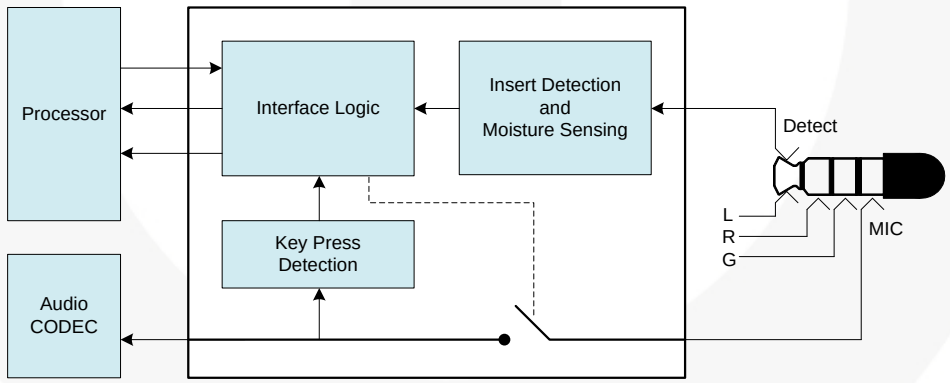


Figure 1. Block Diagram

Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package	Packing Method
FSA8039AUMSX	-40°C to 85°C	NF	10-Lead, UMLP, 1.4 mm x 1.8 mm, 0.4 mm Pitch	Tape & Reel

Typical Application Diagram

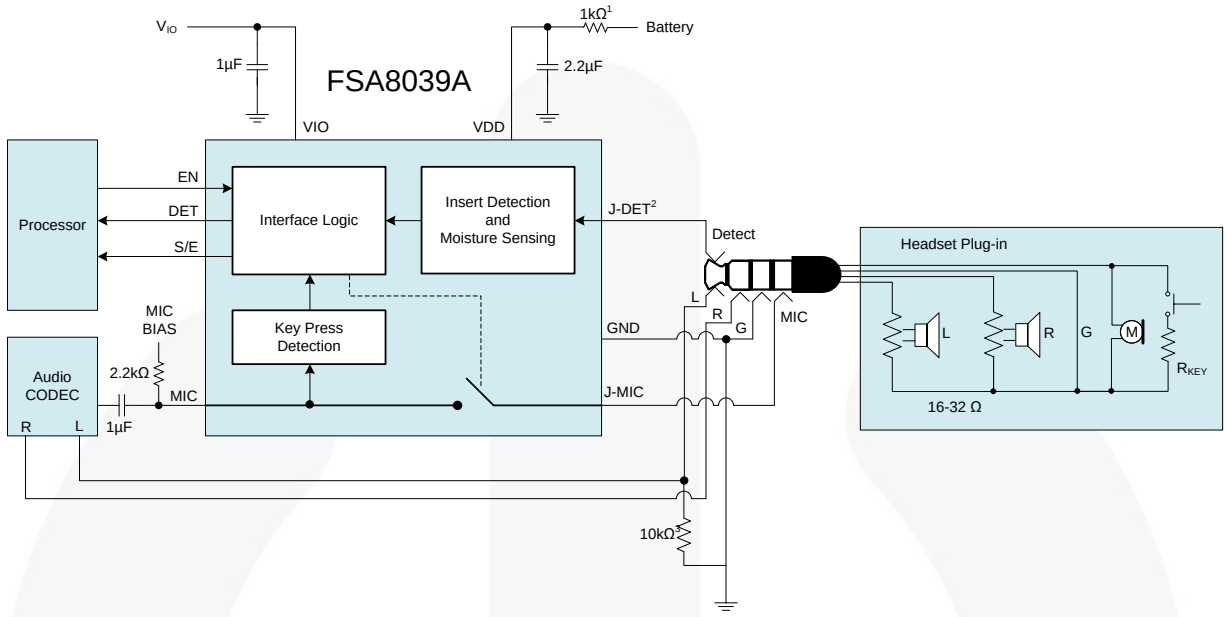


Figure 2. Typical Application

Notes:

1. A 1 kΩ resistor with a 2.2 µF capacitor is recommended for direct battery connection. This filter helps stabilize power rail events not associated with the FSA8039A. If power is supplied from a stable source, such as from a PMIC or LDO, a single 1 µF capacitor is recommended.
2. The J-DET is shorted to the left (L) audio channel when the headset or accessory plug is inserted into most audio jacks. Any external circuitry attached to the J-DET pin could affect audio performance in the 20-20 kHz range on the left channel.
3. The optional 10 kΩ resistor on the left channel is used to assist in detection of high-impedance accessories. This resistor has negligible impact on audio fidelity.

Pin Configuration

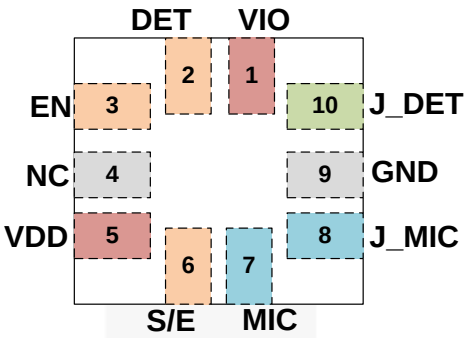


Figure 3. Pin Assignment (Through View)

Pin Definitions

Name	Pin #	Type	Description			
VIO	1	Power	Baseband or processor I/O supply voltage			
DET	2	Output	Indicates if audio accessory is plugged in (debounced output)	DET=V_{OL}, Accessory plugged in		
				DET=V_{OH}, Accessory unplugged		
EN	3	Input	Microphone switch control		No Plug	Plug inserted
				EN=V_{IL}	MIC switch open	Music Mode
				EN=V_{IH}	MIC switch open	MIC switch closed
NC	4	NC	No connect; connect to GND for improved solder stability			
VDD	5	Power	Supply voltage			
S/E	6	Output	Indicates when an accessory key has been pressed (debounced output)	S/E=V_{OL}, No Key Press		
				S/E=V_{OH}, Key Press		
MIC	7	I/O	Connection to the microphone pre-amplifier	EN=V_{IL}, Switch Open EN=V_{IH}, Switch Closed		
J_MIC	8	I/O	Connection from the audio jack mechanical plug microphone pin			
GND	9	Ground	Ground for both the audio jack and PCB			
J_DET	10	Input	Input from the audio jack mechanical plug insert/removal detection pin			

Application Information

Moisture Detection

Moisture in the audio jack can cause the phone to incorrectly route audio signals to the audio jack rather than the phone speaker or microphone. Users perceive this as a dropped call or muted phone. The FSA8039A protects against this type of false plug-insert notification.

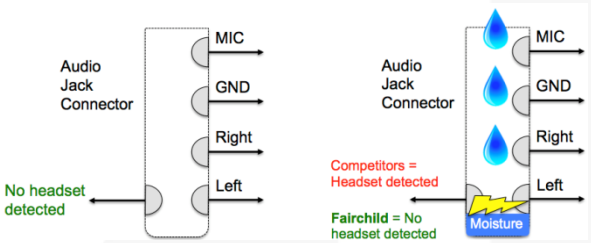


Figure 4. Moisture Impedance Detection

Music Mode

When a 4-pole headset is inserted into the audio jack and a music/listening application is used, the MIC bias is normally enabled for headset button press detection (i.e. mute, volume change, etc.). This consumes power due to a constant path from the MIC bias resistor and microphone in the headset to GND. Fairchild has developed a Music Mode to enable the MIC switch periodically to monitor for a pressed button. This results in a power savings for battery-sensitive devices, such as cell phones or MP3 players. The FSA8039A enters Music Mode when EN=LOW and a 4-pole headset is inserted. Music Mode reduces MIC bias current by approximately 90%.

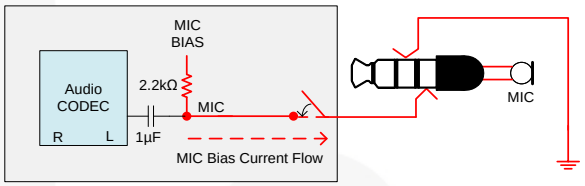
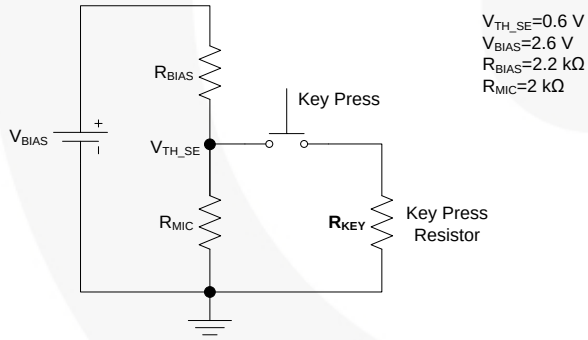


Figure 5. MIC Bias Leakage Path

Headset Key-Press Operation

The headset key-press comparator threshold is a function of the MIC bias voltage, MIC bias resistor, and the MIC impedance. All of these variables must be considered when calculating the key-press resistor value. Figure 6 is an example of how to calculate the key-press resistor value.



$$R_{KEY} \leq \frac{1}{\left(\frac{1}{V_{TH\_SE} / \frac{V_{BIAS}-V_{TH\_SE}}{R_{BIAS}}}\right) - \frac{1}{R_{MIC}}}$$

$$R_{KEY} \leq 980\ \Omega$$

Figure 6. Example Key-Press Resistor Calculations and Values

Design / Layout Best Practices

System-level Electrostatic Discharge (ESD) events often occur in the audio path of a mobile device, typically when inserting or removing an accessory from the audio jack. The audio path from the audio jack to the audio codec or microphone pre-amplifier is typically designed for relatively low frequencies (<100 kHz). An ESD event is a high-frequency event with fast edge rates (<100 ns/V). For this reason, the audio paths represent a high-frequency transmission line to the ESD signal.

Use the following PCB design and layout best practices when designing a system audio path.

Audio Path Layout Guidelines for ESD

For the MIC and ground signals between the audio jack and FSA8039A, decrease the spacing between these traces to increase the inductive coupling of the signals. In effect, this creates a low-frequency band pass filter that shunts ESD energy to ground before it reaches internal components. Where feasible, lay the MIC trace as a shielded stripline, as shown in Figure 7.

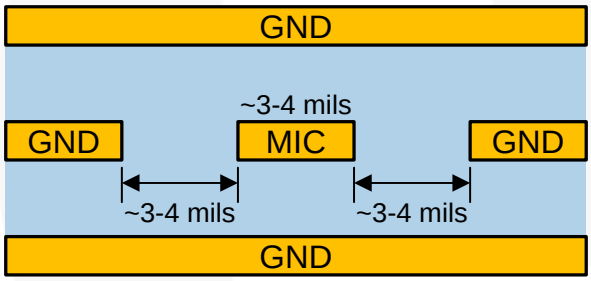


Figure 7. MIC PCB Trace as Shielded Stripline

Ground Layout Guidelines

Ground layout for audio path devices should consider high-frequency effects. During an ESD event, parasitic inductance and resistance in the ground path reduces its ability to shunt the fast transient energy. Use the following techniques to improve grounding effectiveness:

- Use “star” ground connections (not daisy-chain).
- Use ground vias to minimize ground path impedance and ground loops.
- Stitch ground traces to the ground plane at the device, where possible *(see Figure 8)*.
- Flood ground, where possible *(see Figure 8)*.
- Avoid ground “islands” or “peninsulas” if possible.
- If using a modular audio jack assembly that is not soldered to the main PCB, use a ground pad on the jack with an ohmic connection to battery ground.

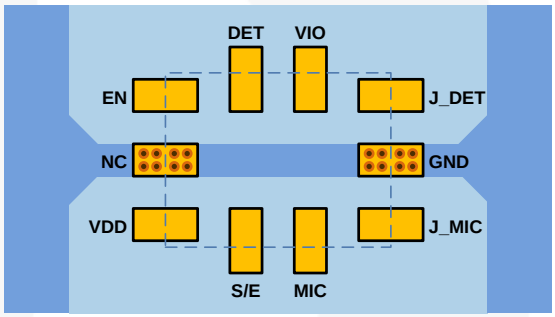


Figure 8. PCB Layout/Grounding

In addition to ESD robustness, these techniques can improve audio signal performance by reducing audio crosstalk and echo due to resistive voltage drops in the audio ground path.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{DD}, V_{IO}	Supply Voltage from Battery		-0.5	6.0	V
V_{SW}	Switch I/O Voltage (MIC, J_MIC)		-0.5	V_{DD}+0.5	V
V_{JD}	Input Voltage for J_DET Input		-1.5	V_{DD}+0.5	V
I_{IK}	Input Clamp Diode Current		-50		mA
I_{SW}	Switch I/O Current			50	mA
T_{STG}	Storage Temperature Range		-65	+150	°C
T_J	Maximum Junction Temperature			+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)			+260	°C
ESD	IEC 61000-4-2 System ESD	Air Gap	15		kV
		Contact	8		
	Human Body Model, ANSI/ESDA/JEDEC JS-001-2012	J_DET, J_MIC, V_{DD}, V_{IO}, GND	8		
		All Other Pins	2		
	Charged Device Model, JEDEC JESD22-C101	All Pins	2		

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Battery Supply Voltage	2.5	4.5	V
V_{IO}	Parallel I/O Supply Voltage	1.6	V_{DD}	V
T_A	Operating Temperature	-40	+85	ºC
J_DET_{Audiof}	Audio Frequency on J_DET Pin; V_{DD}=2.4 to 4.5 V; DET= V_{OL}	20	20000	Hz
V_{SW}	MIC Switch Input Voltage Range	0	V_{DD}	V
J_DET_{AudioV}	Audio Voltage on J_DET Pin	-1	1	V
J_DET_{RL}	Maximum Resistance on Accessory Left Channel for Valid Attach / Audio Accessory Plug Inserted		10	kΩ

DC Electrical Characteristics

All typical values are at T_A=25°C, C_{IN_VDD}=1.0 µF, and C_{IN_VIO}=0.1 µF unless otherwise specified.

Symbol	Parameter	V_{DD} (V)	Conditions	T_A = -40 to +85°C			Unit
				Min.	Typ.	Max.	
MIC Switch							
R_{ON}	MIC Switch On Resistance	3.8	I_{OUT}=30 mA, V_{IN}=2.2 V		0.4	2.0	Ω
$R_{FLAT(ON)}$	On Resistance Flatness	3.8	I_{OUT}=30 mA, V_{IN}=1.6 V to 2.8 V		0.30	1.50	
I_{OFF}	Power-Off Leakage Current on MIC Pin	0	MIC=4.3 V			1	µA
Key Press							
V_{TH_SE}	Key Detection Threshold	2.5 to 4.5	Detection Threshold	0.60			V
Parallel I/O (KP, INTB)							
V_{OH}	Output High Voltage		I_{OH}=-100 µA	0.8 × V_{IO}			V
V_{OL}	Output Low Voltage		I_{OL}=+100 µA			0.2 × V_{IO}	
I_{IN}	EN Input Leakage Current					1	µA
V_{IL}	Low-Level Input Voltage					0.3 × V_{IO}	V
V_{IH}	High-Level Input Voltage			0.7 × V_{IO}			V
Current							
$I_{DD-SLNA}$	Battery Supply Sleep Mode Current with No Accessory Attached and LDO Disabled	2.5 to 4.5	Static Current during Sleep Mode		1.5	3.0	µA
$I_{DD-SLWA}$	Battery Supply Sleep Mode Current with Accessory Attached	2.5 to 4.5	Active Current		20	30	µA

Note:

4. Refer to Figure 6 and R_{KEY} calculation.

AC Electrical Characteristics

All typical values are for T_A=25°C, C_{IN_VDD}=1.0 µF, and C_{IN_VIO}=0.1 µF unless otherwise specified.

Symbol	Parameter	V_{DD} (V)	Conditions	Typical	Unit
MIC Switch					
THD+N	Total Harmonic Distortion + Noise (Char)	3.8	R_T=600 Ω, f=20 Hz to 20 kHz, V_{MIC}=2.0 V_{DC} +0.5 V_{pp} Sine	0.01	%
OIRR	Off Isolation	3.8	f=20 Hz to 20 kHz, R_S=R_T=32 Ω, C_L=0 pF	-85	dB
Timing Characteristics					
t_{POLL}	ON Time of MIC Switch for Sensing SEND / END Key Press Oscillator Stable Time	2.5 to 4.5	DET=V_{OL}, EN=V_{IL}	1	ms
t_{WAIT}	Period of MIC Switching for Sensing SEND / END Key Press	2.5 to 4.5	DET=V_{OL}, EN=V_{IL}	10	ms
t_{DET_IN}	Debounce Time after J_DET Changes State from HIGH to LOW	2.5 to 4.5		70	ms
t_{KBK}	Debounce Time for Sensing SEND / END Key Press / Release	2.5 to 4.5		30	ms
t_{DET_REM}	Debounce Time from Changing J_DET State from LOW to HIGH to Detect Jack Removal	2.5 to 4.5		30	µs
Power					
PSRR	Power Supply Rejection Ratio	3.8	Power Supply Noise 300 mV_{PP}, f=217 Hz	-90	dB

10-Lead, Quad Ultrathin MLP (UMLP) Nominal Values

JEDEC Symbol	Description	Nominal Values (mm)
A	Overall Height	0.5
A1	Package Standoff	0.026
A3	Lead Thickness	0.152
b	Lead Width	0.2
L	Lead Length	0.4
e	Lead Pitch	0.4
D	Body Length (Y)	1.8
E	Body Width (X)	1.4

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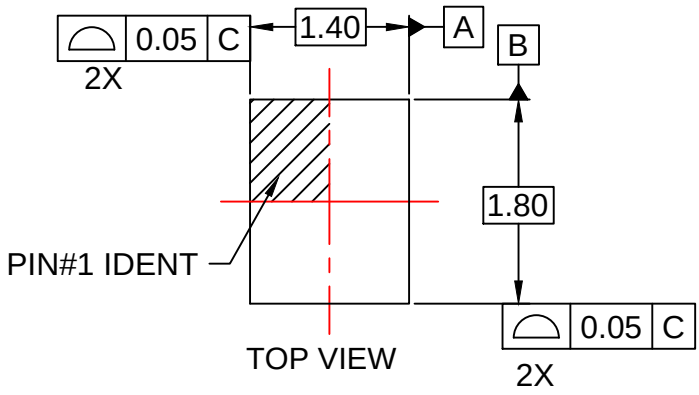

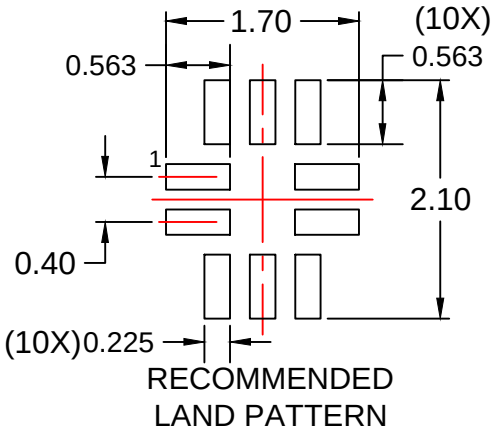

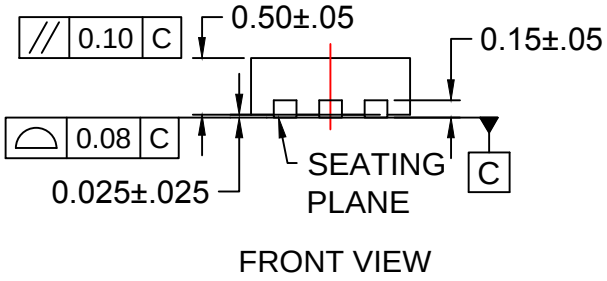

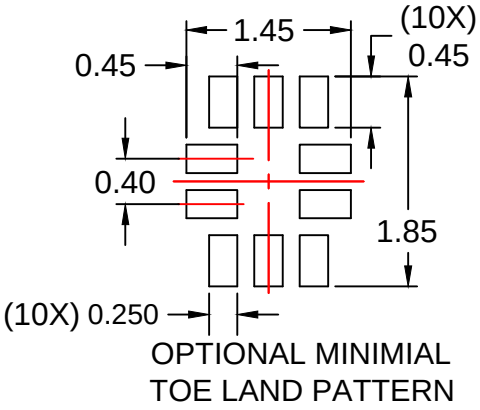

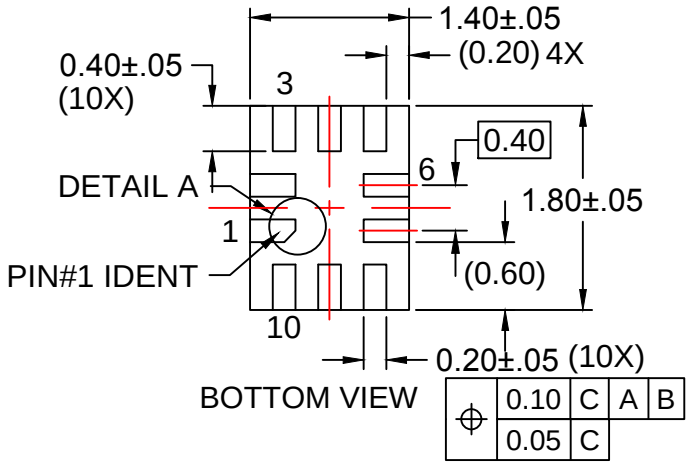

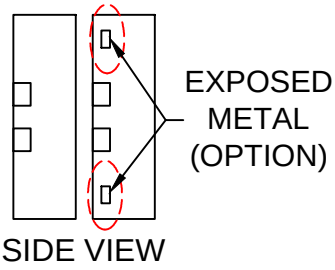

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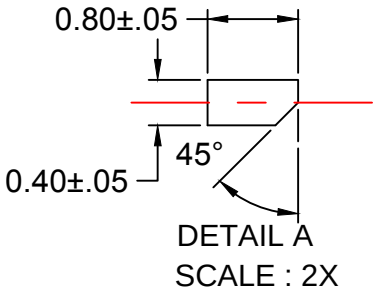

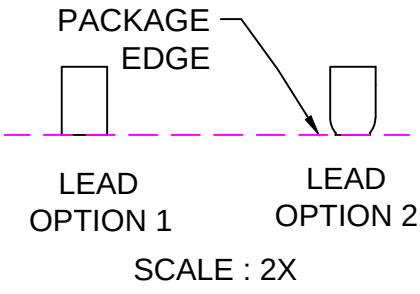

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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