

## Excellent Integrated System Limited

Stocking Distributor

Click to view price, real time Inventory, Delivery & Lifecycle Information:

[Texas Instruments](#)  
[TUSB1210BRHBRQ1](#)

For any questions, you can email us directly:

[sales@integrated-circuit.com](mailto:sales@integrated-circuit.com)



Product Folder



Sample &amp; Buy



Technical Documents



Tools &amp; Software



Support &amp; Community


**TEXAS  
INSTRUMENTS**
**TUSB1210-Q1**

SLLSEL4A – SEPTEMBER 2014 – REVISED OCTOBER 2014

## TUSB1210-Q1 Standalone USB Transceiver Chip Silicon

### 1 Features

- AEC-Q100 Qualified with:
  - Temperature Grade 3: –40°C to 85°C
  - HBM ESD Classification 1C
  - CDM ESD Classification C4B
- USB2.0 PHY Transceiver Chip, Designed to Interface with a USB Controller via a ULPI 12-pin Interface, Fully Compliant With:
  - *Universal Serial Bus Specification Rev. 2.0*
  - *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3*
  - *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*
- DP/DM Line External Component Compensation (Patent #US7965100 B1)
- Interfaces to Host, Peripheral and OTG Device Cores; Optimized for Portable Devices or System ASICs with Built-in USB OTG Device Core
- Complete USB OTG Physical Front-End that Supports Host Negotiation Protocol (HNP) and Session Request Protocol (SRP)
- ULPI Interface:
  - I/O Interface (1.8 V) Optimized for Non-Terminated 50 Ω Line Impedance
  - ULPI CLOCK Pin (60 MHz) Supports Both Input and Output Clock Configurations
  - Fully Programmable ULPI-Compliant Register Set
- Available in a 32-Pin Quad Flat No Lead [QFN (RHB)] Package

### 2 Applications

- Mobile Phones
- Tablet Devices
- Desktop Computers
- Portable Computers
- Video Game Consoles
- Portable Music Players

### 3 Description

The TUSB1210-Q1 is a USB2.0 transceiver chip, designed to interface with a USB controller via a ULPI interface. It supports all USB2.0 data rates (High-Speed 480 Mbps, Full-Speed 12 Mbps and Low-Speed 1.5 Mbps), and is compliant to both Host and Peripheral modes. It additionally supports a UART mode and legacy ULPI serial modes.

TUSB1210-Q1 also supports the OTG (Ver1.3) optional addendum to the USB 2.0 Specification, including Host Negotiation Protocol (HNP) and Session Request Protocol (SRP).

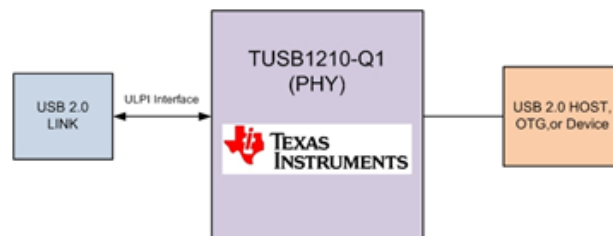
The DP/DM external component compensation in the transmitter compensates for variations in the series impedance in order to match with the data line impedance and the receiver input impedance, to limit data reflections, and thereby, improve eye diagrams.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TUSB1210-Q1	VQFN (32)	5.00 mm x 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

#### Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

## TUSB1210-Q1

SLLSEL4A – SEPTEMBER 2014 – REVISED OCTOBER 2014

[www.ti.com](http://www.ti.com)

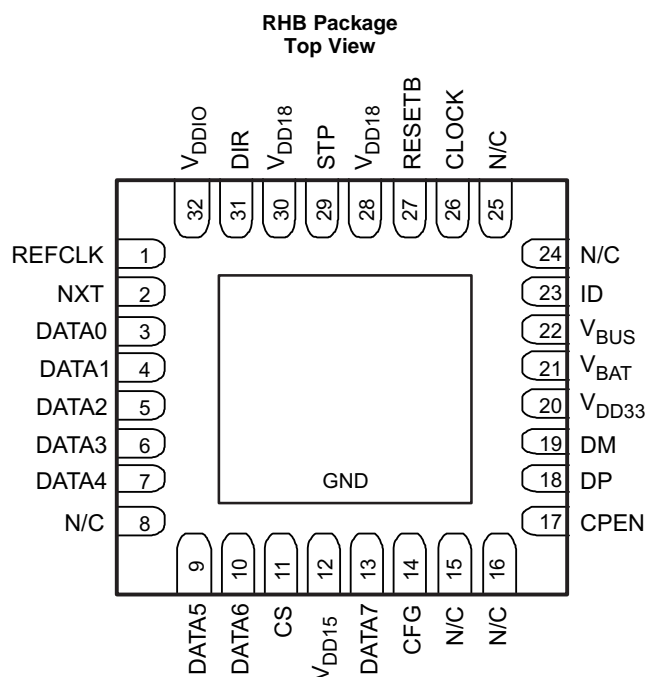
### Table of Contents

<b>1 Features</b> .....	<b>1</b>	7.4 Device Functional Modes.....	<b>18</b>
<b>2 Applications</b> .....	<b>1</b>	7.5 Register Map.....	<b>20</b>
<b>3 Description</b> .....	<b>1</b>	<b>8 Application and Implementation</b> .....	<b>49</b>
<b>4 Revision History</b> .....	<b>2</b>	8.1 Application Information.....	<b>49</b>
<b>5 Pin Configuration and Functions</b> .....	<b>3</b>	8.2 Typical Application.....	<b>49</b>
<b>6 Specifications</b> .....	<b>4</b>	8.3 External Components.....	<b>53</b>
6.1 Absolute Maximum Ratings.....	<b>4</b>	<b>9 Power Supply Recommendations</b> .....	<b>54</b>
6.2 Handling Ratings.....	<b>4</b>	9.1 TUSB1210 Power Supply.....	<b>54</b>
6.3 Recommended Operating Conditions.....	<b>5</b>	9.2 Ground.....	<b>54</b>
6.4 Thermal Information.....	<b>5</b>	9.3 Power Providers.....	<b>54</b>
6.5 Analog I/O Electrical Characteristics.....	<b>5</b>	9.4 Power Modules.....	<b>54</b>
6.6 Digital I/O Electrical Characteristics.....	<b>5</b>	9.5 Power Consumption.....	<b>55</b>
6.7 Digital IO Pins (Non-ULPI).....	<b>5</b>	<b>10 Layout</b> .....	<b>56</b>
6.8 PHY Electrical Characteristics.....	<b>6</b>	10.1 Layout Guidelines.....	<b>56</b>
6.9 Pullup/Pulldown Resistors.....	<b>8</b>	10.2 Layout Example.....	<b>56</b>
6.10 OTG Electrical Characteristics.....	<b>9</b>	<b>11 Device and Documentation Support</b> .....	<b>57</b>
6.11 Power Characteristics.....	<b>10</b>	11.1 Documentation Support.....	<b>57</b>
6.12 Switching Characteristics.....	<b>10</b>	11.2 Community Resources.....	<b>57</b>
6.13 Timing Requirements.....	<b>11</b>	11.3 Trademarks.....	<b>57</b>
6.14 Typical Characteristics.....	<b>13</b>	11.4 Electrostatic Discharge Caution.....	<b>57</b>
<b>7 Detailed Description</b> .....	<b>14</b>	11.5 Glossary.....	<b>57</b>
7.1 Overview.....	<b>14</b>	<b>12 Mechanical, Packaging, and Orderable Information</b> .....	<b>58</b>
7.2 Functional Block Diagram.....	<b>14</b>	12.1 Via Channel.....	<b>58</b>
7.3 Feature Description.....	<b>15</b>	12.2 Packaging Information.....	<b>58</b>

## 4 Revision History

Changes from Original (September 2014) to Revision A	Page
• Changed the Features list.....	<b>1</b>
• Deleted 5 paragraphs from the Description following: "TUSB1210-Q1 also supports the OTG (Ver1.3)..".	<b>1</b>
• Changed the <a href="#">Diagram</a> image.....	<b>1</b>
• Added $V_{IL}$ and $V_{IH}$ to the <a href="#">Recommended Operating Conditions</a> table.....	<b>5</b>
• Changed the <a href="#">Thermal Information</a> table.....	<b>5</b>
• Changed the <a href="#">Digital I/O Electrical Characteristics</a> table.....	<b>5</b>
• Digital IO Electrical Characteristics sections to the <a href="#">Switching Characteristics</a> .....	<b>10</b>
• Added the Typical Characteristics section.....	<b>13</b>
• Added 5 new paragraphs to the Overview section.....	<b>14</b>

## 5 Pin Configuration and Functions



### Pin Functions

PIN NAME	NO.	A/D	TYPE	LEVEL	DESCRIPTION
CFG	14	D	I	V <sub>DDIO</sub>	REFCLK clock frequency configuration pin. Two frequencies are supported: 19.2 MHz when 0, or 26 MHz when 1.
CLOCK	26	D	O	V <sub>DDIO</sub>	ULPI 60 MHz clock on which ULPI data is synchronized. Two modes are possible: Input Mode: CLOCK defaults as an input. Output Mode: When an input clock is detected on REFCLK pin (after 4 rising edges) then CLOCK will change to an output.
CPEN	17	D	O	V <sub>DD33</sub>	CMOS active-high digital output control of external 5V VBUS supply
CS	11	D	I	V <sub>DDIO</sub>	Active-high chip select pin. When low the IC is in power down and ULPI bus is tri-stated. When high normal operation. Tie to V <sub>DDIO</sub> if unused.
DATA0	3	D	I/O	V <sub>DDIO</sub>	ULPI DATA input/output signal 0 synchronized to CLOCK
DATA1	4	D	I/O	V <sub>DDIO</sub>	ULPI DATA input/output signal 1 synchronized to CLOCK
DATA2	5	D	I/O	V <sub>DDIO</sub>	ULPI DATA input/output signal 2 synchronized to CLOCK
DATA3	6	D	I/O	V <sub>DDIO</sub>	ULPI DATA input/output signal 3 synchronized to CLOCK
DATA4	7	D	I/O	V <sub>DDIO</sub>	ULPI DATA input/output signal 4 synchronized to CLOCK
DATA5	9	D	I/O	V <sub>DDIO</sub>	ULPI DATA input/output signal 5 synchronized to CLOCK
DATA6	10	D	I/O	V <sub>DDIO</sub>	ULPI DATA input/output signal 6 synchronized to CLOCK
DATA7	13	D	I/O	V <sub>DDIO</sub>	ULPI DATA input/output signal 7 synchronized to CLOCK
DIR	31	D	O	V <sub>DDIO</sub>	ULPI DIR output signal
DM	19	A	I/O	V <sub>DD33</sub>	DM pin of the USB connector
DP	18	A	I/O	V <sub>DD33</sub>	DP pin of the USB connector
ID	23	A	I/O	V <sub>DD33</sub>	Identification (ID) pin of the USB connector
N/C	8	–	–	V <sub>DDIO</sub>	No connect
N/C	15,16, 24, 24	–	–	–	No connect
NXT	2	D	O	V <sub>DDIO</sub>	ULPI NXT output signal

## TUSB1210-Q1

SLLSL4A – SEPTEMBER 2014 – REVISED OCTOBER 2014

www.ti.com

### Pin Functions (continued)

PIN NAME	NO.	A/D	TYPE	LEVEL	DESCRIPTION
REFCLK	1	A	I	3.3 V	V <sub>DD33</sub> Reference clock input (square-wave only). Tie to GND when pin 26 (CLOCK) is required to be Input mode. Connect to square-wave reference clock of amplitude in the range of 3 V to 3.6 V when Pin 26 (CLOCK) is required to be Output mode. See pin 14 (CFG) description for REFCLK input frequency settings.
RESETB	27	D	I	V <sub>DDIO</sub>	When low, all digital logic (except 32 kHz logic required for power up sequencing) including registers are reset to their default values, and ULPI bus is tri-stated. When high, normal USB operation.
STP	29	D	I	V <sub>DDIO</sub>	ULPI STP input signal
V <sub>BAT</sub>	21	A	power	V <sub>BAT</sub>	Input supply voltage or battery source
V <sub>BUS</sub>	22	A	power	V <sub>BUS</sub>	V <sub>BUS</sub> pin of the USB connector
VDD15	12	A	power		1.5-V internal LDO output. Connect to external filtering capacitor.
V <sub>DD18</sub>	28, 30	A	power	V <sub>DD18</sub>	External 1.8-V supply input. Connect to external filtering capacitor.
V <sub>DD33</sub>	20	A	power	V <sub>DD33</sub>	3.3-V internal LDO output. Connect to external filtering capacitor.
V <sub>DDIO</sub>	32	A	I	V <sub>DDIO</sub>	External 1.8V supply input for digital I/Os. Connect to external filtering capacitor.
GND	Thermal Pad	A	power	--	Reference Ground

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Main battery supply voltage <sup>(2)</sup>		0	5	V
	Voltage on any input <sup>(3)</sup>	Where supply represents the voltage applied to the power supply pin associated with the input	-0.3	1 × V <sub>CC</sub> + 0.3	V
	V <sub>BUS</sub> input		-2	20	V
	ID, DP, DM inputs	Stress condition specified 24h	-0.3	5.25	V
V <sub>DDIO</sub>	IO supply voltage	Continuous	-0.3	1.98	V
T <sub>A</sub>	Ambient temperature range		-40	85	°C
T <sub>J</sub>	Junction temperature range		-40	150	°C
	Ambient temperature for parametric compliance	Parametric compliance	-14	125	°C
		With max 125°C as junction temperature	-40	85	°C
	DP, DM, ID high voltage short circuit	DP, DM or ID pins short circuited to V <sub>BUS</sub> supply, in any mode of TUSB1210-Q1 operation, continuously for 24 hours	0	5.25	V

- Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The product will have negligible reliability impact if voltage spikes of 5.5 V occur for a total (cumulative over lifetime) duration of 5 milliseconds.
- Except V<sub>BAT</sub> input, V<sub>BUS</sub>, ID, DP, and DM pads

### 6.2 Handling Ratings

			MIN	MAX	UNIT
T <sub>stg</sub>	Storage temperature range		-65	150	°C
V <sub>ESD</sub>	Electrostatic discharge (ESD) performance:	Human body model (HBM), per AEC Q100-002 Classification Level H1C, all pins <sup>(1)</sup>	1500	1500	V
		Charged device model (CDM), per AEC Q100-011 Classification Level C4B	-750	750	
		Corner pins	-500	500	

- AEC Q100-002 indicates HBM stressing is done in accordance with ANSI/ESDA/JEDEC JS-001 specifications.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V <sub>BAT</sub>	Battery supply voltage		2.7	3.6	4.8	V
	Battery supply voltage for USB 2.0 compliancy (USB 2.0 certification)	When V <sub>DD33</sub> is supplied internally	3.15			V
		When V <sub>DD33</sub> is shorted to V <sub>BAT</sub> externally	3.05			
V <sub>DDIO</sub>	Digital IO pin supply		1.71		1.98	V
V <sub>IL</sub>	Low-level input voltage	CLOCK, STP, DIR, NXT, DATA0 to DATA7			0.35 x V <sub>DDIO</sub>	V
V <sub>IH</sub>	High-level output voltage	CLOCK, STP, DIR, NXT, DATA0 to DATA7	0.65 x V <sub>DDIO</sub>			V
T <sub>A</sub>	Ambient temperature range		–40		85	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		RHB	UNIT
		(16 Pins)	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	34.72	°C/W
R <sub>θJC(top)</sub>	Junction-to-case(top) thermal resistance	37.3	
R <sub>θJB</sub>	Junction-to-board thermal resistance	10.3	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.5	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	10.5	
R <sub>θJC(bottom)</sub>	Junction-to-case(bottom) thermal resistance	3.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

### 6.5 Analog I/O Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
<b>CPEN Output Pin</b>					
V <sub>OL</sub>	CPEN low-level output voltage	I <sub>OL</sub> = 3 mA		0.3	V
V <sub>OH</sub>	CPEN high-level output voltage	I <sub>OH</sub> = –3 mA	V <sub>DD33</sub> – 0.3		V

### 6.6 Digital I/O Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLOCK						
V <sub>OL</sub>	Low-level output voltage	Frequency = 60 MHz, Load = 10 pF	0.45			V
V <sub>OH</sub>	High-level output voltage		V <sub>DDIO</sub> - 0.45			V
STP, DIR, NXT, DATA0 to DATA7						
V <sub>OL</sub>	Low-level output voltage	Frequency = 30 MHz, Load = 10 pF	0.45			
V <sub>OH</sub>	High-level output voltage		V <sub>DDIO</sub> - 0.45			

### 6.7 Digital IO Pins (Non-ULPI)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>CS, CFG, RESETB Input Pins</b>					
V <sub>IL</sub>	Maximum low-level input voltage		0.35 x V <sub>DDIO</sub>		V
V <sub>IH</sub>	Minimum high-level input voltage	0.65 x V <sub>DDIO</sub>			V
<b>RESETB Input Pin Timing Spec</b>					
t <sub>w(POR)</sub>	Internal power-on reset pulse width	0.2			μs

## TUSB1210-Q1

SLLSEL4A – SEPTEMBER 2014 – REVISED OCTOBER 2014

www.ti.com

### Digital IO Pins (Non-ULPI) (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{w(RES\overline{E}T)}$ External RESETB pulse width	Applied to external RESETB pin when CLOCK is toggling.	8			CLOCK cycles

### 6.8 PHY Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	COMMENTS	MIN	TYP	MAX	UNIT
<b>LS/FS Single-Ended Receivers</b>					
SK <sub>WVP_VM</sub>	Skew between VP and VM	–2	0	2	ns
V <sub>SE_HYS</sub>	Single-ended hysteresis	50			mV
V <sub>IH</sub>	High (driven)	2			V
V <sub>IL</sub>	Low			0.8	V
V <sub>TH</sub>	Switching threshold	0.8		2	V
<b>LS/FS Differential Receiver</b>					
V <sub>DI</sub>	Differential input sensitivity	Ref. USB2.0	200		mV
V <sub>CM</sub>	Differential Common mode range	Ref. USB2.0	0.8	2.5	V
<b>LS Transmitter</b>					
V <sub>OL</sub>	Low	Ref. USB2.0	0	300	mV
V <sub>OH</sub>	High (driven)	Ref. USB2.0	2.8	3.6	V
V <sub>CRS</sub>	Output signal crossover voltage	Ref. USB2.0, covered by eye diagram	1.3	2	V
t <sub>r</sub>	Rise time	Ref. USB2.0, covered by eye diagram	75	300	ns
t <sub>f</sub>	Fall time		75	300	ns
t <sub>FRFM</sub>	Differential rise and fall time matching		80%	125%	
t <sub>FDRATE</sub>	Low-speed data rate	Ref. USB2.0, covered by eye diagram	1.4775	1.5225	Mb/s
t <sub>DJ1</sub>	Source jitter total (including frequency tolerance)	To next transition	–25	25	ns
t <sub>DJ2</sub>		For paired transitions	–10	10	
t <sub>FEOPT</sub>	Source SE0 interval of EOP	Ref. USB2.0, covered by eye diagram	1.25	1.5	μs
	Downstream eye diagram	Ref. USB2.0, covered by eye diagram			
V <sub>CM</sub>	Differential common mode range	Ref. USB2.0	0.8	2.5	V
<b>FS Transmitter</b>					
V <sub>OL</sub>	Low	Ref. USB2.0	0	300	mV
V <sub>OH</sub>	High (driven)	Ref. USB2.0	2.8	3.6	V
V <sub>CRS</sub>	Output signal crossover voltage	Ref. USB2.0, covered by eye diagram	1.3	2	V
t <sub>FR</sub>	Rise time	Ref. USB2.0	4	20	ns
t <sub>FF</sub>	Fall time	Ref. USB2.0	4	20	ns
t <sub>FRFM</sub>	Differential rise and fall time matching	Ref. USB2.0, covered by eye diagram	90%	111.11%	
Z <sub>DRV</sub>	Driver output resistance	Ref. USB2.0	28	44	Ω
T <sub>FDRATE</sub>	Full-speed data rate	Ref. USB2.0, covered by eye diagram	11.97	12.03	Mb/s
t <sub>DJ1</sub>	Source jitter total (including frequency tolerance)	To next transition	–2	2	ns
t <sub>DJ2</sub>		For paired transitions	–1	1	
T <sub>FEOPT</sub>	Source SE0 interval of EOP	Ref. USB2.0, covered by eye diagram	160	175	ns
	Downstream eye diagram	Ref. USB2.0, covered by eye diagram			

## PHY Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
	Upstream eye diagram					
<b>HS Differential Receiver</b>						
VHSSQ	High-speed squelch detection threshold (differential signal amplitude)	Ref. USB2.0	100		150	mV
VHSDSC	High-speed disconnect detection threshold (differential signal amplitude)	Ref. USB2.0	525		625	mV
	High-speed differential input signaling levels	Ref. USB2.0, specified by eye pattern templates				mV
VHSCM	High-speed data signaling common mode voltage range (guidelines for receiver)	Ref. USB2.0	–50		500	mV
	Receiver jitter tolerance	Ref. USB2.0, specified by eye pattern templates			150	ps
<b>HS Transmitter</b>						
V <sub>HSOI</sub>	High-speed idle level	Ref. USB2.0	–10		10	mV
V <sub>HSOH</sub>	High-speed data signaling high	Ref. USB2.0	360		440	mV
V <sub>HSOL</sub>	High-speed data signaling low	Ref. USB2.0	–10		10	mV
VCHIRPJ	Chirp J level (differential voltage)	Ref. USB2.0	700		1100	mV
VCHIRPK	Chirp K level (differential voltage)	Ref. USB2.0	–900		–500	mV
t <sub>r</sub>	Rise Time (10% - 90%)	Ref. USB2.0, covered by eye diagram	500			ps
t <sub>f</sub>	Fall time (10% - 90%)	Ref. USB2.0, covered by eye diagram	500			ps
ZHSDRV	Driver output resistance (which also serves as high-speed termination)	Ref. USB2.0	40.5		49.5	Ω
THSDRAT	High-speed data range	Ref. USB2.0, covered by eye diagram	479.76		480.24	Mb/s
	Data source jitter	Ref. USB2.0, covered by eye diagram				
	Downstream eye diagram	Ref. USB2.0, covered by eye diagram				
	Upstream eye diagram	Ref. USB2.0, covered by eye diagram				
<b>CEA-2011/UART Transceiver</b>						
	UART Transmitter CEA-2011					
t <sub>PH_UART_EDGE</sub>	Phone UART edge rates	DP_PULLDOWN asserted			1	Ms
V <sub>OH_SER</sub>	Serial interface output high	ISOURCE = 4 mA	2.4	3.3	3.6	V
V <sub>OL_SER</sub>	Serial interface output low	ISINK = –4 mA	0	0.1	0.4	V
	UART Receiver CEA-2011					
V <sub>IH_SER</sub>	Serial interface input high	DP_PULLDOWN asserted	2			V
V <sub>IL_SER</sub>	Serial interface input low	DP_PULLDOWN asserted			0.8	V
V <sub>TH</sub>	Switching threshold		0.8		2	V



## TUSB1210-Q1

SLLSEL4A – SEPTEMBER 2014 – REVISED OCTOBER 2014

[www.ti.com](http://www.ti.com)

### 6.9 Pullup/Pulldown Resistors

over operating free-air temperature range (unless otherwise noted)

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
RPUI	Bus pullup resistor on upstream port (idle bus)	Bus idle	0.9	1.1	1.575	kΩ
RPUA	Bus pullup resistor on upstream port (receiving)	Bus driven/driver's outputs unloaded	1.425	2.2	3.09	
VIHZ	High (floating)	Pullups/pulldowns on both DP and DM lines	2.7		3.6	V
VPH_DP_UP	Phone D+ pullup voltage	Driver's outputs unloaded	3	3.3	3.6	V
	Pulldown resistors					
RPH_DP_DWN	Phone D+/- pulldown	Driver's outputs unloaded	14.25	18	24.8	kΩ
RPH_DM_DWN						
VIHZ	High (floating)	Pullups/pulldowns on both DP and DM lines	2.7		3.6	V
	D+/- Data line					
CINUB	Upstream facing port	[1.0]		22	75	pF
VOTG_DATA_LKG	On-the-go device leakage	[2]			0.342	V
ZINP	Input impedance exclusive of pullup/pulldown	Driver's outputs unloaded	300			kΩ

## 6.10 OTG Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		COMMENTS		MIN	TYP	MAX	UNIT
OTG V <sub>BUS</sub> Electrical							
V <sub>BUS</sub> Comparators							
VA_SESS_VLD	A-device session valid			0.8	1.4	2.0	V
VA_VBUS_VLD	A-device V <sub>BUS</sub> valid			4.4	4.5	4.625	V
VB_SESS_END	B-device session end			0.2	0.5	0.8	V
VB_SESS_VLD	B-device session valid			2.1	2.4	2.7	V
V <sub>BUS</sub> Line							
RA_BUS_IN	A-device V <sub>BUS</sub> input impedance to ground	SRP (V <sub>BUS</sub> pulsing) capable A-device not driving V <sub>BUS</sub>		40	70	100	kΩ
RB_SRP_DWN	B-device V <sub>BUS</sub> SRP pulldown	5.25 V / 8 mA, Pullup voltage = 3 V		0.656	10		kΩ
RB_SRP_UP	B-device V <sub>BUS</sub> SRP pullup	(5.25 V – 3 V) / 8 mA, Pullup voltage = 3 V		0.281	1	2	kΩ
t <sub>RISE_SRP_UP_MAX</sub>	B-device V <sub>BUS</sub> SRP rise time maximum for OTG-A communication	0 to 2.1 V with < 13 μF load	RV <sub>BUS</sub> = 0 Ω and R1KSERIES = '0'	31.4			ms
			RV <sub>BUS</sub> = 1000 Ω ±10% and R1KSERIES = '1'	57.8			
			RV <sub>BUS</sub> = 1200 Ω ±10% and R1KSERIES = '1'	64			
			RV <sub>BUS</sub> = 1800 Ω ±10% and R1KSERIES = '1'	85.4			
t <sub>RISE_SRP_UP_MIN</sub>	B-device V <sub>BUS</sub> SRP rise time minimum for standard host connection	0.8 to 2 V with > 97 μF load	RV <sub>BUS</sub> = 0 Ω and R1KSERIES = '0'	46.2			ms
			RV <sub>BUS</sub> = 1000 Ω ±10% and R1KSERIES = '1'	96			
			RV <sub>BUS</sub> = 1200 Ω ±10% and R1KSERIES = '1'	100			
			RV <sub>BUS</sub> = 1800 Ω ±10% and R1KSERIES = '1'	100			

Table 1. OTG ID Electrical

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
ID Comparators — ID External Resistors Specifications						
R_ID_GND	ID ground comparator	ID_GND interrupt	12	20	28	kΩ
R_ID_FLOAT	ID Float comparator	ID_FLOAT interrupt	200		500	kΩ
	ID Line					
R_PH_ID_UP	Phone ID pullup to VPH_ID_UP	ID unloaded (V_RUSB)	70	90	286	kΩ
V_PH_ID_UP	Phone ID pullup voltage	Connected to V_RUSB	2.5		3.2	V
	ID line maximum voltage				5.25	V

## TUSB1210-Q1

SLLSEL4A – SEPTEMBER 2014 – REVISED OCTOBER 2014

www.ti.com

### 6.11 Power Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
V <sub>DD33</sub> Internal LDO Regulator Characteristics								
V <sub>INVDD33</sub>	Input voltage	V <sub>BAT</sub> USB		V <sub>VDD33</sub> typ + 0.2	3.6	4.5	V	
V <sub>VDD33</sub>	Output voltage	ON mode,	VUSB3V3_VSEL = '000	2.4	2.5	2.6	V	
			VUSB3V3_VSEL = '001	2.65	2.75	2.85		
			VUSB3V3_VSEL = '010	2.9	3.0	3.1		
			VUSB3V3_VSEL = '011 (default)	3.0	3.1	3.2		
			VUSB3V3_VSEL = '100	3.1	3.2	3.3		
			VUSB3V3_VSEL = '101	3.2	3.3	3.4		
			VUSB3V3_VSEL = '110	3.3	3.4	3.5		
			VUSB3V3_VSEL = '111	3.4	3.5	3.6		
I <sub>VDD33</sub>	Rated output current	V <sub>BAT</sub> USB	Active mode				15	mA
			Suspend/reset mode				1	
V <sub>DD15</sub> Internal LDO Regulator Characteristics								
V <sub>IN VDD15</sub>	Input voltage	On mode, V <sub>IN VDD15</sub> = V <sub>BAT</sub>		2.7	3.6	4.5	V	
V <sub>VDD15</sub>	Output voltage	V <sub>INVDD15</sub> min – V <sub>INVDD15</sub> max		1.45	1.56	1.65	V	
I <sub>VDD15</sub>	Rated output current	On mode				30	mA	

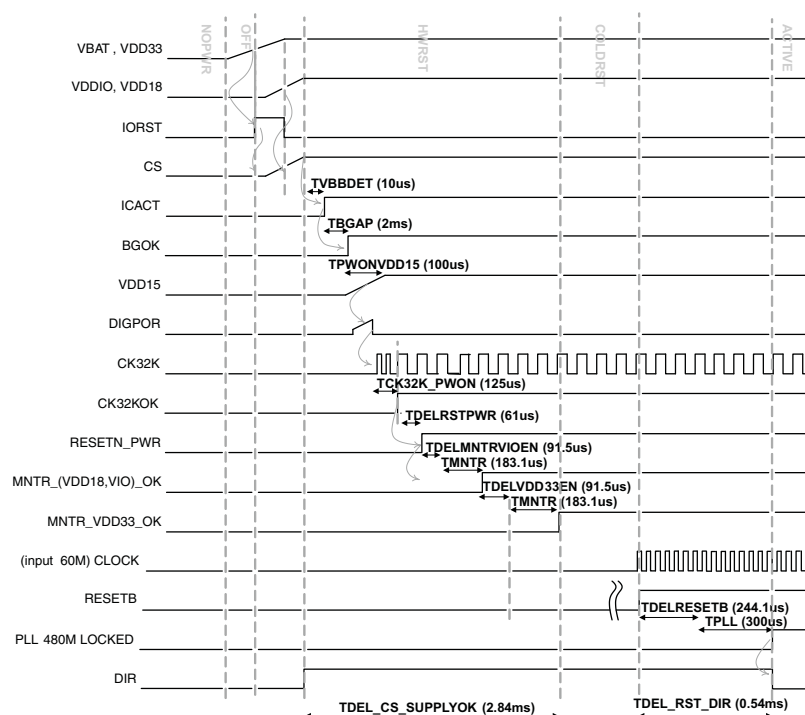
### 6.12 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics: Clock Input						
	Clock input duty cycle		40		60%	
f <sub>CLK</sub>	Clock nominal frequency			60		MHz
	Clock input rise/fall time	In % of clock period t <sub>CLK</sub> ( = 1/f <sub>CLK</sub> )			10%	
	Clock input frequency accuracy				250	ppm
	Clock input integrated jitter				600	ps rms
Electrical Characteristics: REFCLK						
	REFCLK input duty cycle		40		60%	
f <sub>REFCLK</sub>	REFCLK nominal frequency	When CFG pin is tied to GND		19.2		MHz
		When CFG pin is tied to V <sub>DDIO</sub>		26		
	REFCLK input rise/fall time	In % of clock period t <sub>REFCLK</sub> ( = 1/f <sub>REFCLK</sub> )			20%	
	REFCLK input frequency accuracy				250	ppm
	REFCLK input integrated jitter				600	ps rms
	REFCLK HIZ Leakage current				3	μA
	REFCLK HIZ Leakage current		-3			
Digital IO Electrical Characteristics: CLOCK						
t <sub>r</sub>	Rise time	Frequency = 60 MHz, Load = 10 pF			1	ns
t <sub>f</sub>	Fall time	Frequency = 30 MHz, Load = 10 pF			1	ns
Digital IO Electrical Characteristics: STP, DIR, NXT, DATA0 to DATA7						
t <sub>r</sub>	Rise time	Frequency = 30 MHz, Load = 10 pF			1	ns
t <sub>f</sub>	Fall time				1	ns

## 6.13 Timing Requirements

PARAMETER		INPUT CLOCK		OUTPUT CLOCK		UNIT
		MIN	MAX	MIN	MAX	
ULPI Interface Timing						
t <sub>SC</sub> , t <sub>SD</sub>	Set-up time (control in, 8-bit data in)	3		6		ns
t <sub>SC</sub> , t <sub>HD</sub>	Hold time (control in, 8-bit data in)	1.5		0		ns
t <sub>DC</sub> , t <sub>DD</sub>	Output delay (control out, 8-bit data out)	6		9		ns
USB UART Interface Timing						
t <sub>PH_DP_CON</sub>	Phone D+ connect time	100				ms
t <sub>PH_DISC_DET</sub>	Phone D+ disconnect time	150				ms
f <sub>UART_DFLT</sub>	Default UART signaling rate (typical rate)	9600				bps



**Figure 1. TUSB1210-Q1 Power-Up Timing (ULPI Clock Input Mode)**

**Table 2. Timers and Debounce**

PARAMETER	COMMENTS	MIN	TYP	MAX	UNIT
$t_{DEL\_CS\_SUPPLYOK}$	Chip-select-to-supplies OK delay		2.84	4.10	ms
$t_{DEL\_RST\_DIR}$	RESETB to PHY PLL locked and DIR falling-edge delay		0.54	0.647	ms
$t_{VBDET}$	$V_{BAT}$ detection delay		10		$\mu$ s
$t_{BGAP}$	Bandgap power-on delay		2		ms
$t_{PWONVDD15}$	$V_{DD15}$ power-on delay		100		$\mu$ s
$t_{PWONCK32K}$	32-KHz RC-OSC power-on delay		125		$\mu$ s
$t_{DELRSTPWR}$	Power control reset delay		61		$\mu$ s
$t_{DELMNTRVIOEN}$	Monitor enable delay		91.5		$\mu$ s
$t_{MNTR}$	Supply monitoring debounce		183.1		$\mu$ s
$t_{DELVDD33EN}$	$V_{DD33}$ LDO enable delay		93.75		$\mu$ s
$t_{DELRESETB}$	RESETB internal delay		244.1		$\mu$ s
$t_{PLL}$	PLL lock time		300		$\mu$ s

## TUSB1210-Q1

SLLSEL4A –SEPTEMBER 2014–REVISED OCTOBER 2014

[www.ti.com](http://www.ti.com)

### 6.13.1 Timing Parameter Definitions

The timing parameter symbols used in the timing requirement and switching characteristic tables are created in accordance with JEDEC Standard 100. To shorten the symbols, some pin names and other related terminologies have been abbreviated as shown in [Table 3](#).

**Table 3. Timing Parameter Definitions**

LOWERCASE SUBSCRIPTS	
SYMBOL	PARAMETER
C	Cycle time (period)
D	Delay time
Dis	Disable time
En	Enable time
H	Hold time
Su	Setup time
START	Start bit
T	Transition time
V	Valid time
W	Pulse duration (width)
X	Unknown, changing, or don't care level
H	High
L	Low
V	Valid
IV	Invalid
AE	Active edge
FE	First edge
LE	Last edge
Z	High impedance

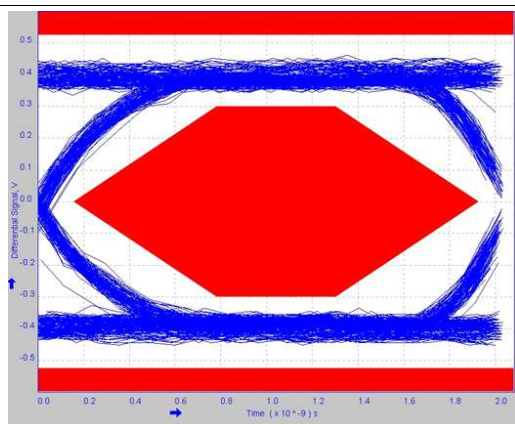
### 6.13.2 Interface Target Frequencies

[Table 4](#) assumes testing over the recommended operating conditions.

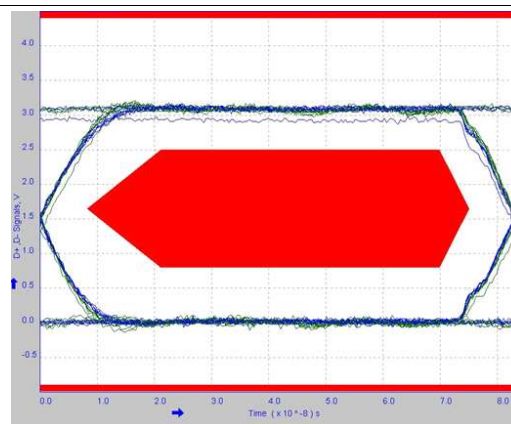
**Table 4. TUSB1210-Q1 Interface Target Frequencies**

IO INTERFACE	INTERFACE DESIGNATION		TARGET FREQUENCY 1.5 V
USB	Universal serial bus	High speed	480 Mbits/s
		Full speed	12 Mbits/s
		Low speed	1.5 Mbits/s

## 6.14 Typical Characteristics



**Figure 2. High-Speed Eye Diagram**



**Figure 3. Full-Speed Eye Diagram**

## TUSB1210-Q1

SLLSEL4A – SEPTEMBER 2014 – REVISED OCTOBER 2014

www.ti.com

## 7 Detailed Description

### 7.1 Overview

The TUSB1210-Q1 is a USB2.0 transceiver chip, designed to interface with a USB controller via a ULPI interface. It supports all USB2.0 data rates High-Speed, Full-Speed, and Low-Speed. Compliant to both Host and Peripheral (OTG) modes. It additionally supports a UART mode and legacy ULPI serial modes. TUSB1210-Q1 Integrates a 3.3-V LDO, which makes it flexible to work with either battery operated systems or pure 3.3 V supplied systems. Also, it has an integrated PLL Supporting 2 Clock Frequencies 19.2 MHz/26 MHz. The ULPI clock pin (60 MHz) supports both input and output clock configurations. TUSB1210-Q1 has low power consumption, optimized for portable devices, and complete USB OTG Physical Front-End that supports Host Negotiation Protocol (HNP) and Session Request Protocol (SRP).

TUSB1210-Q1 is optimized to be interfaced through a 12-pin SDR UTMI Low Pin Interface (ULPI), supporting both input clock and output clock modes, with 1.8 V interface supply voltage.

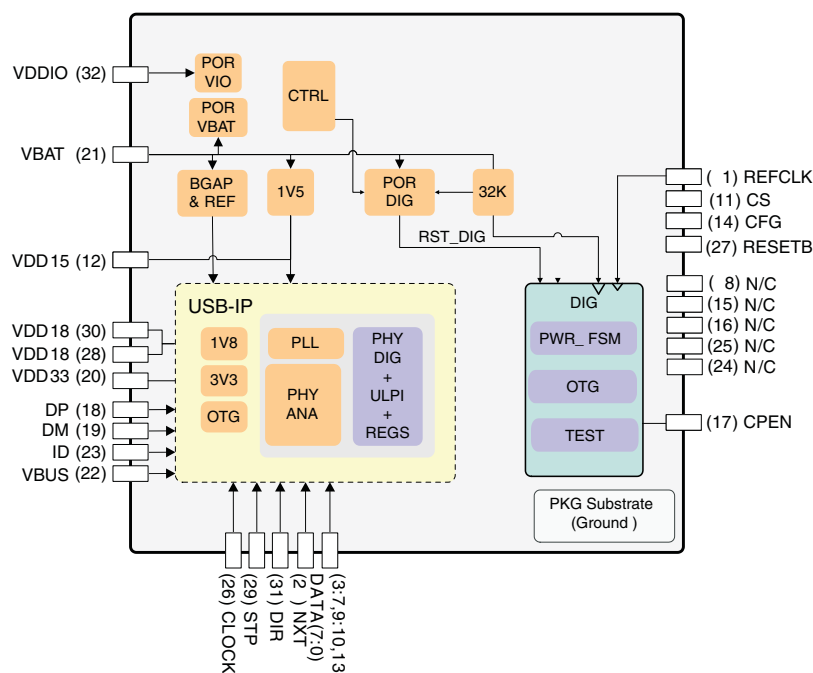
TUSB1210-Q1 integrates a 3.3 V LDO, which makes it flexible to work with either battery operated systems or pure 3.3 V supplied systems. Both the main supply and the 3.3 V power domain can be supplied through an external switched-mode converter for optimized power efficiency.

TUSB1210-Q1 includes a POR circuit to detect supply presence on  $V_{BAT}$  and  $V_{DDIO}$  pins. TUSB1210-Q1 can be disabled or configured in low power mode for energy saving.

TUSB1210-Q1 is protected against accidental shorts to 5 V or ground on its exposed interface (DP/DM/ID). It is also protected against up to 20 V surges on  $V_{BUS}$ .

TUSB1210-Q1 integrates a high-performance low-jitter 480 MHz PLL and supports two clock configurations. Depending on the required link configuration, TUSB1210-Q1 supports both ULPI input and output clock mode : input clock mode, in which case a square-wave 60 MHz clock is provided to TUSB1210-Q1 at the ULPI interface CLOCK pin; and output clock mode in which case TUSB1210-Q1 can accept a square-wave reference clock at REFCLK of either 19.2 MHz, 26 MHz. Frequency is indicated to TUSB1210-Q1 via the configuration pin CFG. This can be useful if a reference clock is already available in the system.

### 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Processor Subsystem

#### 7.3.1.1 Clock Specifications

##### 7.3.1.1.1 USB PLL Reference Clock

The USB PLL block generates the clocks used to synchronize :

- the ULPI interface (60 MHz clock)
- the USB interface (depending on the USB data rate, 480 Mbps, 12 Mbps or 1.5 Mbps)

TUSB1210-Q1 requires an external reference clock which is used as an input to the 480 MHz USB PLL block. Depending on the clock configuration, this reference clock can be provided either at REFCLK pin or at CLOCK pin. By default CLK pin is configured as an input.

Two clock configurations are possible:

- Input clock configuration (see [ULPI Input Clock Configuration](#))
- Output clock configuration (see [ULPI Output Clock Configuration](#))

##### 7.3.1.1.2 ULPI Input Clock Configuration

In this mode REFCLK must be externally tied to GND. CLOCK remains configured as an input.

When the ULPI interface is used in input clock configuration, that is, the 60 MHz ULPI clock is provided to TUSB1210-Q1 on Clock pin, then this is used as the reference clock for the 480 MHz USB PLL block. See [Switching Characteristics](#).

##### 7.3.1.1.3 ULPI Output Clock Configuration

In this mode a reference clock must be externally provided on REFCLK pin. When an input clock is detected on REFCLK pin then CLK will automatically change to an output, i.e., 60 MHz ULPI clock is output by TUSB1210-Q1 on CLK pin.

Two reference clock input frequencies are supported. REFCLK input frequency is communicated to TUSB1210-Q1 via a configuration pin, CFG, see  $f_{REFCLK}$  in [Table 11](#) for frequency correspondence. TUSB1210-Q1 supports square-wave reference clock input only. Reference clock input must be square-wave of amplitude in the range 3 V to 3.6 V. See [Switching Characteristics](#).

##### 7.3.1.1.4 Clock 32 kHz

An internal clock generator running at 32 kHz has been implemented to provide a low-speed, low-power clock to the system. See [Clock 32 kHz](#).

##### 7.3.1.1.5 Reset

All logic is reset if CS = 0 or  $V_{BAT}$  are not present.

All logic (except 32 kHz logic) is reset if  $V_{DDIO}$  is not present.

PHY logic is reset when any supplies are not present ( $V_{DDIO}$ ,  $V_{DD15}$ ,  $V_{DD18}$ ,  $V_{DD33}$ ) or if RESETB pin is low.

TUSB1210-Q1 may be reset manually by toggling the RESETB pin to GND for at least 200 ns.

If manual reset via RESETB is not required then RESETB pin may be tied to  $V_{DDIO}$  permanently.

### 7.3.1.2 USB Transceiver

The TUSB1210-Q1 device includes a universal serial bus (USB) on-the-go (OTG) transceiver that supports USB 480 Mb/s high-speed (HS), 12 Mb/s full-speed (FS), and USB 1.5 Mb/s low-speed (LS) through a 12-pin UTMI+ low pin interface (ULPI).



## TUSB1210-Q1

SLLSEL4A – SEPTEMBER 2014 – REVISED OCTOBER 2014

www.ti.com

### Feature Description (continued)

#### NOTE

LS device mode is not allowed by a USB2.0 HS capable PHY, therefore it is not supported by TUSB1210-Q1. This is stated in USB2.0 standard Chapter 7, page 119, second paragraph: "A *high-speed capable upstream facing transceiver must not support low-speed signaling mode.*" There is also some related commentary in Chapter 7.1.2.3.

#### 7.3.1.2.1 PHY Electrical Characteristics

The PHY is the physical signaling layer of the USB 2.0. It essentially contains all the drivers and receivers required for physical data and protocol signaling on the DP and DM lines.

The PHY interfaces to the USB controller through a standard 12-pin digital interface called UTMI+ low pin interface (ULPI).

The transmitters and receivers inside the PHY are classified into two main classes.

- The full-speed (FS) and low-speed (LS) transceivers. These are the legacy USB1.x transceivers.
- The HS (HS) transceivers

In order to bias the transistors and run the logic, the PHY also contains reference generation circuitry which consists of:

- A DPLL which does a frequency multiplication to achieve the 480-MHz low-jitter lock necessary for USB and also the clock required for the switched capacitor resistance block.
- A switched capacitor resistance block which is used to replicate an external resistor on chip.

Built-in pullup and pulldown resistors are used as part of the protocol signaling.

Apart from this, the PHY also contains circuitry which protects it from accidental 5-V short on the DP and DM lines.

##### 7.3.1.2.1.1 LS/FS Single-Ended Receivers

In addition to the differential receiver, there is a single-ended receiver (SE–, SE+) for each of the two data lines D+/. The main purpose of the single-ended receivers is to qualify the D+ and D– signals in the full-speed/low-speed modes of operation. See [PHY Electrical Characteristics](#).

##### 7.3.1.2.1.2 LS/FS Differential Receiver

A differential input receiver (Rx) retrieves the LS/FS differential data signaling. The differential voltage on the line is converted into digital data by a differential comparator on DP/DM. This data is then sent to a clock and data recovery circuit which recovers the clock from the data. An additional serial mode exists in which the differential data is directly output on the RXRCV pin. See [Switching Characteristics](#).

##### 7.3.1.2.1.3 LS/FS Transmitter

The USB transceiver (Tx) uses a differential output driver to drive the USB data signal D+/. onto the USB cable. The driver's outputs support 3-state operation to achieve bidirectional half-duplex transactions. See [Switching Characteristics](#).

##### 7.3.1.2.1.4 HS Differential Receiver

The HS receiver consists of the following blocks:

A differential input comparator to receive the serial data

- A squelch detector to qualify the received data
- An oversampler-based clock data recovery scheme followed by a NRZI decoder, bit unstuffing, and serial-to-parallel converter to generate the ULPI DATAOUT

See [Switching Characteristics](#).

## Feature Description (continued)

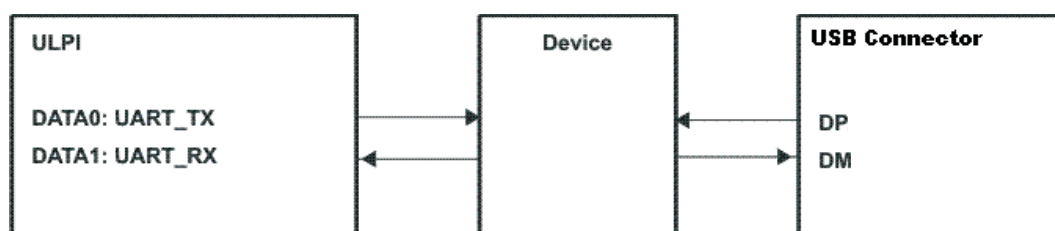
### 7.3.1.2.1.5 HS Differential Transmitter

The HS transmitter is always operated via the ULPI parallel interface. The parallel data on the interface is serialized, bit stuffed, NRZI encoded, and transmitted as a dc output current on DP or DM depending on the data. Each line has an effective 22.5-Ω load to ground, which generates the voltage levels for signaling.

A disconnect detector is also part of the HS transmitter. A disconnect on the far end of the cable causes the impedance seen by the transmitter to double thereby doubling the differential amplitude seen on the DP/DM lines of [Switching Characteristics](#).

### 7.3.1.2.1.6 UART Transceiver

In this mode, the ULPI data bus is redefined as a 2-pin UART interface, which exchanges data through a direct access to the FS/LS analog transmitter and receiver. See [Switching Characteristics](#).



**Figure 4. USB UART Data Flow**

### 7.3.1.2.2 OTG Characteristics

The on-the-go (OTG) block integrates three main functions:

- The USB plug detection function on  $V_{BUS}$  and ID
- The ID resistor detection
- The  $V_{BUS}$  level detection

See [OTG Electrical Characteristics](#).

## TUSB1210-Q1

SLLSEL4A –SEPTEMBER 2014–REVISED OCTOBER 2014

www.ti.com

### 7.4 Device Functional Modes

#### 7.4.1 TUSB1210-Q1 Modes vs ULPI Pin Status

Table 5, Table 6, and Table 7 show the status of each of the 12 ULPI pins including input/output direction and whether output pins are driven to '0' or to '1', or pulled up/pulled down via internal pullup/pulldown resistors.

Note that pullup/pulldown resistors are automatically replaced by driven '1'/'0' levels respectively once internal IORST is released, with the exception of the pullup on STP which is maintained in all modes.

Pin assignment changes in ULPI 3-pin serial mode, ULPI 6-pin serial mode, and UART mode. Unused pins are tied low in these modes as shown below.

**Table 5. TUSB1210-Q1 Modes vs ULPI Pin Status:ULPI Synchronous Mode Power-Up**

		ULPI SYNCHRONOUS MODE POWER-UP							
		UNTIL IORST RELEASE		PLL OFF		PLL ON + STP HIGH		PLL ON + STP LOW	
PIN NO.	PIN NAME	DIR	PU/PD	DIR	PU/PD	DIR	PU/PD	DIR	PU/PD
26	CLOCK	Hiz	PD	I	PD	IO	-	IO	-
31	DIR	Hiz	PU	O, ('1')	-	O, ('0')	-	O	-
2	NXT	Hiz	PD	O, ('0')	-	O, ('0')	-	O	-
29	STP	Hiz	PU	I	PU	I	PU	I	PU
3	DATA0	Hiz	PD	O, ('0')	-	I	PD	IO	-
4	DATA1	Hiz	PD	O, ('0')	-	I	PD	IO	-
5	DATA2	Hiz	PD	O, ('0')	-	I	PD	IO	-
6	DATA3	Hiz	PD	O, ('0')	-	I	PD	IO	-
7	DATA4	Hiz	PD	O, ('0')	-	I	PD	IO	-
9	DATA5	Hiz	PD	O, ('0')	-	I	PD	IO	-
10	DATA6	Hiz	PD	O, ('0')	-	I	PD	IO	-
13	DATA7	Hiz	PD	O, ('0')	-	I	PD	IO	-

**Table 6. TUSB1210-Q1 Modes vs ULPI Pin Status: USB Suspend Mode**

		SUSPEND MODE		LINK / EXTERNAL RECOMMENDED SETTING DURING SUSPEND MODE	
		DIR	PU/PD	DIR	PU/PD
26	CLOCK	I	-	O	-
31	DIR	O, ('1')	-	I	-
2	NXT	O, ('0')	-	I	-
29	STP	I	PU <sup>(1)</sup>	O, ('0')	-
3	DATA0	O, (LINESTATE0)	-	I	-
4	DATA1	O, (LINESTATE1)	-	I	-
5	DATA2	O, ('0')	-	I	-
6	DATA3	O, (INT)	-	I	-
7	DATA4	O, ('0')	-	I	-
9	DATA5	O, ('0')	-	I	-
10	DATA6	O, ('0')	-	I	-
13	DATA7	O, ('0')	-	I	-

(1) Can be disabled by software before entering Suspend Mode to reduce current consumption

**Table 7. TUSB1210-Q1 Modes vs ULPI Pin Status: ULPI 6-Pin Serial Mode and UART Mode**

PIN NO.	ULPI 6-PIN SERIAL MODE			ULPI 3-PIN SERIAL MODE			UART MODE		
	PIN NAME	DIR	PU/PD	PIN NAME	DIR	PU/PD	PIN NAME	DIR	PU/PD
26	CLOCK (1)	IO	-	CLOCK (1)	IO	-	CLOCK (1)	IO	-
31	DIR	O	-	DIR	O	-	DIR	O	-
2	NXT	O	-	NXT	O	-	NXT	O	-
29	STP	I	PU	STP	I	PU	STP	I	PU
3	TX_ENABLE	I	-	TX_ENABLE	I	-	TXD	I	-
4	TX_DAT	I	-	DAT	IO	-	RXD	IO	-
5	TX_SE0	I	-	SE0	IO	-	tie low	O	-
6	INT	O	-	INT	O	-	INT	O	-
7	RX_DP	O	-	tie low	O	-	tie low	O	-
9	RX_DM	O	-	tie low	O	-	tie low	O	-
10	RX_RCV	O	-	tie low	O	-	tie low	O	-
13	tie low	O	-	tie low	O	-	tie low	O	-

## TUSB1210-Q1

SLLSEL4A – SEPTEMBER 2014 – REVISED OCTOBER 2014

[www.ti.com](http://www.ti.com)

## 7.5 Register Map

**Table 8. USB Register Summary**

REGISTER NAME	TYPE	REGISTER WIDTH (BITS)	PHYSICAL ADDRESS
VENDOR_ID_LO	R	8	0x00
VENDOR_ID_HI	R	8	0x01
PRODUCT_ID_LO	R	8	0x02
PRODUCT_ID_HI	R	8	0x03
FUNC_CTRL	RW	8	0x04
FUNC_CTRL_SET	RW	8	0x05
FUNC_CTRL_CLR	RW	8	0x06
IFC_CTRL	RW	8	0x07
IFC_CTRL_SET	RW	8	0x08
IFC_CTRL_CLR	RW	8	0x09
OTG_CTRL	RW	8	0x0A
OTG_CTRL_SET	RW	8	0x0B
OTG_CTRL_CLR	RW	8	0x0C
USB_INT_EN_RISE	RW	8	0x0D
USB_INT_EN_RISE_SET	RW	8	0x0E
USB_INT_EN_RISE_CLR	RW	8	0x0F
USB_INT_EN_FALL	RW	8	0x10
USB_INT_EN_FALL_SET	RW	8	0x11
USB_INT_EN_FALL_CLR	RW	8	0x12
USB_INT_STS	R	8	0x13
USB_INT_LATCH	R	8	0x14
DEBUG	R	8	0x15
SCRATCH_REG	RW	8	0x16
SCRATCH_REG_SET	RW	8	0x17
SCRATCH_REG_CLR	RW	8	0x18
Reserved	R	8	0x19 0x2E
ACCESS_EXT_REG_SET	RW	8	0x2F
Reserved	R	8	0x30 0x3C
VENDOR_SPECIFIC1	RW	8	0x3D
VENDOR_SPECIFIC1_SET	RW	8	0x3E
VENDOR_SPECIFIC1_CLR	RW	8	0x3F
VENDOR_SPECIFIC2	RW	8	0x80
VENDOR_SPECIFIC2_SET	RW	8	0x81
VENDOR_SPECIFIC2_CLR	RW	8	0x82
VENDOR_SPECIFIC1_STS	R	8	0x83
VENDOR_SPECIFIC1_LATCH	R	8	0x84
VENDOR_SPECIFIC3	RW	8	0x85
VENDOR_SPECIFIC3_SET	RW	8	0x86
VENDOR_SPECIFIC3_CLR	RW	8	0x87

### 7.5.1 VENDOR\_ID\_LO

ADDRESS OFFSET		0x00							
PHYSICAL ADDRESS		0x00		INSTANCE		USB_SCUSB			
DESCRIPTION		Lower byte of vendor ID supplied by USB-IF (TI Vendor ID = 0x0451)							
TYPE		R							
WRITE LATENCY									
7	6	5	4	3	2	1	0		
VENDOR_ID									
BITS		FIELD NAME		DESCRIPTION		TYPE		RESET	
7:00		VENDOR_ID				R		0x51	

### 7.5.2 VENDOR\_ID\_HI

ADDRESS OFFSET		0x01						
PHYSICAL ADDRESS		0x01		INSTANCE		USB_SCUSB		
DESCRIPTION		Upper byte of vendor ID supplied by USB-IF (TI Vendor ID = 0x0451)						
TYPE		R						
WRITE LATENCY								
7	6	5	4	3	2	1	0	
VENDOR_ID								
BITS		FIELD NAME		DESCRIPTION		TYPE		RESET
7:00		VEN DOR_ID				R		0x04

### 7.5.3 PRODUCT\_ID\_LO

ADDRESS OFFSET		0x02						
PHYSICAL ADDRESS		0x02		INSTANCE		USB_SCUSB		
DESCRIPTION		Lower byte of Product ID supplied by Vendor (TUSB1210-Q1 Product ID is 0x1507).						
TYPE		R						
WRITE LATENCY								
7	6	5	4	3	2	1	0	
PRODUCT_ID								
BITS		FIELD NAME		DESCRIPTION		TYPE		RESET
7:00		PRODUCT_ID				R		0x07

## TUSB1210-Q1

SLLSEL4A –SEPTEMBER 2014–REVISED OCTOBER 2014

www.ti.com

### 7.5.4 PRODUCT\_ID\_HI

ADDRESS OFFSET		0x03							
PHYSICAL ADDRESS		0x03		INSTANCE		USB_SCUSB			
DESCRIPTION		Upper byte of Product ID supplied by Vendor (TUSB1210-Q1 Product ID is 0x1507).							
TYPE		R							
WRITE LATENCY									
7	6	5	4	3	2	1	0		
PRODUCT_ID									
BITS		FIELD NAME		DESCRIPTION		TYPE		RESET	
7:00		PRODUCT_ID				R		0x15	

### 7.5.5 FUNC\_CTRL

ADDRESS OFFSET		0x04													
PHYSICAL ADDRESS		0x04		INSTANCE	USB_SCUSB										
DESCRIPTION		Controls UTMI function settings of the PHY.													
TYPE		RW													
WRITE LATENCY															
7		6		5		4		3		2		1		0	
Reserved		SUSPENDM		RESET		OPMODE				TERMSELECT		XCVRSELECT			
BITS		FIELD NAME		DESCRIPTION								TYPE		RESET	
7		Reserved										R		0	
6		SUSPENDM		Active low PHY suspend. Put PHY into Low Power Mode. In Low Power Mode the PHY power down all blocks except the full speed receiver, OTG comparators, and the ULPI interface pins. The PHY automatically set this bit to '1' when Low Power Mode is exited.								RW		1	
5		RESET		Active high transceiver reset. Does not reset the ULPI interface or ULPI register set.  Once set, the PHY asserts the DIR signal and reset the UTMI core. When the reset is completed, the PHY de-asserts DIR and clears this bit. After de-asserting DIR, the PHY re-assert DIR and send an RX command update.  Note: This bit is auto-cleared, this explain why it can't be read at '1'.								RW		0	
4:03		OPMODE		Select the required bit encoding style during transmit  0x0: Normal operation  0x1: Non-driving  0x2: Disable bit-stuff and NRZI encoding  0x3: Reserved (No SYNC and EOP generation feature not supported)								RW		0x0	
2		TERMSELECT		Controls the internal 1.5Kohms pull-up resistor and 45ohms HS terminations. Control over bus resistors changes depending on XcvrSelect, OpMode, DpPulldown and DmPulldown.								RW		0	
1:00		XCVRSELECT		Select the required transceiver speed.  0x0: Enable HS transceiver  0x1: Enable FS transceiver  0x2: Enable LS transceiver  0x3: Enable FS transceiver for LS packets  (FS preamble is automatically pre-pended)								RW		0x1	

### 7.5.6 FUNC\_CTRL\_SET

ADDRESS OFFSET	0x05						
PHYSICAL ADDRESS	0x05			INSTANCE	USB_SCUSB		

<b>DESCRIPTION</b>		This register doesn't physically exist. It is the same as the func_ctrl register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action).					
<b>TYPE</b>		RW					
<b>WRITE LATENCY</b>							
<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
Reserved	SUSPENDM	RESET	OPMODE		TERMSELECT	XCVRSELECT	
<b>BITS</b>	<b>FIELD NAME</b>		<b>DESCRIPTION</b>		<b>TYPE</b>		<b>RESET</b>
7	Reserved				R		0
6	SUSPENDM				RW		1
5	RESET				RW		0
4:03	OPMODE				RW		0x0
2	TERMSELECT				RW		0
1:00	XCVRSELECT				RW		0x1

### 7.5.7 FUNC\_CTRL\_CLR

ADDRESS OFFSET		0x06						
PHYSICAL ADDRESS		0x06		INSTANCE		USB_SCUSB		
DESCRIPTION		This register doesn't physically exist. It is the same as the func_ctrl register with read/clear-only property (write '1' to clear a particular bit, a write '0' has no-action).						
TYPE		RW						
WRITE LATENCY								
7	6	5	4	3	2	1	0	
Reserved	SUSPENDM	RESET	OPMODE		TERMSELECT	XCVRSELECT		
BITS		FIELD NAME		DESCRIPTION		TYPE		RESET
7		Reserved				R		0
6		SUSPENDM				RW		1
5		RESET				RW		0
4:03		OPMODE				RW		0x0
2		TERMSELECT				RW		0
1:00		XCVRSELECT				RW		0x1



## TUSB1210-Q1

SLLSEL4A – SEPTEMBER 2014 – REVISED OCTOBER 2014

www.ti.com

### 7.5.8 IFC\_CTRL

ADDRESS OFFSET		0x07						
PHYSICAL ADDRESS		0x07		INSTANCE		USB_SCUSB		
DESCRIPTION		Enables alternative interfaces and PHY features.						
TYPE		RW						
WRITE LATENCY								
7	6	5	4	3	2	1	0	
INTERFACE_PROTECT_DISABLE	INDICATORPASSTHRU	INDICATORCOMPLEMENT	AUTORESUME	CLOCKSUSPENDM	CARKITMODE	FSLSSERIALMODE_3PIN	FSLSSERIALMODE_6PIN	
BITS	FIELD NAME		DESCRIPTION				TYPE	RESET
7	INTERFACE_PROTECT_DISABLE		Controls circuitry built into the PHY for protecting the ULPI interface when the link tri-states stp and data. 0b: Enables the interface protect circuit 1b: Disables the interface protect circuit				RW	0
6	INDICATORPASSTHRU		Controls whether the complement output is qualified with the internal vbusvalid comparator before being used in the VBUS State in the RXCMD. 0b: Complement output signal is qualified with the internal VBUSVALID comparator. 1b: Complement output signal is not qualified with the internal VBUSVALID comparator.				RW	0
5	INDICATORCOMPLEMENT		Tells the PHY to invert EXTERNALVBUSINDICATOR input signal, generating the complement output. 0b: PHY will not invert signal EXTERNALVBUSINDICATOR (default) 1b: PHY will invert signal EXTERNALVBUSINDICATOR				RW	0
4	AUTORESUME		Enables the PHY to automatically transmit resume signaling. Refer to USB specification 7.1.7.7 and 7.9 for more details. 0 = AutoResume disabled 1 = AutoResume enabled (default)				RW	1
3	CLOCKSUSPENDM		Active low clock suspend. Valid only in Serial Modes. Powers down the internal clock circuitry only. Valid only when SuspendM = 1b. The PHY must ignore ClockSuspend when SuspendM = 0b. By default, the clock will not be powered in Serial and Carkit Modes. 0b : Clock will not be powered in Serial and UART Modes. 1b : Clock will be powered in Serial and UART Modes.				RW	0
2	CARKITMODE		Changes the ULPI interface to UART interface. The PHY automatically clear this field when UART mode is exited. 0b: UART disabled. 1b: Enable serial UART mode.				RW	0
1	FSLSSERIALMODE_3PIN		Changes the ULPI interface to 3-pin Serial. The PHY must automatically clear this field when serial mode is exited. 0b: FS/LS packets are sent using parallel interface 1b: FS/LS packets are sent using 4-pin serial interface				RW	0
0	FSLSSERIALMODE_6PIN		Changes the ULPI interface to 6-pin Serial. The PHY must automatically clear this field when serial mode is exited. 0b: FS/LS packets are sent using parallel interface 1b: FS/LS packets are sent using 6-pin serial interface				RW	0

### 7.5.9 IFC\_CTRL\_SET

ADDRESS OFFSET	0x08		
PHYSICAL ADDRESS	0x08	INSTANCE	USB_SCUSB
DESCRIPTION	This register doesn't physically exist. It is the same as the ifc_ctrl register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action).		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
INTERFACE_PROTECT_DISABLE	INDICATORPASSTHRU	INDICATORCOMPLEMENT	AUTORESUME	CLOCKSUSPENDMODE	CARKITMODE	FSLSSERIALMODE_3PIN	FSLSSERIALMODE_6PIN
BITS	FIELD NAME		DESCRIPTION		TYPE		RESET
7	INTERFACE_PROTECT_DISABLE				RW		0
6	INDICATORPASSTHRU				RW		0
5	INDICATORCOMPLEMENT				RW		0
4	AUTORESUME				RW		1
3	CLOCKSUSPENDMODE				RW		0
2	CARKITMODE				RW		0
1	FSLSSERIALMODE_3PIN				RW		0
0	FSLSSERIALMODE_6PIN				R		0

## TUSB1210-Q1

SLLSEL4A – SEPTEMBER 2014 – REVISED OCTOBER 2014

[www.ti.com](http://www.ti.com)

### 7.5.10 IFC\_CTRL\_CLR

ADDRESS OFFSET		0x09					
PHYSICAL ADDRESS		0x09		INSTANCE		USB_SCUSB	
DESCRIPTION		This register doesn't physically exist. It is the same as the ifc_ctrl register with read/clear-only property (write '1' to clear a particular bit, a write '0' has no-action).					
TYPE		RW					
WRITE LATENCY							
7	6	5	4	3	2	1	0
INTERFACE_P ROTECT_DISA BLE	IN DICATORPAS STHRU	INDICATORCO MPLEMENT	AUTORESUME	CLOCKSUSPE NDM	CARKITMODE	FSLSSERIALM ODE_3PIN	FSLSSERIALM ODE_6PIN
BITS	FIELD NAME			DESCRIPTION		TYPE	RESET
7	INTERFACE_PROTECT_DISABLE					RW	0
6	INDICATORPASSTHRU					RW	0
5	INDICATORCOMPLEMENT					RW	0
4	AUTORESUME					RW	1
3	CLOCKSUSPENDM					RW	0
2	CARKITMODE					RW	0
1	FSLSSERIALMODE_3PIN					RW	0
0	FSLSSERIALMODE_6PIN					R	0

### 7.5.11 OTG\_CTRL

ADDRESS OFFSET		0x0A						
PHYSICAL ADDRESS		0x0A		INSTANCE		USB_SCUSB		
DESCRIPTION		Controls UTMI+ OTG functions of the PHY.						
TYPE		RW						
WRITE LATENCY								
7	6	5	4	3	2	1	0	
USEEXTERNALVBUSINDICATOR	DRVVBUSEXTERNAL	DRVVBUS	CHRGVBUS	DISCHRGVBUS	DMPULLDOWN	DPPULLDOWN	IDPULLUP	
BITS	FIELD NAME		DESCRIPTION				TYPE	RESET
7	USEEXTERNALVBUSINDICATOR		Tells the PHY to use an external VBUS over-current indicator.  0b: Use the internal OTG comparator (VA_VBUS_VLD) or internal VBUS valid indicator (default) 1b: Use external VBUS valid indicator signal.				RW	0
6	DRVVBUSEXTERNAL		Selects between the internal and the external 5 V VBUS supply.  0b: Pin17 (CPEN) is disabled (output GND level). TUSB1210-Q1 does not support internal VBUS supply. 1b: Pin17 (CPEN) is set to '1' (output VDD33 voltage level) if DRVVBUS bit is '1', else Pin17 (CPEN) is disabled (output GND level) if DRVVBUS bit is '0'				RW	0
5	DRVVBUS		VBUS output control bit  0b : do not drive VBUS 1b : drive 5V on VBUS  Note: Both DRVVBUS and DRVVBUSEXTERNAL bits must be set to 1 in order to set Pin17 (CPEN). CPEN pin can be used to enable an external VBUS supply				RW	0
4	CHRGVBUS		Charge VBUS through a resistor. Used for VBUS pulsing SRP. The Link must first check that VBUS has been discharged (see DischrgVbus register bit), and that both D+ and D- data lines have been low (SE0) for 2ms.  0b : do not charge VBUS 1b : charge VBUS				RW	0
3	DISCHRGVBUS		Discharge VBUS through a resistor. If the Link sets this bit to 1, it waits for an RX CMD indicating SessEnd has transitioned from 0 to 1, and then resets this bit to 0 to stop the discharge.  0b : do not discharge VBUS 1b : discharge VBUS				RW	0
2	DMPULLDOWN		Enables the 15k Ohm pull-down resistor on D-.  0b : Pull-down resistor not connected to D-. 1b : Pull-down resistor connected to D-.				RW	1
1	DPPULLDOWN		Enables the 15k Ohm pull-down resistor on D+.  0b : Pull-down resistor not connected to D+. 1b : Pull-down resistor connected to D+.				RW	1
0	IDPULLUP		Connects a pull-up to the ID line and enables sampling of the signal level.  0b : Disable sampling of ID line. 1b : Enable sampling of ID line.				RW	0

### 7.5.12 OTG\_CTRL\_SET

ADDRESS OFFSET	0x0B		
PHYSICAL ADDRESS	0x0B	INSTANCE	USB_SCUSB
DESCRIPTION	This register doesn't physically exist. It is the same as the otg_ctrl register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action).		
TYPE	RW		
WRITE LATENCY			

## TUSB1210-Q1

SLLSEL4A – SEPTEMBER 2014 – REVISED OCTOBER 2014

[www.ti.com](http://www.ti.com)

7	6	5	4	3	2	1	0
USEEXTERNALV BUSINDICA TOR	DRVVBUSEXT ERNAL	DRVVBUS	CHRGVBUS	DISCHRGVBU S	DMPULLDOWN	DPPULLDOWN	IDPULLUP
BITS	FIELD NAME			DESCRIPTION		TYPE	RESET
7	USEEXTERNALVBUSINDICATOR					RW	0
6	DRVVBUSEXTERNAL					RW	0
5	DRVVBUS					RW	0
4	CHRGVBUS					RW	0
3	DISCHRGVBUS					RW	0
2	DMPULLDOWN					RW	1
1	DPPULLDOWN					RW	1
0	IDPULLUP					RW	0

**7.5.13 OTG\_CTRL\_CLR**

ADDRESS OFFSET		0x0C					
PHYSICAL ADDRESS		0x0C		INSTANCE		USB_SCUSB	
DESCRIPTION		This register doesn't physically exist. It is the same as the otg_ctrl register with read/Clear-only property (write '1' to clear a particular bit, a write '0' has no-action).					
TYPE		RW					
WRITE LATENCY							
7	6	5	4	3	2	1	0
USEEXTERNALV BUSINDICA TOR	DRVVBUSEXT ERNAL	DRVVBUS	CHRGVBUS	DISCHRGVBU S	DMPULLDOWN N	DPPULLDOWN	IDPULLUP
BITS	FIELD NAME			DESCRIPTION		TYPE	RESET
7	USEEXTERNALV BUSINDICATOR					RW	0
6	DRVVBUSEXT ERNAL					RW	0
5	DRVVBUS					RW	0
4	CHRGVBUS					RW	0
3	DISCHRGVBUS					RW	0
2	DMPULLDOWN					RW	1
1	DPPULLDOWN					RW	1
0	IDPULLUP					RW	0

## TUSB1210-Q1

SLLSEL4A – SEPTEMBER 2014 – REVISED OCTOBER 2014

[www.ti.com](http://www.ti.com)

### 7.5.14 USB\_INT\_EN\_RISE

ADDRESS OFFSET		0x0D													
PHYSICAL ADDRESS		0x0D		INSTANCE		USB_SCUSB									
DESCRIPTION		If set, the bits in this register cause an interrupt event notification to be generated when the corresponding PHY signal changes from low to high. By default, all transitions are enabled.													
TYPE		RW													
WRITE LATENCY															
7		6		5		4		3		2		1		0	
Reserved		Reserved		Reserved		IDGND_RISE		SESEND_RISE		SESSVALID_RISE		VBUSVALID_RISE		HOSTDISCONNECT_RISE	
BITS	FIELD NAME			DESCRIPTION								TYPE		RESET	
7	Reserved											R		0	
6	Reserved											R		0	
5	Reserved											R		0	
4	IDGND_RISE			Generate an interrupt event notification when IdGnd changes from low to high.								RW		1	
				Event is automatically masked if IdPullup bit is clear to 0 and for 50ms after IdPullup is set to 1.											
3	SESEND_RISE			Generate an interrupt event notification when SessEnd changes from low to high.								RW		1	
2	SESSVALID_RISE			Generate an interrupt event notification when SessValid changes from low to high. SessValid is the same as UTMI+ AValid.								RW		1	
1	VBUSVALID_RISE			Generate an interrupt event notification when VbusValid changes from low to high.								RW		1	
0	HOSTDISCONNECT_RISE			Generate an interrupt event notification when Hostdisconnect changes from low to high. Applicable only in host mode (DpPulldown and DmPulldown both set to 1b).								RW		1	

### 7.5.15 USB\_INT\_EN\_RISE\_SET

ADDRESS OFFSET		0x0E						
PHYSICAL ADDRESS		0x0E		INSTANCE		USB_SCUSB		
DESCRIPTION		This register doesn't physically exist. It is the same as the usb_int_en_rise register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action).						
TYPE		RW						
WRITE LATENCY								
7	6	5	4	3	2	1	0	
Reserved	Reserved	Reserved	IDGND_RISE	SESEND_RISE	SESSVALID_RISE	VBUSVALID_RISE	HOSTDISCONNECT_RISE	
BITS		FIELD NAME		DESCRIPTION		TYPE		RESET
7		Reserved				R		0
6		Reserved				R		0
5		Reserved				R		0
4		IDGND_RISE				RW		1
3		SESEND_RISE				RW		1
2		SESSVALID_RISE				RW		1
1		VBUSVALID_RISE				RW		1
0		HOSTDISCONNECT_RISE				RW		1



**TUSB1210-Q1**

SLLSEL4A – SEPTEMBER 2014 – REVISED OCTOBER 2014

[www.ti.com](http://www.ti.com)
**7.5.16 USB\_INT\_EN\_RISE\_CLR**

ADDRESS OFFSET		0x0F					
PHYSICAL ADDRESS		0x0F		INSTANCE		USB_SCUSB	
DESCRIPTION		This register doesn't physically exist. It is the same as the usb_int_en_rise register with read/clear-only property (write '1' to clear a particular bit, a write '0' has no-action).					
TYPE		RW					
WRITE LATENCY							
7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	IDGND_RISE	SESEND_RISE	SESSVALID_RISE	VBUSVALID_RISE	HOSTDISCONNECT_RISE
BITS	FIELD NAME		DESCRIPTION		TYPE	RESET	
7	Reserved				R	0	
6	Reserved				R	0	
5	Reserved				R	0	
4	IDGND_RISE				RW	1	
3	SESEND_RISE				RW	1	
2	SESSVALID_RISE				RW	1	
1	VBUSVALID_RISE				RW	1	
0	HOSTDISCONNECT_RISE				RW	1	

**7.5.17 USB\_INT\_EN\_FALL**

ADDRESS OFFSET		0x10						
PHYSICAL ADDRESS		0x10		INSTANCE		USB_SCUSB		
DESCRIPTION		If set, the bits in this register cause an interrupt event notification to be generated when the corresponding PHY signal changes from low to high. By default, all transitions are enabled.						
TYPE		RW						
WRITE LATENCY								
7		6	5	4	3	2	1	0
Reserved		Reserved	Reserved	IDGND_FALL	SESEND_FALL	SESSVALID_FALL	VBUSVALID_FALL	HOSTDISCONNECT_FALL
BITS	FIELD NAME		DESCRIPTION				TYPE	RESET
7	Reserved						R	0
6	Reserved						R	0
5	Reserved						R	0
4	IDGND_FALL		Generate an interrupt event notification when IdGnd changes from high to low.  Event is automatically masked if IdPullup bit is clear to 0 and for 50ms after IdPullup is set to 1.				RW	1
3	SESEND_FALL		Generate an interrupt event notification when SessEnd changes from high to low.				RW	1
2	SESSVALID_FALL		Generate an interrupt event notification when SessValid changes from high to low. SessValid is the same as UTMI+ AValid.				RW	1
1	VBUSVALID_FALL		Generate an interrupt event notification when VbusValid changes from high to low.				RW	1
0	HOSTDISCONNECT_FALL		Generate an interrupt event notification when Hostdisconnect changes from high to low. Applicable only in host mode (DpPulldown and DmPulldown both set to 1b).				RW	1

**TUSB1210-Q1**

SLLSEL4A – SEPTEMBER 2014 – REVISED OCTOBER 2014

[www.ti.com](http://www.ti.com)
**7.5.18 USB\_INT\_EN\_FALL\_SET**

ADDRESS OFFSET		0x11					
PHYSICAL ADDRESS		0x11		INSTANCE		USB_SCUSB	
DESCRIPTION		This register doesn't physically exist. It is the same as the usb_int_en_fall register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action)					
TYPE		RW					
WRITE LATENCY							
7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	IDGND_FALL	SESEND_FALL	SESSVALID_FALL	VBUSVALID_FALL	HOSTDISCONNECT_FALL
BITS	FIELD NAME		DESCRIPTION			TYPE	RESET
7	Reserved					R	0
6	Reserved					R	0
5	Reserved					R	0
4	IDGND_FALL					RW	1
3	SESEND_FALL					RW	1
2	SESSVALID_FALL					RW	1
1	VBUSVALID_FALL					RW	1
0	HOSTDISCONNECT_FALL					RW	1

### 7.5.19 USB\_INT\_EN\_FALL\_CLR

ADDRESS OFFSET	0x12		
PHYSICAL ADDRESS	0x12	INSTANCE	USB_SCUSB
DESCRIPTION	<p>This register doesn't physically exist.</p> <p>It is the same as the usb_int_en_fall register with read/clear-only property (write '1' to clear a particular bit, a write '0' has no-action).</p>		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	IDGND_FALL	SESEND_FALL	SESSVALID_F ALL	VBUSVALID_F ALL	HOSTDISCON NECT_FALL
BITS	FIELD NAME		DESCRIPTION			TYPE	RESET
7	Reserved					R	0
6	Reserved					R	0
5	Reserved					R	0
4	IDGND_FALL					RW	1
3	SESEND_FALL					RW	1
2	SESSVALID_FALL					RW	1
1	VBUSVALID_FALL					RW	1
0	HOSTDISCONNECT_FALL					RW	1

## TUSB1210-Q1

SLLSEL4A – SEPTEMBER 2014 – REVISED OCTOBER 2014

[www.ti.com](http://www.ti.com)

### 7.5.20 USB\_INT\_STS

ADDRESS OFFSET		0x13						
PHYSICAL ADDRESS		0x13		INSTANCE		USB_SCUSB		
DESCRIPTION		Indicates the current value of the interrupt source signal.						
TYPE		R						
WRITE LATENCY								
7		6	5	4	3	2	1	0
Reserved		Reserved	Reserved	IDGND	SESEND	SESSVALID	VBUSVALID	HOSTDISCONNECT
BITS	FIELD NAME	DESCRIPTION					TYPE	RESET
7	Reserved						R	0
6	Reserved						R	0
5	Reserved						R	0
4	IDGND	Current value of UTMI+ IdGnd output. This bit is not updated if IdPullup bit is reset to 0 and for 50 ms after IdPullup is set to 1.					R	0
3	SESEND	Current value of UTMI+ SessEnd output.					R	0
2	SESSVALID	Current value of UTMI+ SessValid output. SessValid is the same as UTMI+ AValid.					R	0
1	VBUSVALID	Current value of UTMI+ VbusValid output.					R	0
0	HOSTDISCONNECT	Current value of UTMI+ Hostdisconnect output. Applicable only in host mode. Automatically reset to 0 when Low Power Mode is entered. NOTE: Reset value is '0' when host is connected. Reset value is '1' when host is disconnected.					R	0

## 7.5.21 USB\_INT\_LATCH

ADDRESS OFFSET		0x14													
PHYSICAL ADDRESS		0x14		INSTANCE	USB_SCUSB										
DESCRIPTION		<p>These bits are set by the PHY when an unmasked change occurs on the corresponding internal signal. The PHY will automatically clear all bits when the Link reads this register, or when Low Power Mode is entered. The PHY also clears this register when Serial Mode or Carkit Mode is entered regardless of the value of ClockSuspendM.</p> <p>The PHY follows the rules defined in Table 26 of the ULPI spec for setting any latch register bit. It is important to note that if register read data is returned to the Link in the same cycle that a USB Interrupt Latch bit is to be set, the interrupt condition is given immediately in the register read data and the Latch bit is not set.</p> <p>Note that it is optional for the Link to read the USB Interrupt Latch register in Synchronous Mode because the RX CMD byte already indicates the interrupt source directly</p>													
TYPE		R													
WRITE LATENCY															
7		6		5		4		3		2		1		0	
Reserved		Reserved		Reserved		IDGND_LATCH		SESEND_LATCH		SESSVALID_LATCH		VBUSVALID_LATCH		HOSTDISCONNECT_LATCH	
BITS		FIELD NAME		DESCRIPTION								TYPE		RESET	
7		Reserved										R		0	
6		Reserved										R		0	
5		Reserved										R		0	
4		IDGND_LATCH		Set to 1 by the PHY when an unmasked event occurs on IdGnd. Cleared when this register is read.								R		0	
3		SESEND_LATCH		Set to 1 by the PHY when an unmasked event occurs on SessEnd. Cleared when this register is read.								R		0	
2		SESSVALID_LATCH		Set to 1 by the PHY when an unmasked event occurs on SessValid. Cleared when this register is read. SessValid is the same as UTMI+ AValid.								R		0	
1		VBUSVALID_LATCH		Set to 1 by the PHY when an unmasked event occurs on VbusValid. Cleared when this register is read.								R		0	
0		HOSTDISCONNECT_LATCH		<p>Set to 1 by the PHY when an unmasked event occurs on Hostdisconnect. Cleared when this register is read. Applicable only in host mode.</p> <p>NOTE: As this IT is enabled by default, the reset value depends on the host status</p> <p>Reset value is '0' when host is connected.</p> <p>Reset value is '1' when host is disconnected.</p>								R		0	

## TUSB1210-Q1

SLLSEL4A – SEPTEMBER 2014 – REVISED OCTOBER 2014

[www.ti.com](http://www.ti.com)

### 7.5.22 DEBUG

ADDRESS OFFSET	0x15		
PHYSICAL ADDRESS	0x15	INSTANCE	USB_SCUSB
DESCRIPTION	Indicates the current value of various signals useful for debugging.		
TYPE	R		
WRITE LATENCY			

7	6	5	4	3	2	1	0
Reserved						LINESTATE	
BITS	FIELD NAME	DESCRIPTION				TYPE	RESET
7	Reserved					R	0
6	Reserved					R	0
5	Reserved					R	0
4	Reserved					R	0
3	Reserved					R	0
2	Reserved					R	0
1:00	LINESTATE	These signals reflect the current state of the single ended receivers. They directly reflect the current state of the DP (LineState[0]) and DM (LineState[1]) signals. Read 0x0: SE0 (LS/FS), Squelch (HS/Chirp) Read 0x1: LS: 'K' State, FS: 'J' State, HS: !Squelch, Chirp: !Squelch & HS_Differential_Receiver_Output Read 0x2: LS: 'J' State, FS: 'K' State, HS: Invalid, Chirp: !Squelch & !HS_Differential_Receiver_Output Read 0x3: SE1 (LS/FS), Invalid (HS/Chirp)				R	0x0

### 7.5.23 SCRATCH\_REG

ADDRESS OFFSET	0x16		
PHYSICAL ADDRESS	0x16	INSTANCE	USB_SCUSB
DESCRIPTION	Empty register byte for testing purposes. Software can read, write, set, and clear this register and the PHY functionality will not be affected.		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
SCRATCH							
BITS	FIELD NAME	DESCRIPTION				TYPE	RESET
7:00	SCRATCH	Scratch data.				RW	0x00

### 7.5.24 SCRATCH\_REG\_SET

ADDRESS OFFSET	0x17		
PHYSICAL ADDRESS	0x17	INSTANCE	USB_SCUSB
DESCRIPTION	This register doesn't physically exist. It is the same as the scratch_reg register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action).		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
SCRATCH							
BITS	FIELD NAME	DESCRIPTION				TYPE	RESET
7:00	SCRATCH					RW	0x00

### 7.5.25 SCRATCH\_REG\_CLR

ADDRESS OFFSET	0x18		
PHYSICAL ADDRESS	0x18	INSTANCE	USB_SCUSB
DESCRIPTION	This register doesn't physically exist. It is the same as the scratch_reg with read/clear-only property (write '1' to clear a particular bit, a write '0' has no-action).		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
SCRATCH							
BITS	FIELD NAME	DESCRIPTION				TYPE	RESET
7:00	SCRATCH					RW	0x00



## TUSB1210-Q1

SLLSEL4A – SEPTEMBER 2014 – REVISED OCTOBER 2014

www.ti.com

### 7.5.26 VENDOR\_SPECIFIC1

ADDRESS OFFSET		0x3D					
PHYSICAL ADDRESS		0x3D		INSTANCE		USB_SCUSB	
DESCRIPTION		Power Control register .					
TYPE		RW					
WRITE LATENCY							
7	6	5	4	3	2	1	0
SPARE	MNTR_VUSBIN_OK_EN	ID_FLOAT_EN	ID_RES_EN	BVALID_FALL	BVALID_RISE	SPARE	ABNORMALSTRESS_EN
BITS	FIELD NAME	DESCRIPTION				TYPE	RESET
7	SPARE	Reserved. The link must never write a 1b to this bit.				RW	0
6	MNTR_VUSBIN_OK_EN	When set to 1, it enables RX CMDs for high to low or low to high transitions on MNTR_VUSBIN_OK. This bit is provided for debugging purposes.				RW	0
5	ID_FLOAT_EN	When set to 1, it enables RX CMDs for high to low or low to high transitions on ID_FLOAT. This bit is provided for debugging purposes.				RW	0
4	ID_RES_EN	When set to 1, it enables RX CMDs for high to low or low to high transitions on ID_RESA, ID_RESB and ID_RESC. This bit is provided for debugging purposes.				RW	0
3	BVALID_FALL	Enables RX CMDs for high to low transitions on BVALID. When BVALID changes from high to low, the USB TRANS will send an RX CMD to the link with the alt_int bit set to 1b.  This bit is optional and is not necessary for OTG devices. This bit is provided for debugging purposes. Disabled by default.				RW	0
2	BVALID_RISE	Enables RX CMDs for low to high transitions on BVALID. When BVALID changes from low to high, the USB Trans will send an RX CMD to the link with the alt_int bit set to 1b.  This bit is optional and is not necessary for OTG devices. This bit is provided for debugging purposes. Disabled by default.				RW	0
1	SPARE	Reserved. The link must never write a 1b to this bit.				RW	0
0	ABNORMALSTRESS_EN	When set to 1, it enables RX CMDs for low to high and high to low transitions on ABNORMALSTRESS. This bit is provided for debugging purposes.				RW	0

### 7.5.27 VENDOR\_SPECIFIC1\_SET

ADDRESS OFFSET	0x3E		
PHYSICAL ADDRESS	0x3E	INSTANCE	USB_SCUSB
DESCRIPTION	This register doesn't physically exist. It is the same as the func_ctrl register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action).		
TYPE	RW		
WRITE LATEN CY			

7	6	5	4	3	2	1	0
SPARE	MNTR_VUSBIN_OK_EN	ID_FLOAT_EN	ID_RES_EN	BVALID_FALL	BVALID_RISE	SPARE	ABNORMALSTRESS_EN
BITS	FIELD NAME		DESCRIPTION			TYPE	RESET
7	SPARE					RW	0
6	MNTR_VUSBIN_OK_EN					RW	0
5	ID_FLOAT_EN					RW	0
4	ID_RES_EN					RW	0
3	BVALID_FALL					RW	0
2	BVALID_RISE					RW	0
1	SPARE					RW	0
0	ABNORMALSTRESS_EN					RW	0

## TUSB1210-Q1

SLLSEL4A – SEPTEMBER 2014 – REVISED OCTOBER 2014

[www.ti.com](http://www.ti.com)

### 7.5.28 VENDOR\_SPECIFIC1\_CLR

ADDRESS OFFSET		0x3F					
PHYSICAL ADDRESS		0x3F		INSTANCE		USB_SCUSB	
DESCRIPTION		This register doesn't physically exist. It is the same as the func_ctrl register with read/clear-only property (write '1' to clear a particular bit, a write '0' has no-action).					
TYPE		RW					
WRITE LATENCY							
7	6	5	4	3	2	1	0
SPARE	MNTR_VUSBIN_OK_EN	ID_FLOAT_EN	ID_RES_EN	BVALID_FALL	BVALID_RISE	SPARE	ABNORMALSTRESS_EN
BITS	FIELD NAME		DESCRIPTION			TYPE	RESET
7	SPARE					RW	0
6	MNTR_VUSBIN_OK_EN					RW	0
5	ID_FLOAT_EN					RW	0
4	ID_RES_EN					RW	0
3	BVALID_FALL					RW	0
2	BVALID_RISE					RW	0
1	SPARE					RW	0
0	ABNORMALSTRESS_EN					RW	0

## 7.5.29 VENDOR\_SPECIFIC2

ADDRESS OFFSET		0x80													
PHYSICAL ADDRESS		0x80		INSTANCE		USB_SCUSB									
DESCRIPTION		Eye diagram programmability and DP/DM swap control .													
TYPE		RW													
WRITE LATENCY															
7		6		5		4		3		2		1		0	
SPARE		DATAPOLARITY		ZHSDRV				IHSTX							
BITS		FIELD NAME		DESCRIPTION								TYPE		RESET	
7		SPARE										RW		0	
6		DATAPOLARITY		Control data polarity on dp/dm								RW		1	
5:04		ZHSDRV		High speed output impedance configuration for eye diagram tuning : 00 45.455 Ω 01 43.779 Ω 10 42.793 Ω 11 42.411 Ω								RW		0x0	
3:00		IHSTX		High speed output drive strength configuration for eye diagram tuning : 0000 17.928 mA 0001 18.117 mA 0010 18.306 mA 0011 18.495 mA 0100 18.683 mA 0101 18.872 mA 0110 19.061 mA 0111 19.249 mA 1000 19.438 mA 1001 19.627 mA 1010 19.816 mA 1011 20.004 mA 1100 20.193 mA 1101 20.382 mA 1110 20.570 mA 1111 20.759 mA IHSTX[0] is also the AC BOOST enable IHSTX[0] = 0 à AC BOOST is disabled IHSTX[0] = 1 à AC BOOST is enabled								RW		0x1	

**TUSB1210-Q1**

SLLSEL4A – SEPTEMBER 2014 – REVISED OCTOBER 2014

[www.ti.com](http://www.ti.com)
**7.5.30 VENDOR\_SPECIFIC2\_SET**

ADDRESS OFFSET		0x81					
PHYSICAL ADDRESS		0x81		INSTANCE		USB_SCUSB	
DESCRIPTION		This register doesn't physically exist. It is the same as the VENDOR_SPECIFIC1 register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action).					
TYPE		RW					
WRITE LATENCY							
7	6	5	4	3	2	1	0
SPARE	DATAPOLARITY	ZHSDRV		IHSTX			

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	SPARE		RW	0
6	DATAPOLARITY		RW	1
5:04	ZHSDRV		RW	0x0
3:00	IHSTX		RW	0x1

**7.5.31 VENDOR\_SPECIFIC2\_CLR**

ADDRESS OFFSET		0x82					
PHYSICAL ADDRESS		0x82		INSTANCE		USB_SCUSB	
DESCRIPTION		This register doesn't physically exist. It is the same as the VENDOR_SPECIFIC1 register with read/clear-only property (write '1' to clear a particular bit, a write '0' has no-action).					
TYPE		RW					
WRITE LATENCY							
7	6	5	4	3	2	1	0
SPARE	DATAPOLARITY	ZHSDRV		IHSTX			

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	SPARE		RW	0
6	DATAPOLARITY		RW	1
5:04	ZHSDRV		RW	0x0
3:00	IHSTX		RW	0x1

### 7.5.32 VENDOR\_SPECIFIC1\_STS

ADDRESS OFFSET		0x83					
PHYSICAL ADDRESS		0x83		INSTANCE	USB_SCUSB		
DESCRIPTION		Indicates the current value of the interrupt source signal.					
TYPE		R					
WRITE LATENCY							
7	6	5	4	3	2	1	0
Reserved	MNTR_VUSBIN_OK_STS	ABNORMALSTRESS_STS	ID_FLOAT_STS	ID_RESC_STS	ID_RESB_STS	ID_RESA_STS	BVALID_STS

<b>BITS</b>	<b>FIELD NAME</b>	<b>DESCRIPTION</b>	<b>TYPE</b>	<b>RESET</b>
7	Reserved		R	0
6	MNTR_VUSBIN_OK_STS	Current value of MNTR_VUSBIN_OK output	R	0
5	ABNORMALSTRESS_STS	Current value of ABNORMALSTRESS output	R	0
4	ID_FLOAT_STS	Current value of ID_FLOAT output	R	0
3	ID_RESC_STS	Current value of ID_RESC output	R	0
2	ID_RESB_STS	Current value of ID_RESB output	R	0
1	ID_RESA_STS	Current value of ID_RESA output	R	0
0	BVALID_STS	Current value of VB_SESS_VLD output	R	0

## TUSB1210-Q1

SLLSEL4A – SEPTEMBER 2014 – REVISED OCTOBER 2014

[www.ti.com](http://www.ti.com)

### 7.5.33 VENDOR\_SPECIFIC1\_LATCH

ADDRESS OFFSET		0x84					
PHYSICAL ADDRESS		0x84	INSTANCE			USB_SCUSB	
DESCRIPTION		These bits are set by the PHY when an unmasked change occurs on the corresponding internal signal. The PHY will automatically clear all bits when the Link reads this register, or when Low Power Mode is entered. The PHY also clears this register when Serial mode is entered regardless of the value of ClockSuspendM.  The PHY follows the rules defined in Table 26 of the ULPI spec for setting any latch register bit.					
TYPE		R					
WRITE LATENCY							
7	6	5	4	3	2	1	0
Reserved	MNTR_VUSBIN_OK_LATCH	ABNORMALSTRESS_LATCH	ID_FLOAT_LATCH	ID_RESC_LATCH	ID_RESB_LATCH	ID_RESA_LATCH	BVALID_LATCH

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		R	0
6	MNTR_VUSBIN_OK_LATCH	Set to 1 when an unmasked event occurs on MNTR_VUSBIN_OK_LATCH. Clear on read register.	R	0
5	ABNORMALSTRESS_LATCH	Set to 1 when an unmasked event occurs on ABNORMALSTRESS. Clear on read register.	R	0
4	ID_FLOAT_LATCH	Set to 1 when an unmasked event occurs on ID_FLOAT. Clear on read register.	R	0
3	ID_RESC_LATCH	Set to 1 when an unmasked event occurs on ID_RESC. Clear on read register.	R	0
2	ID_RESB_LATCH	Set to 1 when an unmasked event occurs on ID_RESB. Clear on read register.	R	0
1	ID_RESA_LATCH	Set to 1 when an unmasked event occurs on ID_RESA. Clear on read register.	R	0
0	BVALID_LATCH	Set to 1 when an unmasked event occurs on VB_SESS_VLD. Clear on read register.	R	0

**7.5.34 VENDOR\_SPECIFIC3**

ADDRESS OFFSET		0x85							
PHYSICAL ADDRESS		0x85		INSTANCE	USB_SCUSB				
DESCRIPTION									
TYPE		RW							
WRITE LATENCY									
7		6		5	4	3	2	1	0
RESERVED		SOF_EN		CPEN_OD	CPEN_ODOS	IDGND_DRV	VUSB3V3_VSEL		
BITS	FIELD NAME	DESCRIPTION						TYPE	RESET
7	Reserved							RW	0
6	SOF_EN	0: HS USB SOF detector disabled.  1: Enable HS USB SOF detection when PHY is set in device mode.  SOF are output on CPEN pin. HS USB SOF (start-of-frame) output clock is available on CPEN pin when this bit is set. HS USB SOF packet rate is 8 kHz.  This bit is provided for debugging purpose only. It must never been write to '1' in functional mode						RW	0
5	CPEN_OD	This bit has no effect when CPEN_ODOS = '0', else :  0: CPEN pad is in OS (Open Source) mode.  In this case CPEN pin has an internal NMOS driver, and will be active LOW.  Externally there should be a pullup resistor on CPEN (min 1kohm) to a supply voltage (max 3.6V).  1: CPEN pad is in OD (Open Drain) mode  In this case CPEN pin has an internal PMOS driver, and will be active HIGH.  Externally there should be a pull-down resistor on CPEN (min 1 kΩ to GND.						RW	0
4	CPEN_ODOS	Mode selection bit for CPEN pin.  0 : CPEN pad is in CMOS mode  1: CPEN pad is in OD (Open Drain) or OS (Open Source) mode (controlled by CPEN_OD bit)						RW	0
3	IDGND_DRV	Drives ID pin to ground						RW	0x0
2:00	VUSB3V3_VSEL	000 VRUSB3P1V = 2.5 V 001 VRUSB3P1V = 2.75 V 010 VRUSB3P1V = 3.0 V 011 VRUSB3P1V = 3.10 V (default) 100 VRUSB3P1V = 3.20 V 101 VRUSB3P1V = 3.30 V 110 VRUSB3P1V = 3.40 V 111 VRUSB3P1V = 3.50 V						RW	0x3



## TUSB1210-Q1

SLLSEL4A – SEPTEMBER 2014 – REVISED OCTOBER 2014

[www.ti.com](http://www.ti.com)

### 7.5.35 VENDOR\_SPECIFIC3\_SET

ADDRESS OFFSET		0x86						
PHYSICAL ADDRESS		0x86		INSTANCE		USB_SCUSB		
DESCRIPTION								
TYPE		RW						
WRITE LATENCY								
7	6	5	4	3	2	1	0	
RESERVED	SOF_EN	CPEN_OD	CPEN_ODOS	IDGND_DRV	VUSB3V3_VSEL			
BITS	FIELD NAME		DESCRIPTION			TYPE	RESET	
7	Reserved					RW	0	
6	SOF_EN					RW	0	
5	CPEN_OD					RW	0	
4	CPEN_ODOS					RW	0	
3	IDGND_DRV					RW	0x0	
2:00	VUSB3V3_VSEL					RW	0x3	

### 7.5.36 VENDOR\_SPECIFIC3\_CLR

ADDRESS OFFSET		0x87					
PHYSICAL ADDRESS		0x87		INSTANCE	USB_SCUSB		
DESCRIPTION							
TYPE		RW					
WRITE LATENCY							
7	6	5	4	3	2	1	0
RESERVED	SOF_EN	CPEN_OD	CPEN_ODOS	IDGND_DRV	VUSB3V3_VSEL		
BITS	FIELD NAME		DESCRIPTION			TYPE	RESET
7	Reserved					RW	0
6	SOF_EN					RW	0
5	CPEN_OD					RW	0
4	CPEN_ODOS					RW	0
3	IDGND_DRV					RW	0x0
2:00	VUSB3V3_VSEL					RW	0x3

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

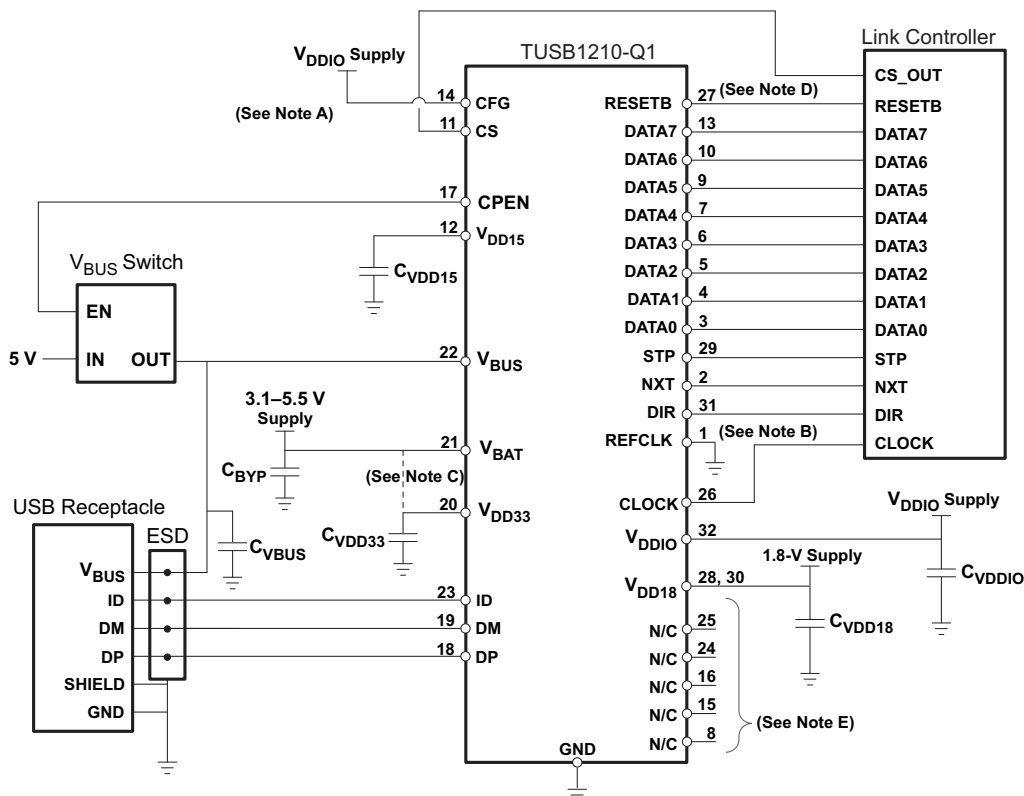
### 8.1 Application Information

Figure 5 shows the suggested application diagram (Host or OTG, ULPI input-clock mode).

### 8.2 Typical Application

#### 8.2.1 Host or OTG, ULPI Input Clock Mode Application

Figure 5 shows a suggested application diagram for TUSB1210-Q1 in the case of ULPI input-clock mode (60 MHz ULPI clock is provided by link processor), in Host or OTG application. Note this is just one example, it is of course possible to operate as HOST or OTG while also in ULPI output-clock mode.



- A. Pin 11 (CS) : can be tied high to  $V_{IO}$  if CS\_OUT pin unavailable; Pin 14 (CFG) : tie-high is Don't Care since ULPI clock is used in input mode
- B. Pin 1 (REFCLK) : must be tied low
- C. Ext 3 V supply supported
- D. Pin 27 (RESETB) can be tied to  $V_{DDIO}$  if unused.
- E. Pins labeled N/C (no-connect) are truly no-connect, and can be tied or left floating.

**Figure 5. Host or OTG, ULPI Input Clock Mode Application Diagram**

## TUSB1210-Q1

SLLSEL4A – SEPTEMBER 2014 – REVISED OCTOBER 2014

www.ti.com

### Typical Application (continued)

#### 8.2.1.1 Design Requirements

**Table 9. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
$V_{BAT}$	3.3 V
$V_{DDIO}$	1.8 V
$V_{BUS}$	5.0 V
USB Support	HS, FS, LS
USB On the Go (OTG)	Yes
Clock Sources	60 MHz Clock

#### 8.2.1.2 Detailed Design Procedure

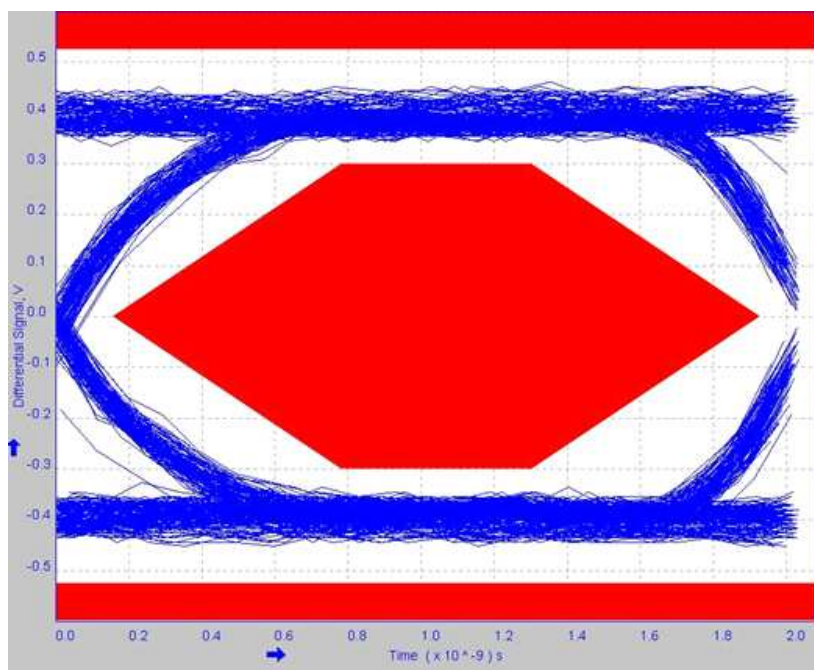
Connect the TUSB1210 device as is shown in [Figure 5](#).

Follow the Board Guidelines of the Application Report, [SWCA124](#).

##### 8.2.1.2.1 Unused Pins Connection

- **VBUS:** Input. Recommended to tie to GND if unused. However leaving  $V_{BUS}$  floating is also acceptable since internally there is an 80 k $\Omega$  resistance to ground.
- **REFCLK:** Input. If REFCLK is unused, and 60 MHz clock is provided by MODEM (60 MHz should be connected to CLOCK pin in this case) then tie REFCLK to GND.
- **CFG:** Tie to GND if REFCLK is 19.2MHz, or tie to  $V_{DDIO}$  if REFCLK is 26 MHz. Tie to either GND or  $V_{DDIO}$  (doesn't matter which) if REFCLK not used (i.e., ULPI input clock configuration).

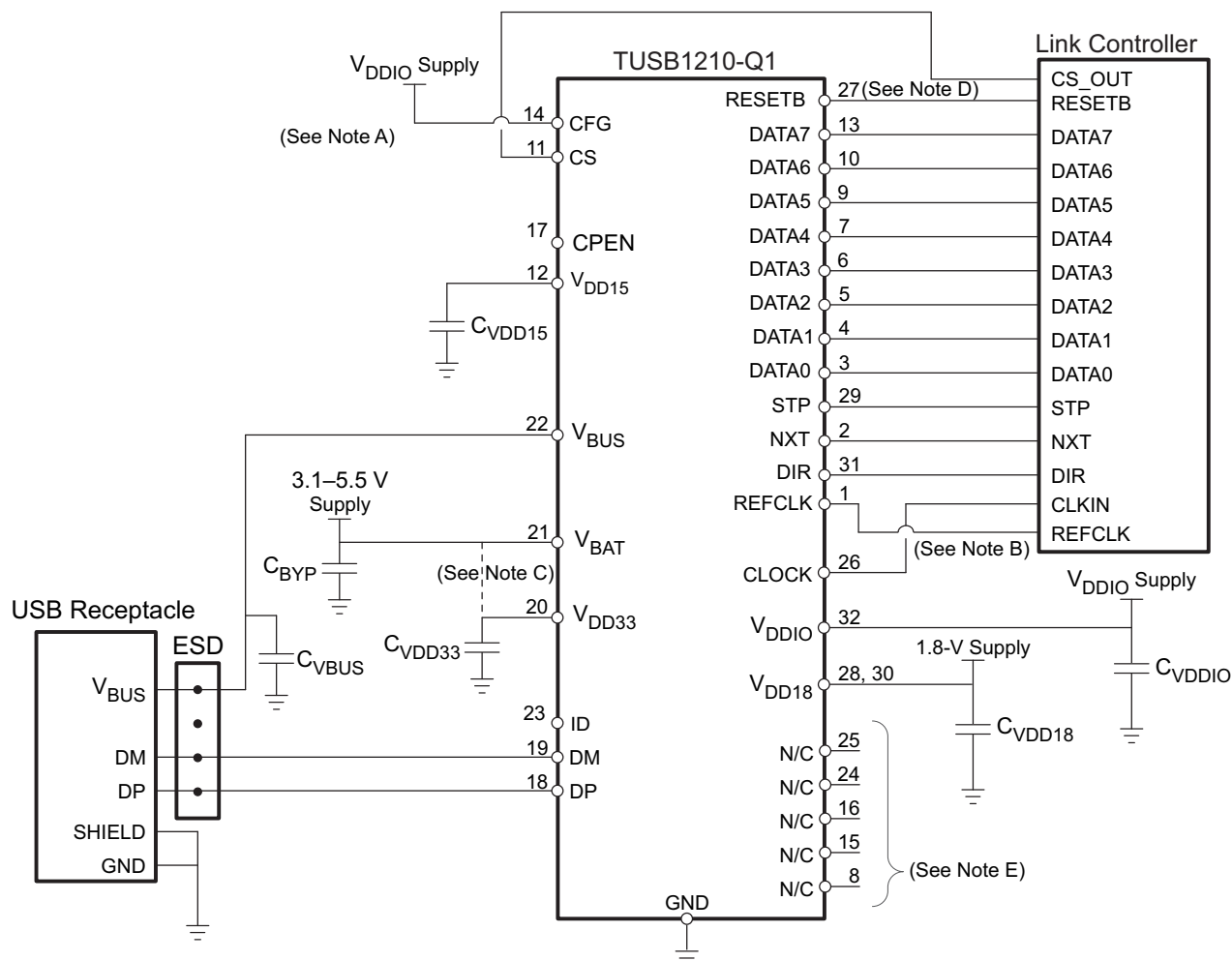
#### 8.2.1.3 Application Curve



**Figure 6. High-Speed Eye Diagram**

## 8.2.2 Device, ULPI Output Clock Mode Application

Figure 7 shows a suggested application diagram for TUSB1210-Q1 in the case of ULPI output clock mode (60 MHz ULPI clock is provided by TUSB1210-Q1, while link processor or another external circuit provides REFCLK), in Device mode application. Note this is just one example, it is of course possible to operate as Device while also in ULPI input-clock mode. Refer also to Figure 5.



- A. Pin 11 (CS) : can be tied high to  $V_{IO}$  if CS\_OUT pin unavailable; Pin 14 (CFG) : Tied to  $V_{DDIO}$  for 26MHz REFCLK mode here, tie to GND for 19.2MHz mode.
- B. Pin 1 (REFCLK) : connect to external 3.3V square-wave reference clock
- C. Ext 3 V supply supported
- D. Pin 27 (RESETB) can be tied to  $V_{DDIO}$  if unused.
- E. Pins labeled N/C (no-connect) are truly no-connect, and can be tied or left floating.

**Figure 7. Device, ULPI Output Clock Mode Application Diagram**

## TUSB1210-Q1

SLLSEL4A – SEPTEMBER 2014 – REVISED OCTOBER 2014

www.ti.com

### 8.2.2.1 Design Requirements

**Table 10. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
$V_{BAT}$	3.3 V
$V_{DDIO}$	1.8 V
$V_{BUS}$	5.0 V
USB Support	HS, FS, LS
Clock Sources	26 MHz or 19.2 MHz Oscillator

### 8.2.2.2 Detailed Design Procedure

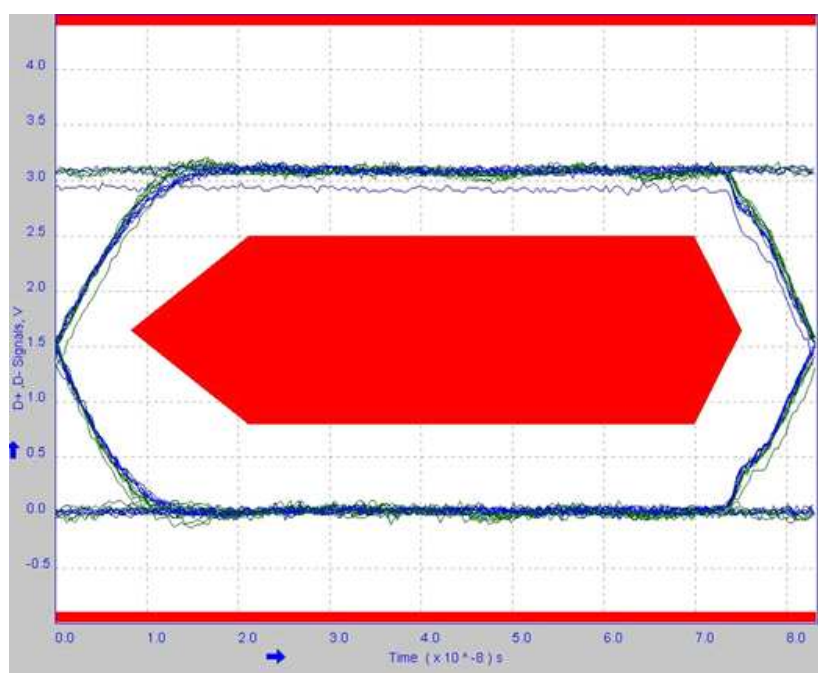
Connect the TUSB1210 device as is shown in [Figure 7](#).

Follow the Board Guidelines of the Application Report, [SWCA124](#).

#### 8.2.2.2.1 Unused Pins Connection

- **ID:** Input. Leave floating if unused or TUSB1210-Q1 is Device mode only. Tie to GND through  $R_{ID} < 1\text{ k}\Omega$  if Host mode.
- **REFCLK:** Input. If REFCLK is unused, and 60 MHz clock is provided by MODEM (60 MHz should be connected to CLOCK pin in this case) then tie REFCLK to GND.
- **CFG:** Tie to GND if REFCLK is 19.2MHz, or tie to  $V_{DDIO}$  if REFCLK is 26 MHz. Tie to either GND or  $V_{DDIO}$  (doesn't matter which) if REFCLK not used (i.e., ULPI input clock configuration).

### 8.2.2.3 Application Curve



**Figure 8. Full-Speed Eye Diagram**

### 8.3 External Components

**Table 11. TUSB1210-Q1 External Components**

FUNCTION	COMPONENT	REFERENCE	VALUE	NOTE	LINK
V <sub>DDIO</sub>	Capacitor	CVDDIO	100 nF	Suggested value, application dependent	<a href="#">Figure 5</a>
V <sub>DD33</sub>	Capacitor	CVDD33	2.2 $\mu$ F	Range: [0.45 $\mu$ F : 6.5 $\mu$ F] , ESR = [0 : 600 m $\Omega$ ] for f > 10 kHz	<a href="#">Figure 5</a>
V <sub>DD15</sub>	Capacitor	CVDD15	2.2 $\mu$ F	Range: [0.45 $\mu$ F : 6.5 $\mu$ F] , ESR = [0 : 600 m $\Omega$ ] for f > 10 kHz	<a href="#">Figure 5</a>
V <sub>DD18</sub>	Capacitor	Ext 1.8V supply	100 nF	Suggested value, application dependent	<a href="#">Figure 5</a>
		CVDD18			
V <sub>BAT</sub>	Capacitor	CBYP	100 nF <sup>(1)</sup>	Range: [0.45 $\mu$ F : 6.5 $\mu$ F] , ESR = [0 : 600 m $\Omega$ ] for f > 10 kHz	<a href="#">Figure 5</a>
V <sub>BUS</sub>	Capacitor	CVBUS	See <a href="#">Table 12</a>	Place close to USB connector	<a href="#">Figure 5</a>

(1) Recommended value but 2.2  $\mu$ F may be sufficient in some applications

**Table 12. TUSB1210-Q1 V<sub>BUS</sub> Capacitors**

FUNCTION	COMPONENT	REFERENCE	VALUE	NOTE	LINK
VBUS - HOST	Capacitor	CVBUS	>120 $\mu$ F		<a href="#">Figure 5</a>
VBUS – DEVICE	Capacitor	CVBUS	4.7 $\mu$ F	Range: 1.0 $\mu$ F to 10.0 $\mu$ F	<a href="#">Figure 5</a>
VBUS - OTG	Capacitor	CVBUS	4.7 $\mu$ F	Range: 1.0 $\mu$ F to 6.5 $\mu$ F	<a href="#">Figure 5</a>

## TUSB1210-Q1

SLLSEL4A – SEPTEMBER 2014 – REVISED OCTOBER 2014

www.ti.com

## 9 Power Supply Recommendations

$V_{BUS}$ , and  $V_{BAT}$ , and  $V_{DDIO}$ , are needed for power the TUSB1210-Q1. Recommended operation is for  $V_{BAT}$  to be present before  $V_{DDIO}$ . Applying  $V_{DDIO}$  before  $V_{BAT}$  to TUSB1210 is not recommended as there is a diode from  $V_{DDIO}$  to  $V_{BAT}$  which will be forward biased when  $V_{DDIO}$  is present but  $V_{BAT}$  is not present. TUSB1210-Q1 does not strictly require  $V_{BUS}$  to function.

### 9.1 TUSB1210 Power Supply

- The  $V_{DDIO}$  pins of the TUSB1210-Q1 supply 1.8 V (nominal) power to the core of the TUSB1210-Q1. This power rail can be isolated from all other power rails by a ferrite bead to reduce noise.
- The  $V_{BAT}$  pin of the TUSB1210-Q1 supply 3.3 V (nominal) power rail to the TUSB1210-Q1. This power rail can be isolated from all other power rails by a ferrite bead to reduce noise.
- The  $V_{BUS}$  pin of the TUSB1210-Q1 supply 5.0 V (nominal) power rail to the TUSB1210-Q1. This pin is normally connected to the  $V_{BUS}$  pin of the USB connector.
- The  $V_{BUS}$  pin of the TUSB1210-Q1 supply 5.0 V (nominal) power rail to the TUSB1210-Q1. This pin is normally connected to the  $V_{BUS}$  pin of the USB connector.

### 9.2 Ground

It is recommended that almost one board ground plane be used in the design. This provides the best image plane for signal traces running above the plane. An earth or chassis ground is implemented only near the USB port connectors on a different plane for EMI and ESD purposes.

### 9.3 Power Providers

Table 13 is a summary of TUSB1210-Q1 power providers.

Table 13. Power Providers<sup>(1)</sup>

NAME	USAGE	TYPE	TYPICAL VOLTAGE (V)	MAXIMUM CURRENT (mA)
$V_{DD15}$	Internal	LDO	1.5	50
$V_{DD18}$	External	LDO	1.8	30
$V_{DD33}$	Internal	LDO	3.1	15

- (1)  $V_{DD33}$  may be supplied externally, or by shorting the  $V_{DD33}$  pin to  $V_{BAT}$  pin provided  $V_{BAT}$  min is in range [3.2 V : 3.6 V]. Note that the  $V_{DD33}$  LDO will always power-on when the chip is enabled, irrespective of whether  $V_{DD33}$  is supplied externally or not. In the case the  $V_{DD33}$  pin is not supplied externally in the application, the electrical specs for this LDO are provided below.

### 9.4 Power Modules

#### 9.4.1 $V_{DD33}$ Regulator

The  $V_{DD33}$  internal LDO regulator powers the USB PHY, charger detection, and OTG functions of the USB subchip inside TUSB1210-Q1. [Power Characteristics](#) describes the regulator characteristics.

$V_{DD33}$  regulator takes its power from  $V_{BAT}$ .

Since the USB2.0 standard requires data lines to be biased with pullups biased from a supply greater than 3 V, and since  $V_{DD33}$  regulator has an inherent voltage drop from its input,  $V_{BAT}$ , to its regulated output, TUSB1210-Q1 will not meet USB 2.0 Standard if operated from a battery whose voltage is lower than 3.3 V.

#### 9.4.2 $V_{DD18}$ Supply

The  $V_{DD18}$  supply is powered externally at the  $V_{DD18}$  pin. See [Table 11](#) for external components.

#### 9.4.3 $V_{DD15}$ Regulator

The  $V_{DD15}$  internal LDO regulator powers the USB subchip inside TUSB1210-Q1. [Power Characteristics](#) describes the regulator characteristics.

## 9.5 Power Consumption

Table 14 describes the power consumption depending on the use cases.

### NOTE

The typical power consumption is obtained in the nominal operating conditions and with the TUSB1210-Q1 standalone.

**Table 14. Power Consumption**

MODE	CONDITIONS	SUPPLY	TYPICAL CONSUMPTION	UNIT
OFF Mode	$V_{BAT} = 3.6\text{ V}$ , $V_{DDIO} = 1.8\text{ V}$ , $V_{DD18} = 1.8\text{ V}$ , $CS = 0\text{ V}$	$I_{VBAT}$	8	$\mu\text{A}$
		$I_{VDDIO}$	3	
		$I_{VDD18}$	5	
		$I_{TOTAL}$	16	
Suspend Mode	$V_{BUS} = 5\text{ V}$ , $V_{BAT} = 3.6\text{ V}$ , $V_{DDIO} = 1.8\text{ V}$ , No clock	$I_{VBAT}$	204	$\mu\text{A}$
		$I_{VDDIO}$	3	
		$I_{VDD18}$	3	
		$I_{TOTAL}$	210	
HS USB Operation (Synchronous Mode)	$V_{BAT} = 3.6\text{ V}$ , $V_{DDIO} = 1.8\text{ V}$ , $V_{DD18} = 1.8\text{ V}$ , active USB transfer	$I_{VBAT}$	24.6	$\text{mA}$
		$I_{VDDIO}$	1.89	
		$I_{VDD18}$	21.5	
		$I_{TOTAL}$	48	
FS USB Operation (Synchronous Mode)	$V_{BAT} = 3.6\text{ V}$ , $V_{DDIO} = 1.8\text{ V}$ , active USB transfer	$I_{VBAT}$	25.8	$\text{mA}$
		$I_{VDDIO}$	1.81	
		$I_{VDD18}$	4.06	
		$I_{TOTAL}$	31.7	
Reset Mode	$RESETB = 0\text{ V}$ , $V_{BUS} = 5\text{ V}$ , $V_{BAT} = 3.6\text{ V}$ , $V_{DDIO} = 1.8\text{ V}$ , No clock	$I_{VBAT}$	237	$\mu\text{A}$
		$I_{VDDIO}$	3	
		$I_{VDD18}$	3	
		$I_{TOTAL}$	243	



## TUSB1210-Q1

SLLSEL4A – SEPTEMBER 2014 – REVISED OCTOBER 2014

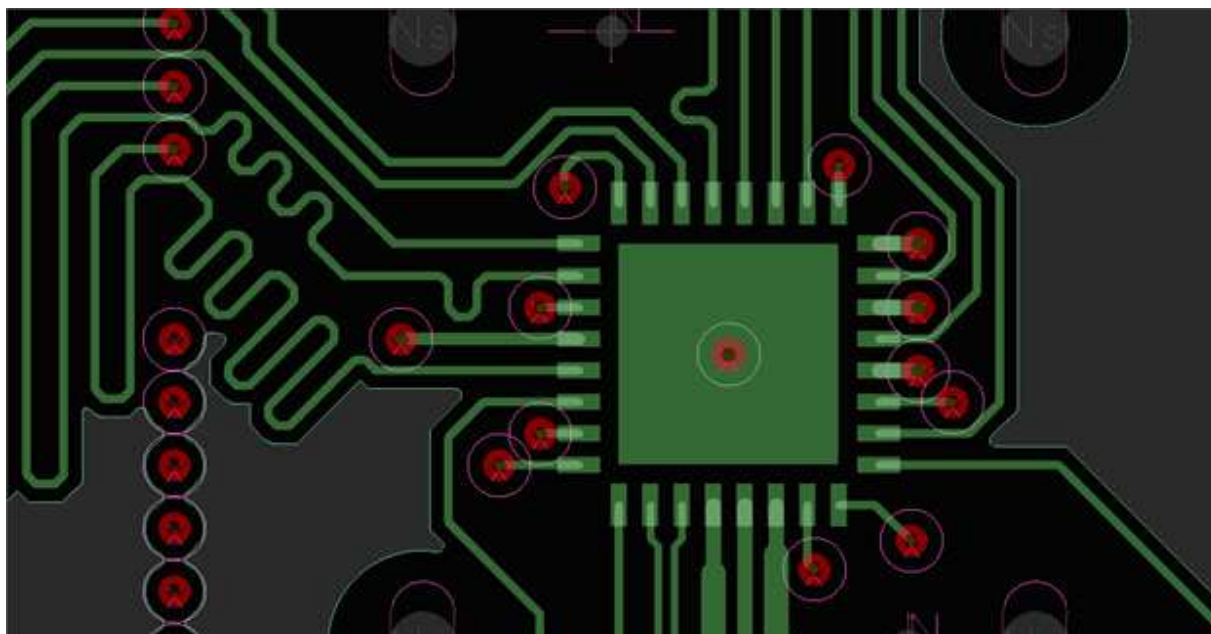
[www.ti.com](http://www.ti.com)

## 10 Layout

### 10.1 Layout Guidelines

- The  $V_{DDIO}$  pins of the TUSB1210-Q1 supply 1.8-V (nominal) power to the core of the TUSB1210-Q1. This power rail can be isolated from all other power rails by a ferrite bead to reduce noise.
- The  $V_{BAT}$  pin of the TUSB1210-Q1 supply 3.3-V (nominal) power rail to the TUSB1210-Q1. This power rail can be isolated from all other power rails by a ferrite bead to reduce noise.
- The  $V_{BUS}$  pin of the TUSB1210-Q1 supply 5-V (nominal) power rail to the TUSB1210-Q1. This pin is normally connected to the  $V_{BUS}$  pin of the USB connector.
- All power rails require 0.1  $\mu$ F decoupling capacitors for stability and noise immunity. The smaller decoupling capacitors should be placed as close to the TUSB1210-Q1 power pins as possible with an optimal grouping of two of differing values per pin.

### 10.2 Layout Example



**Figure 9. TUSB1210-Q1 Layout Example**

## 11 Device and Documentation Support

### 11.1 Documentation Support

**SLLZ066** *Silicon Errata*. Describes the known exceptions to the functional specifications for the TUSB1210-Q1.

### 11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**TI Embedded Processors Wiki** *Texas Instruments Embedded Processors Wiki*. Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

### 11.3 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.5 Glossary

#### 11.5.1 Glossary

**SLYZ022** — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

**TUSB1210-Q1**

SLLSEL4A – SEPTEMBER 2014 – REVISED OCTOBER 2014

[www.ti.com](http://www.ti.com)

## 12 Mechanical, Packaging, and Orderable Information

### 12.1 Via Channel

The T package has been specially engineered with Via Channel technology. This allows larger than normal PCB via and trace sizes and reduced PCB signal layers to be used in a PCB design with the 0.65-mm pitch package, and substantially reduces PCB costs. It allows PCB routing in only two signal layers (four layers total) due to the increased layer efficiency of the Via Channel BGA technology.

Via Channel technology implemented on the [your package] package makes it possible to build an [your device]-based product with a 4-layer PCB, but a 4-layer PCB may not meet system performance goals. Therefore, system performance using a 4-layer PCB design must be evaluated during product design.

### 12.2 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TUSB1210BRHBRQ1	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	T1210Q1	<a href="#">Samples</a>
TUSB1210BRHBTQ1	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	T1210Q1	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.



www.ti.com

**Distributor of Texas Instruments: Excellent Integrated System Limited**

Datasheet of TUSB1210BRHBRQ1 - IC TXRX USB

Contact us: [sales@integrated-circuit.com](mailto:sales@integrated-circuit.com) Website: [www.integrated-circuit.com](http://www.integrated-circuit.com)

---

**PACKAGE OPTION ADDENDUM**

---

7-Oct-2014

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TUSB1210-Q1 :**

- Catalog: [TUSB1210](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

## PACKAGE MATERIALS INFORMATION

### TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB1210BRHBRQ1	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TUSB1210BRHBTQ1	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**



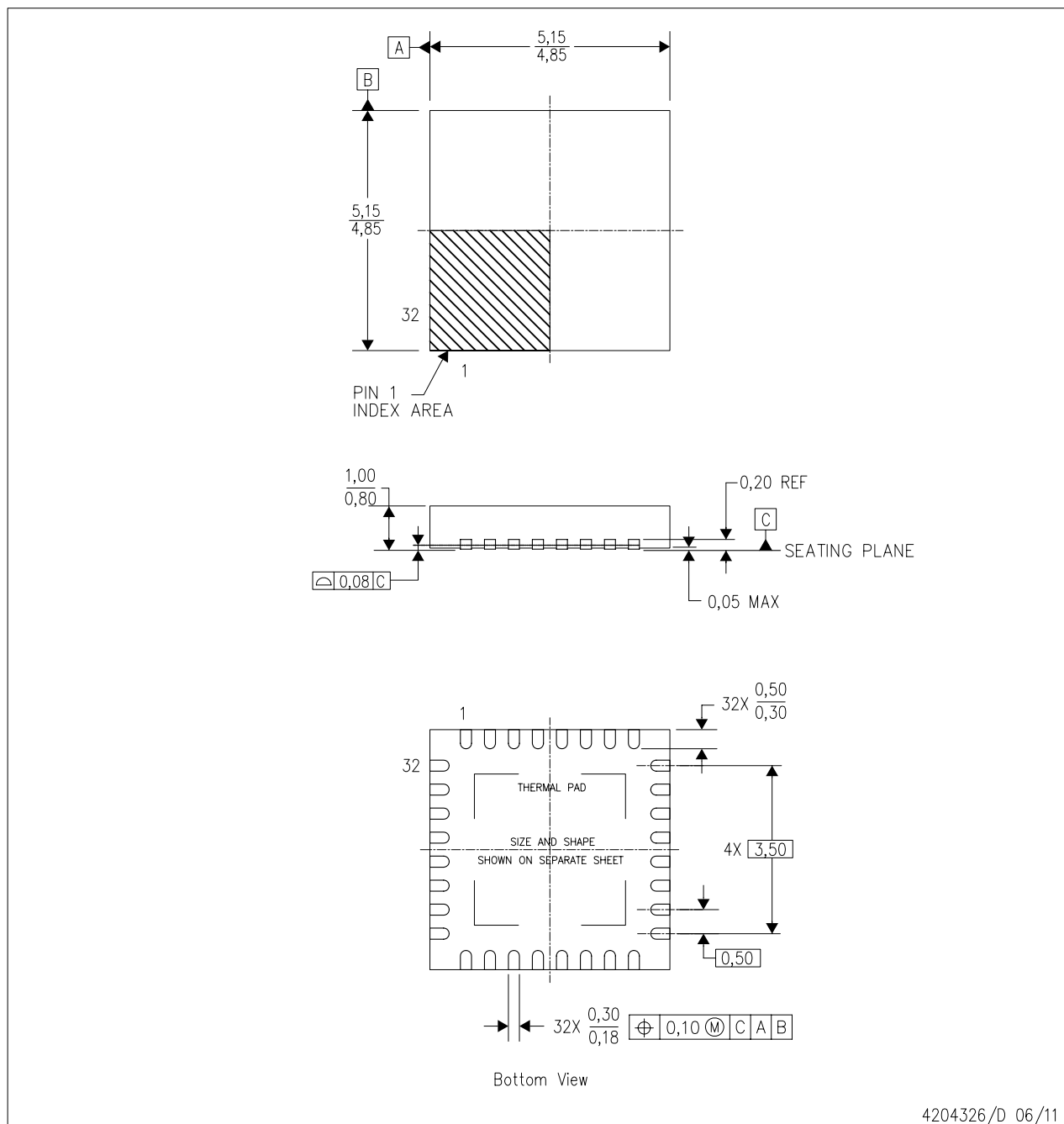
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB1210BRHBRQ1	VQFN	RHB	32	3000	367.0	367.0	35.0
TUSB1210BRHBTQ1	VQFN	RHB	32	250	210.0	185.0	35.0

## MECHANICAL DATA

RHB (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) Package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Falls within JEDEC MO-220.



## THERMAL PAD MECHANICAL DATA

RHB (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD

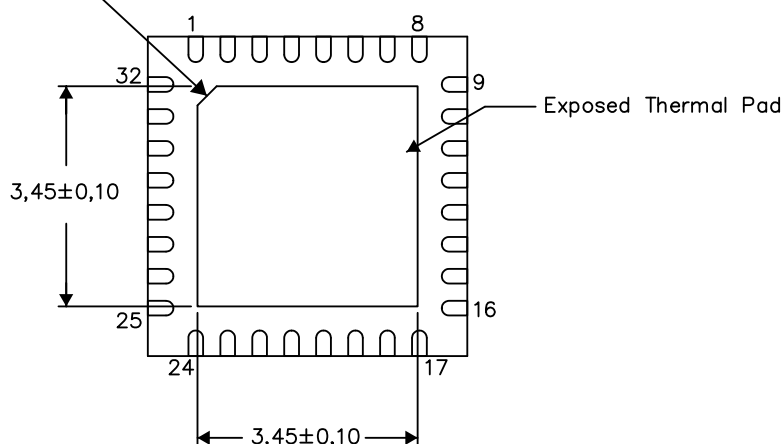
### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.

PIN 1 INDICATOR  
(OPTIONAL)



Bottom View

Exposed Thermal Pad Dimensions

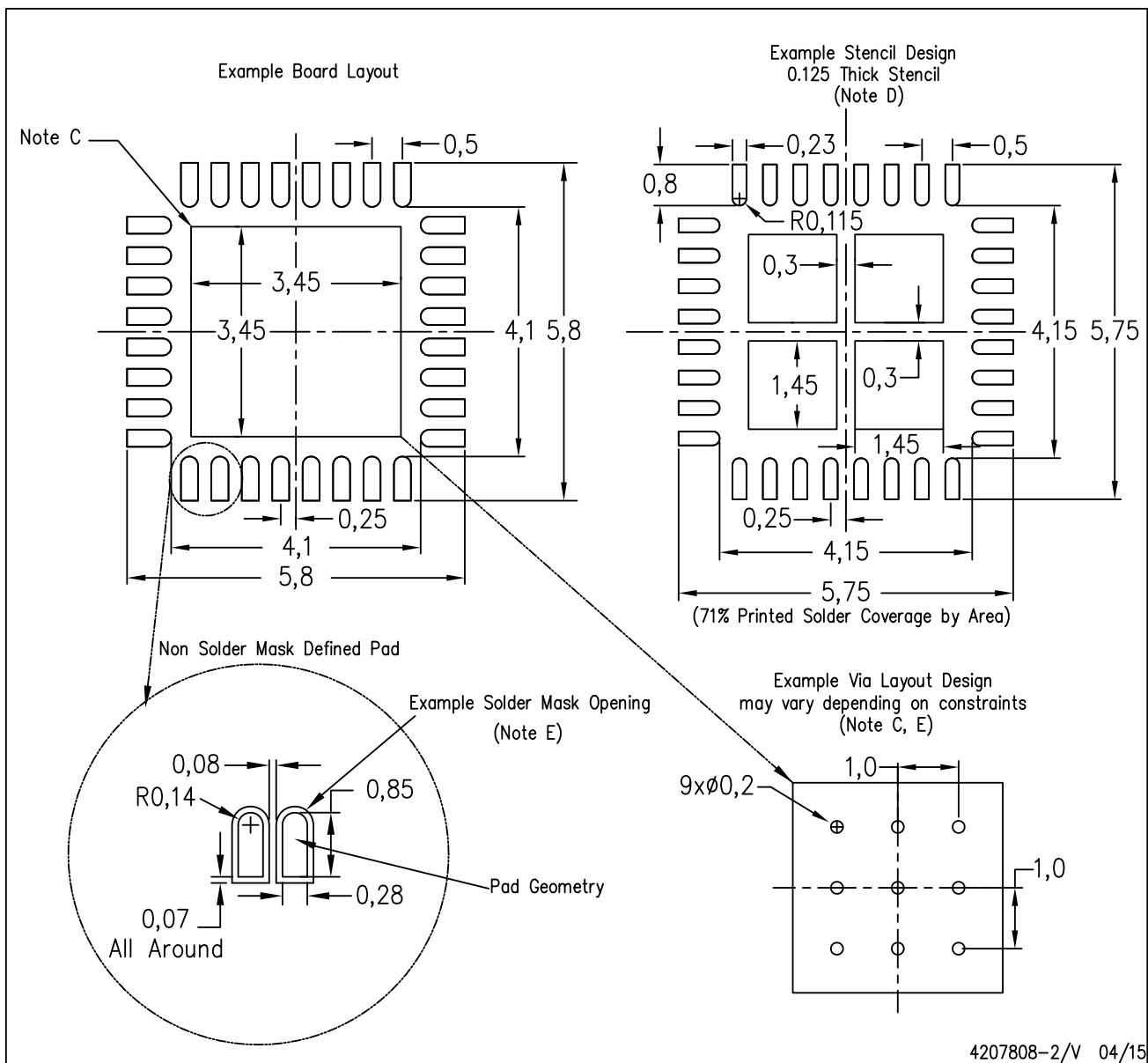
4206356-2/AC 05/15

NOTE: A. All linear dimensions are in millimeters

## LAND PATTERN DATA

RHB (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Automotive and Transportation	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)