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Texas Instruments
CSD17578Q3A

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CSD17578Q3A 30 V N-Channel NexFET™ Power MOSFETs

1 Features

- Low Q_g and Q_{gd}
- Low $R_{DS(on)}$
- Low Thermal Resistance
- Avalanche Rated
- Pb-Free
- RoHS Compliant
- Halogen Free
- SON 3.3 mm × 3.3 mm Plastic Package

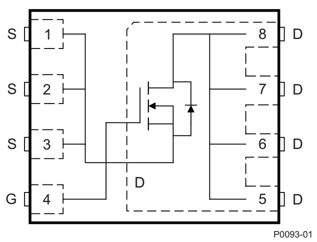
2 Applications

- Point-of-Load Synchronous Buck Converter for Applications in Networking, Telecom, and Computing Systems
- Optimized for Control FET Applications

3 Description

This 30 V, 6.3 mΩ, SON 3.3 mm × 3.3 mm NexFET™ power MOSFET is designed to minimize losses in power conversion applications.

Top View



Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	30		V
Q_g	Gate Charge Total (4.5 V)	7.9		nC
Q_{gd}	Gate Charge Gate to Drain	1.7		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 4.5 V	8.2	mΩ
		V_{GS} = 10 V	6.3	mΩ
$V_{GS(th)}$	Threshold Voltage	1.5		V

Ordering Information(1)

DEVICE	MEDIA	QTY	PACKAGE	SHIP
CSD17578Q3A	13-Inch Reel	2500	SON 3.3 x 3.3 mm Plastic Package	Tape and Reel
CSD17578Q3AT	7-Inch Reel	250		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

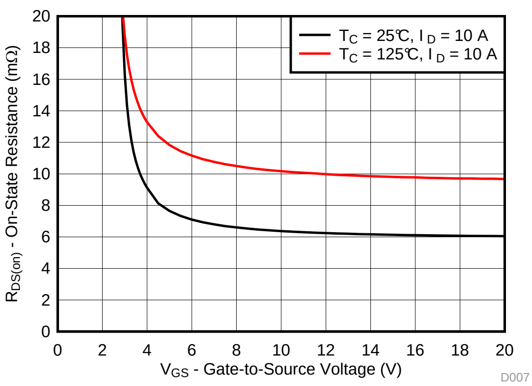
Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current (Package limited)	20	A
	Continuous Drain Current (Silicon limited), T_C = 25°C	54	
	Continuous Drain Current(1)	14	
I_{DM}	Pulsed Drain Current(2)	142	A
P_D	Power Dissipation(1)	2.5	W
	Power Dissipation, T_C = 25°C	37	
T_J, T_{stg}	Operating Junction Temperature, Storage Temperature	–55 to 150	°C
E_{AS}	Avalanche Energy, single pulse I_D = 22 A, L = 0.1 mH, R_G = 25 Ω	24	mJ

(1) Typical $R_{\theta JA}$ = 50°C/W on a 1 inch^2, 2 oz. Cu pad on a 0.06 inch thick FR4 PCB.

(2) Max $R_{\theta JC}$ = 4.2 °C/W, pulse duration ≤100 μs, duty cycle ≤1%

$R_{DS(on)}$ vs V_{GS}



Gate Charge

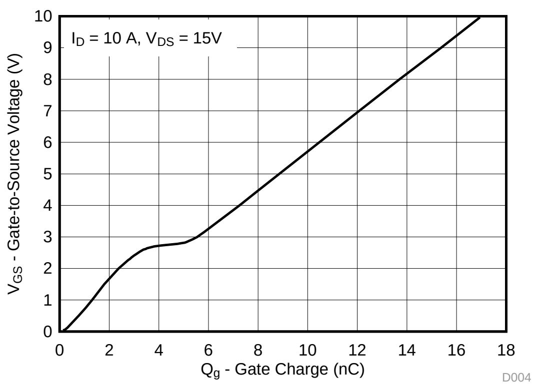


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2014) to Revision A **Page**

- Updated Power Dissipation value in *Absolute Maximum Ratings* table. 1
- Added *Community Resources* section 7
- Updated Package Dimensions drawing 8
- Updated PCB drawing. 9
- Updated Stencil Pattern drawing. 9

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

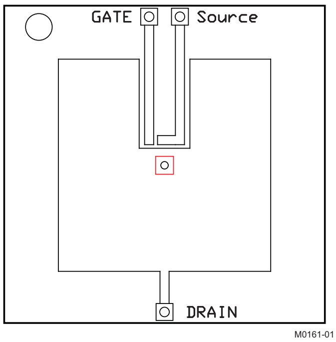
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 250 μA	30			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = 24 V			1	μA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	1.1	1.5	1.9	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 4.5 V, I_D = 10 A		8.2	9.4	mΩ
		V_{GS} = 10 V, I_D = 10 A		6.3	7.3	mΩ
g_{fs}	Transconductance	V_{DS} = 3 V, I_D = 10 A		48		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz		1150	1590	pF
C_{oss}	Output Capacitance			134	174	pF
C_{rss}	Reverse Transfer Capacitance			56	73	pF
R_G	Series Gate Resistance			1.8	3.6	Ω
Q_g	Gate Charge Total (4.5 V)	V_{DS} = 15 V, I_D = 10 A		7.9	10.3	nC
Q_g	Gate Charge Total (10 V)			17.1	22.2	nC
Q_{gd}	Gate Charge Gate-to-Drain			1.7		nC
Q_{gs}	Gate Charge Gate-to-Source			3.3		nC
$Q_{g(th)}$	Gate Charge at V_{th}			1.6		nC
Q_{oss}	Output Charge	V_{DS} = 15 V, V_{GS} = 0 V		4.2		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 15 V, V_{GS} = 10 V, I_{DS} = 10 A, R_G = 0 Ω		2		ns
t_r	Rise Time			6		ns
$t_{d(off)}$	Turn Off Delay Time			13		ns
t_f	Fall Time			1		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_{SD} = 10 A, V_{GS} = 0 V		0.8	1.0	V
Q_{rr}	Reverse Recovery Charge	V_{DS}= 15 V, I_F = 10 A, di/dt = 300 A/μs		4.4		nC
t_{rr}	Reverse Recovery Time			6		ns

5.2 Thermal Information

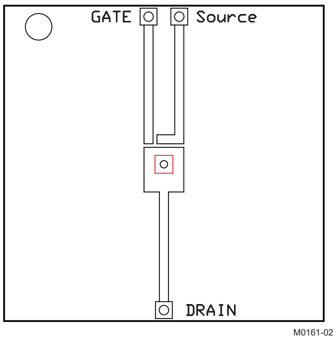
(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{θJC}$	Junction-to-Case Thermal Resistance (1)			4.2	°C/W
$R_{θJA}$	Junction-to-Ambient Thermal Resistance (1)(2)			60	°C/W

(1) $R_{θJC}$ is determined with the device mounted on a 1 inch^2 (6.45 cm^2), 2 oz. (0.071 mm thick) Cu pad on a 1.5 inches × 1.5 inches (3.81 cm × 3.81 cm), 0.06 inch (1.52 mm) thick FR4 PCB. $R_{θJC}$ is specified by design, whereas $R_{θJA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1 inch^2 (6.45 cm^2), 2 oz. (0.071 mm thick) Cu.



Max $R_{\theta JA}$ = 60°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 145°C/W when mounted on a minimum pad area of 2-oz. (0.071-mm thick) Cu.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

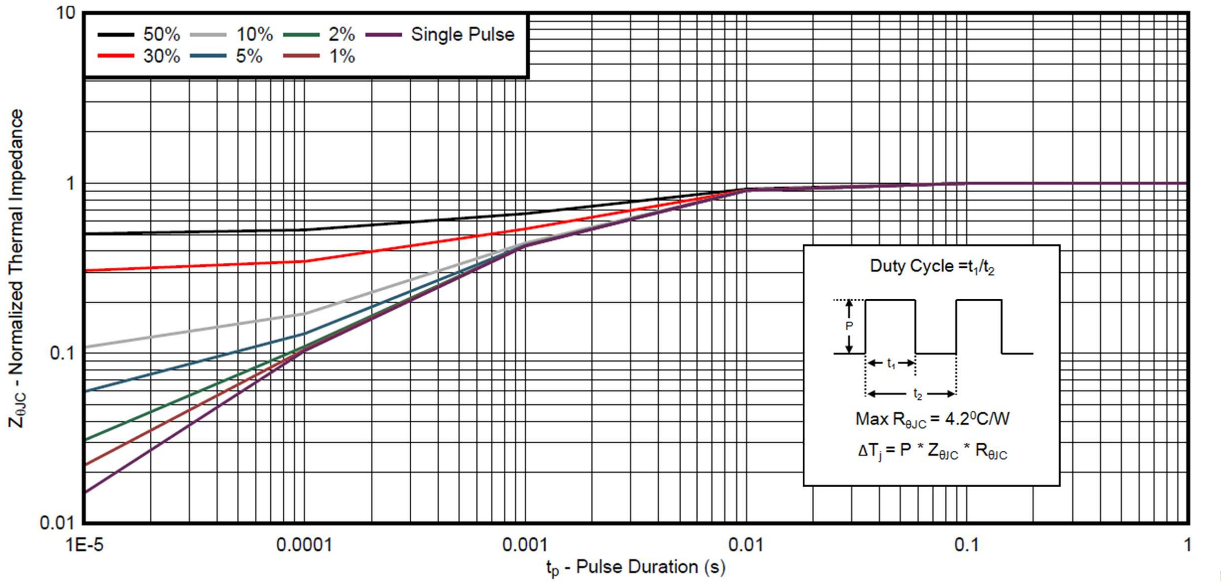


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

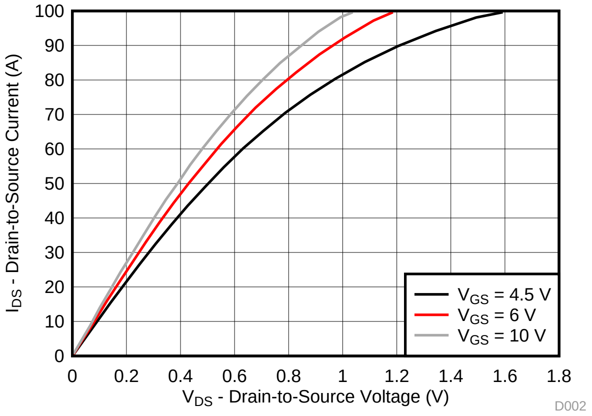
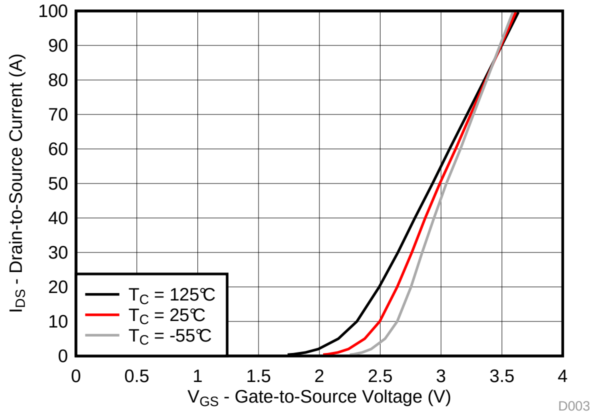
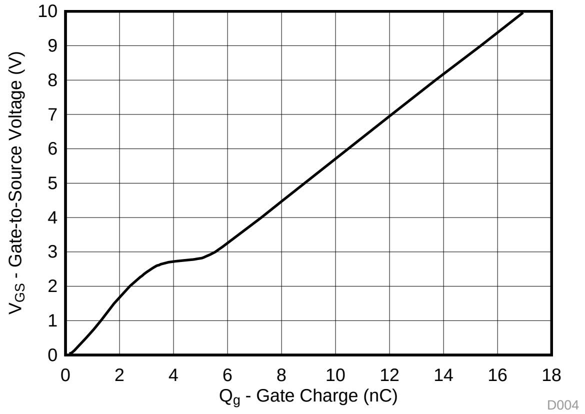


Figure 2. Saturation Characteristics



V_{DS} = 5 V

Figure 3. Transfer Characteristics



I_D = 10 A V_{DS} = 15 V

Figure 4. Gate Charge

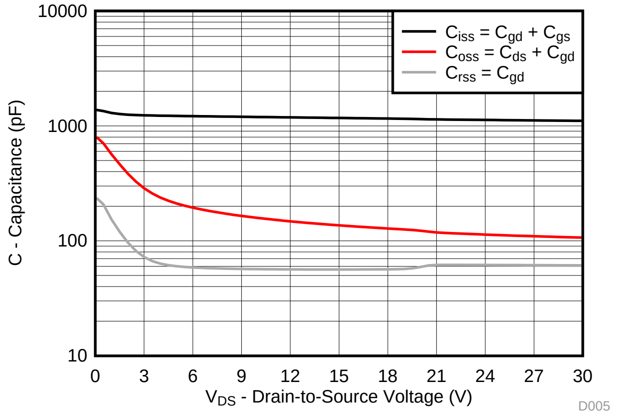
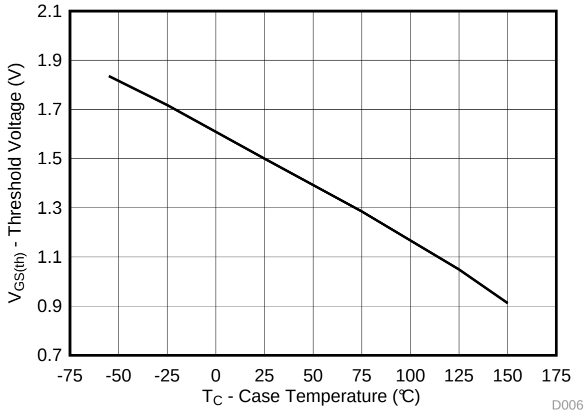


Figure 5. Capacitance



I_D = 250 µA

Figure 6. Threshold Voltage vs Temperature

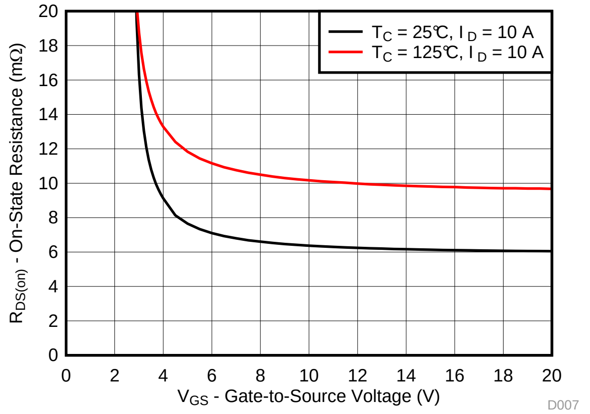
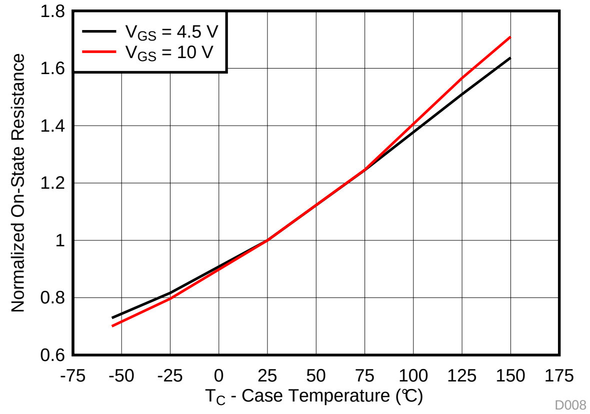


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)



I_D = 10 A

Figure 8. Normalized On-State Resistance vs Temperature

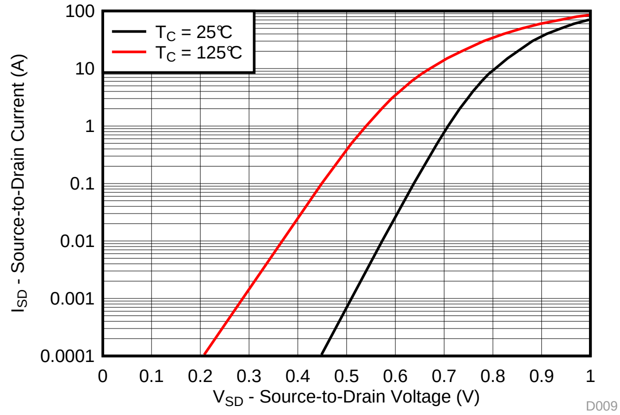
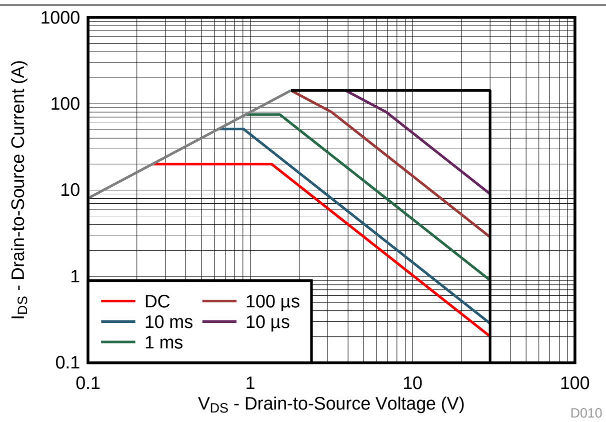


Figure 9. Typical Diode Forward Voltage



Single Pulse,
Max $R_{\theta JC}$ = 4.2°C/W

Figure 10. Maximum Safe Operating Area (SOA)

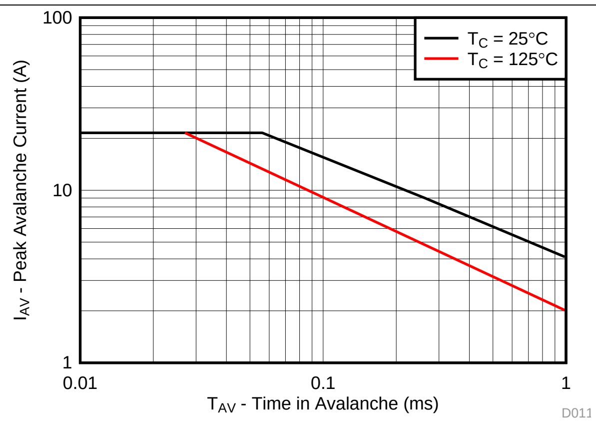


Figure 11. Single Pulse Unclamped Inductive Switching

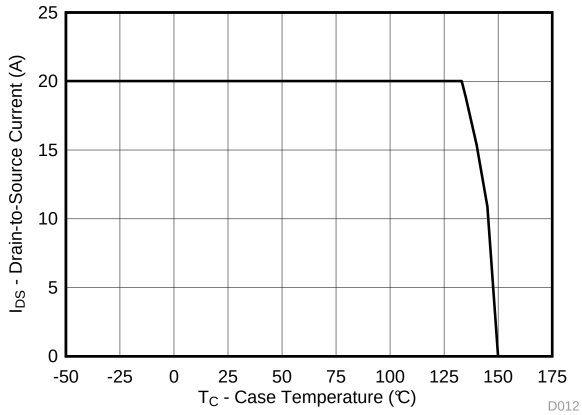


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.2 Trademarks

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6.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.4 Glossary

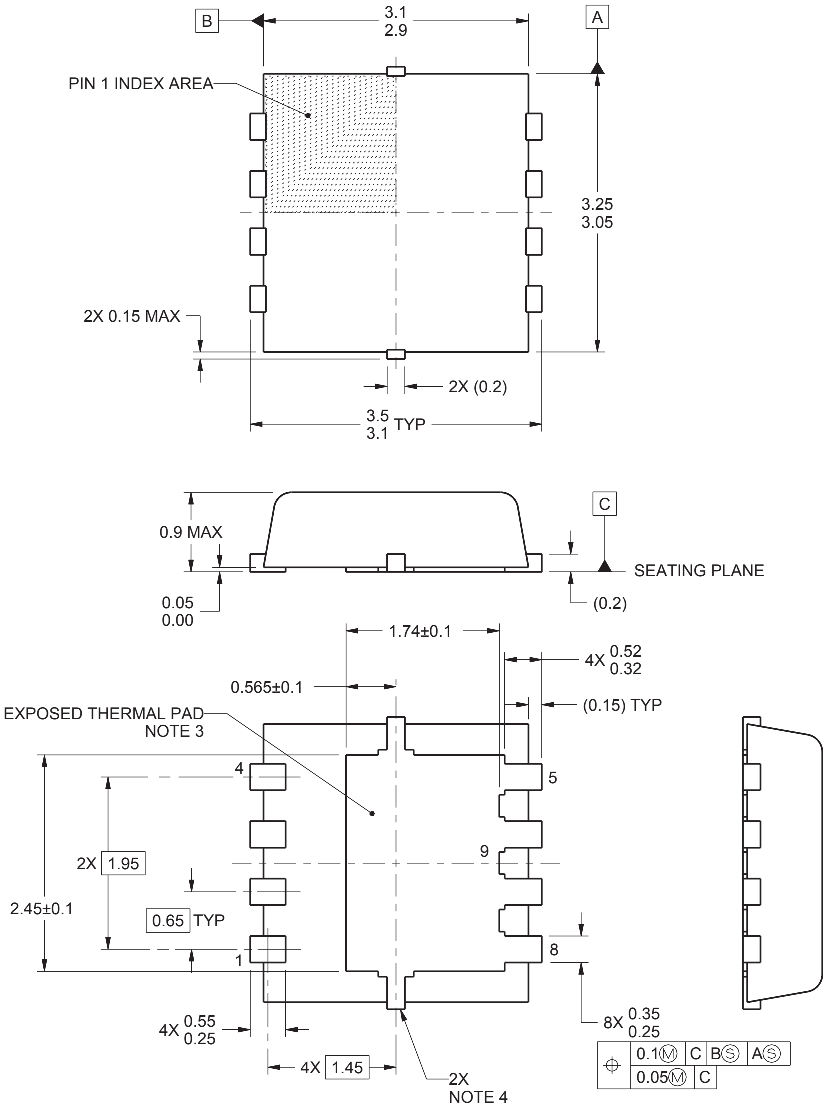
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

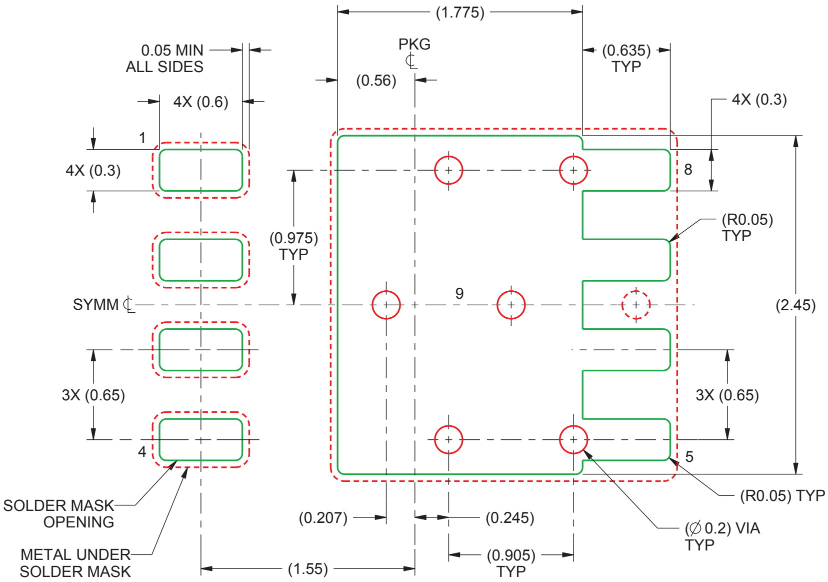
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Q3A Package Dimensions



1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Metalized features are supplier options and may not be on the package.
5. All dimensions do not include mold flash or protrusions.

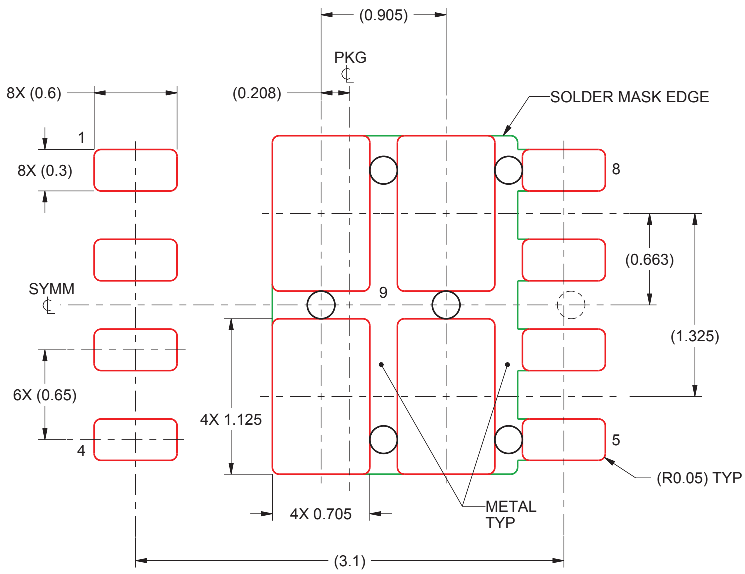
7.2 Q3A Recommended PCB Pattern



1. This package is designed to be soldered to a thermal pad on the board. For more information, see *QFN/SON PCB Attachment* application report, SLUA271.
2. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

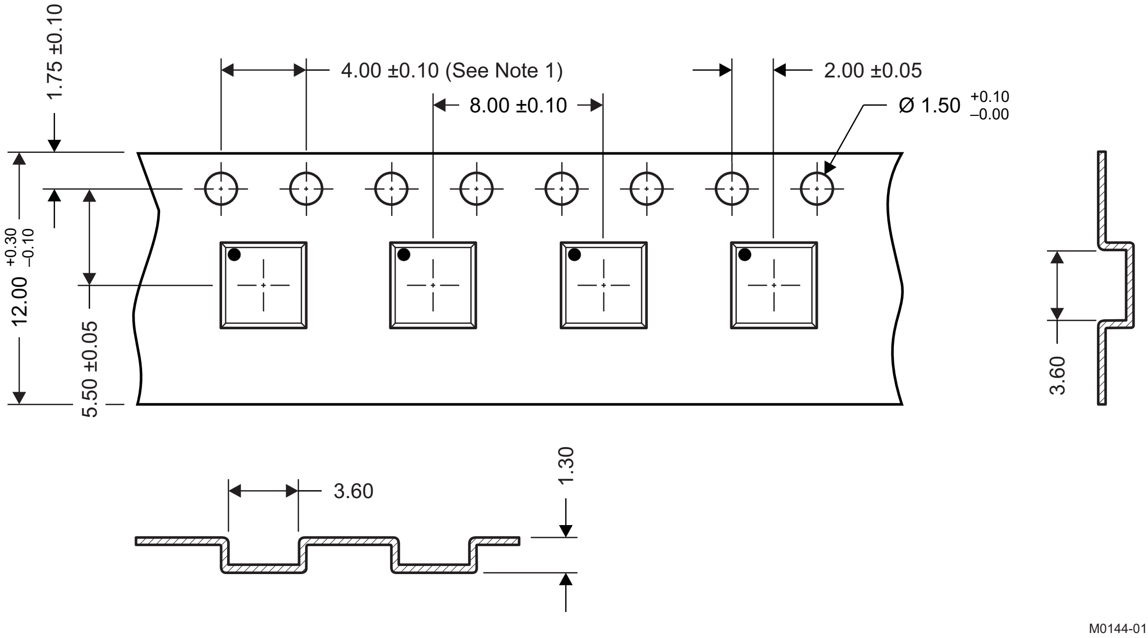
For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

7.3 Q3A Recommended Stencil Pattern



1. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

7.4 Q3A Tape and Reel Information



Notes: 1. 10-sprocket hole-pitch cumulative tolerance ±0.2

2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm

3. Material: black static-dissipative polystyrene

4. All dimensions are in mm, unless otherwise specified.

5. Thickness: 0.30 ±0.05 mm

6. MSL1 260°C (IR and convection) PbF-reflow compatible

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD17578Q3A	ACTIVE	VSONP	DNH	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		17578	Samples
CSD17578Q3AT	ACTIVE	VSONP	DNH	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		17578	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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