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STB46N30M5

Automotive-grade N-channel 300 V, 53 A, 0.037 Ω typ.,
 MDmesh™ V Power MOSFET in a D²PAK package

Datasheet - production data

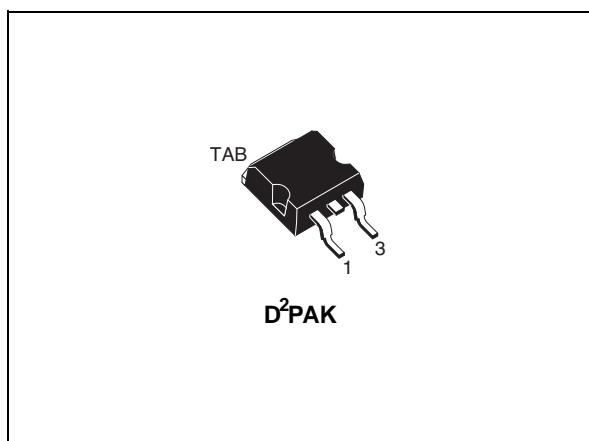
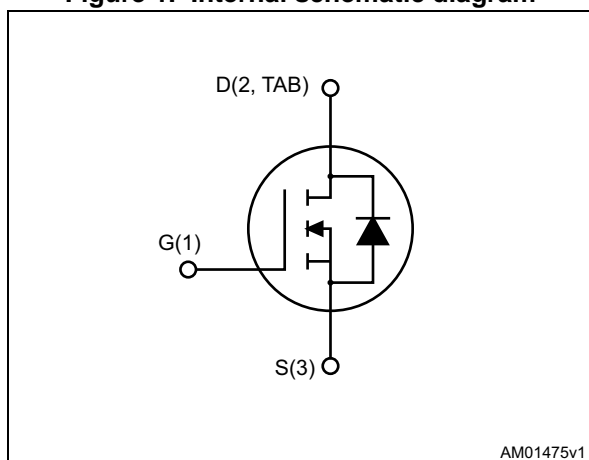


Figure 1. Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STB46N30M5	300 V	0.04 Ω	53 A

- Designed for automotive applications and AEC-Q101 qualified
- Amongst the best R_{DS(on)} * area
- High dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% avalanche tested

Applications

- Switching applications

Description

This device is an N-channel MDmesh™ V Power MOSFET based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

Table 1. Device summary

Order code	Marking	Packages	Packaging
STB46N30M5	46N30M5	D ² PAK	Tape and reel

Contents

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Electrical ratings

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{GS}	Gate-source voltage	± 25	V
I _D	Drain current (continuous) at T _C = 25 °C	53	A
I _D	Drain current (continuous) at T _C = 100 °C	34	A
I _{DM} ⁽¹⁾	Drain current (pulsed)	212	A
P _{TOT}	Total dissipation at T _C = 25 °C	250	W
dv/dt ⁽²⁾	Peak diode recovery voltage slope	15	V/ns
T _{stg}	Storage temperature	- 55 to 150	°C
T _j	Max. operating junction temperature	150	°C

1. Pulse width limited by safe operating area
2. I_{SD} ≤ 53 A, di/dt ≤ 400 A/μs, V_{DS(peak)} < V_{(BR)DSS}, V_{DD}=240 V

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case max	0.5	°C/W
R _{thj-pcb} ⁽¹⁾	Thermal resistance junction-pcb max	30	°C/W

1. When mounted on 1 inch² FR-4, 2 Oz copper board

Table 4. Thermal data

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T _j max)	16	A
E _{AS}	Single pulse avalanche energy (starting T _j = 25°C, I _D = I _{AR} , V _{DD} = 50 V)	550	mJ

Electrical characteristics

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2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified).

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ($V_{GS} = 0$)	$I_D = 1\text{ mA}$	300			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 300\text{ V}$			1	μA
		$V_{DS} = 300\text{ V}, T_C = 125\text{ °C}$			100	μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 26.5\text{ A}$		0.037	0.04	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$	-	4240	-	pF
C_{oss}	Output capacitance		-	205	-	pF
C_{rss}	Reverse transfer capacitance		-	9.5	-	pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0\text{ to }240\text{ V}, V_{GS} = 0$	-	373	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	202	-	pF
R_g	Gate input resistance	$f = 1\text{ MHz}, \text{ gate DC Bias} = 0, \text{ test signal level} = 20\text{ mV}, I_D = 0$	-	1.4	-	Ω
Q_g	Total gate charge	$V_{DD} = 240\text{ V}, I_D = 24\text{ A}, V_{GS} = 10\text{ V}$ (see Figure 16)	-	95	-	nC
Q_{gs}	Gate-source charge		-	23	-	nC
Q_{gd}	Gate-drain charge		-	37	-	nC

- $C_{o(tr)}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS} .
- $C_{o(er)}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS} .

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Electrical characteristics

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(v)}$	Voltage delay time	$V_{DD} = 240\text{ V}$, $I_D = 32\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 15)	-	66	-	ns
$t_{r(v)}$	Voltage rise time		-	15	-	ns
$t_{f(i)}$	Current fall time		-	24	-	ns
$t_{c(off)}$	Crossing time		-	22.5	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		53	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		212	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 53\text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 48\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 20)	-	223		ns
Q_{rr}	Reverse recovery charge		-	2.5		μC
I_{RRM}	Reverse recovery current	$I_{SD} = 48\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 20)	-	23		A
t_{rr}	Reverse recovery time		-	280		ns
Q_{rr}	Reverse recovery charge		-	3.9		μC
I_{RRM}	Reverse recovery current		-	28		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Electrical characteristics

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2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

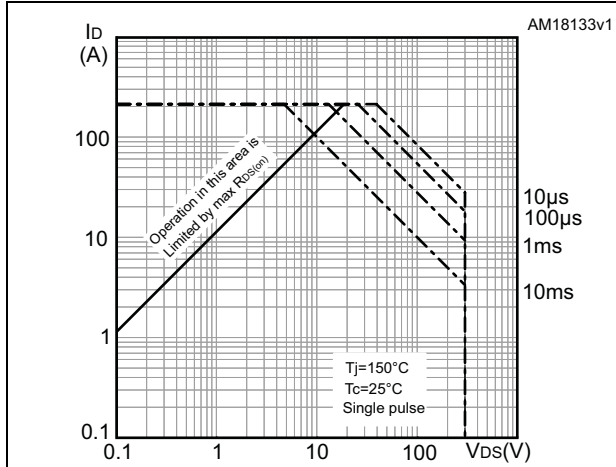


Figure 3. Thermal impedance

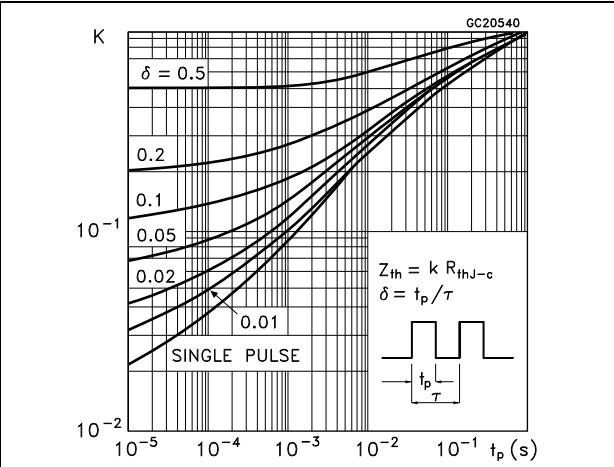


Figure 4. Output characteristics

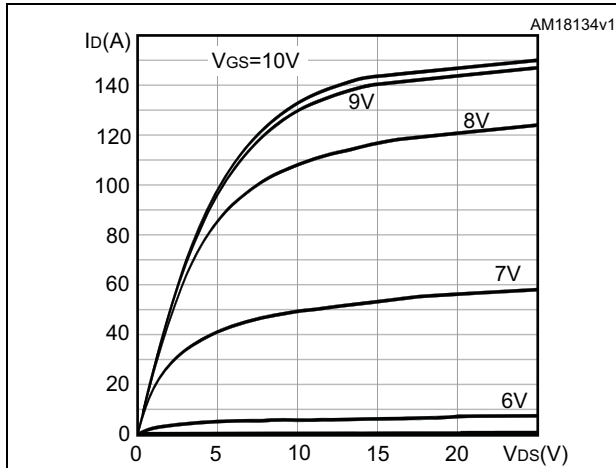


Figure 5. Transfer characteristics

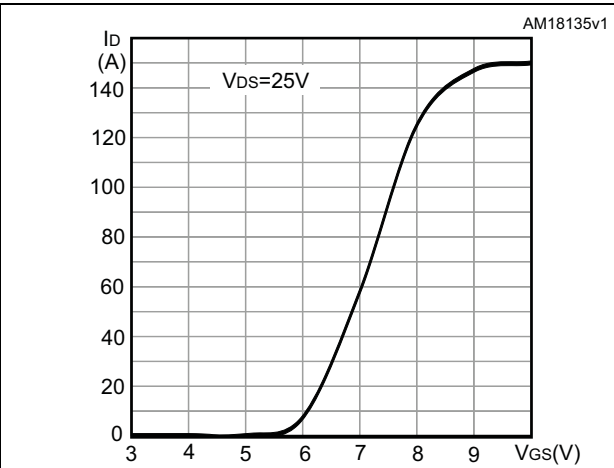


Figure 6. Gate charge vs gate-source voltage

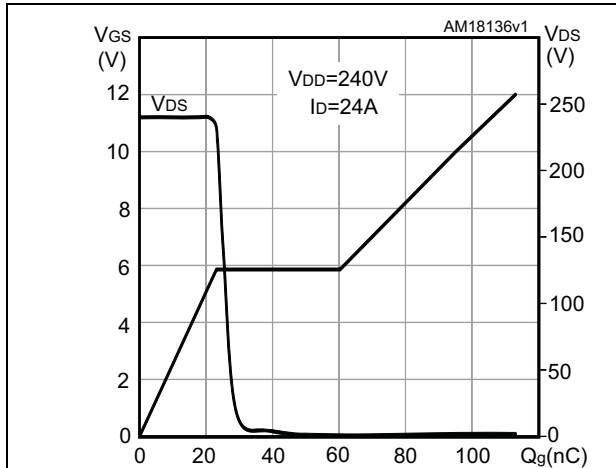
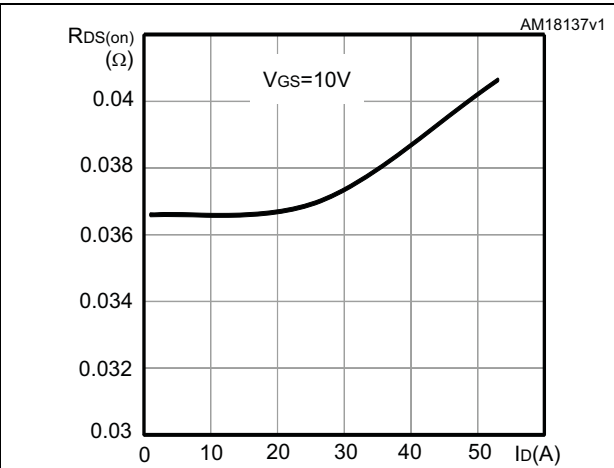


Figure 7. Static drain-source on-resistance



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Electrical characteristics

Figure 8. Capacitance variations

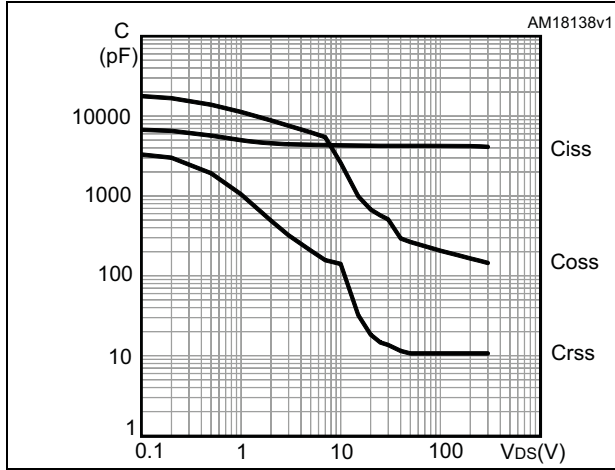


Figure 9. Output capacitance stored energy

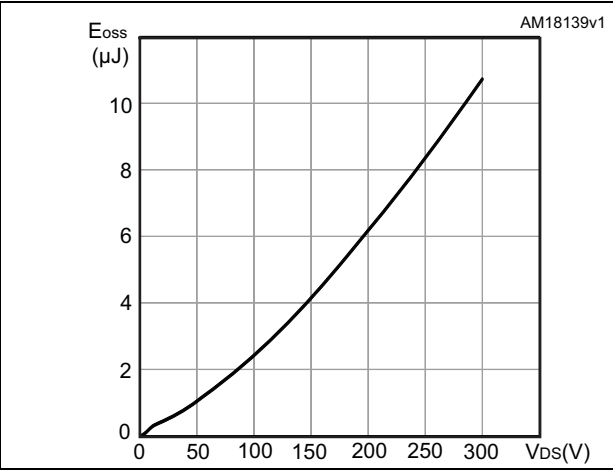


Figure 10. Normalized gate threshold voltage vs temperature

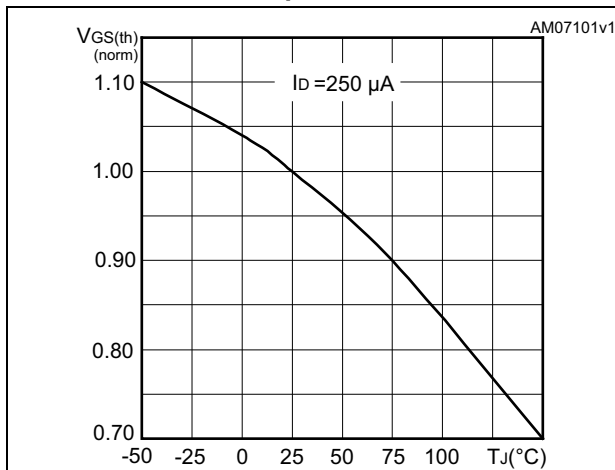


Figure 11. Normalized on-resistance vs temperature

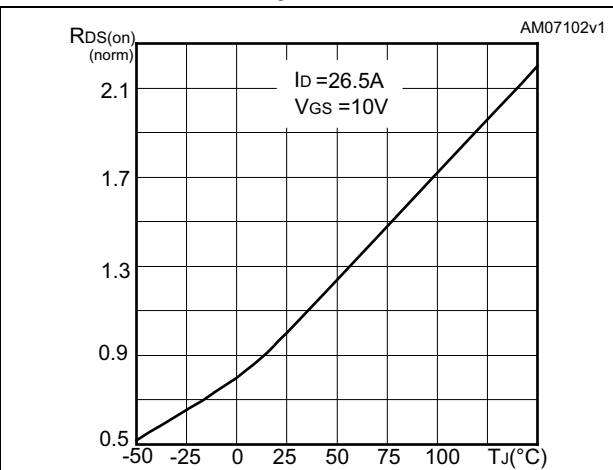


Figure 12. Normalized V(BR)DSS vs temperature

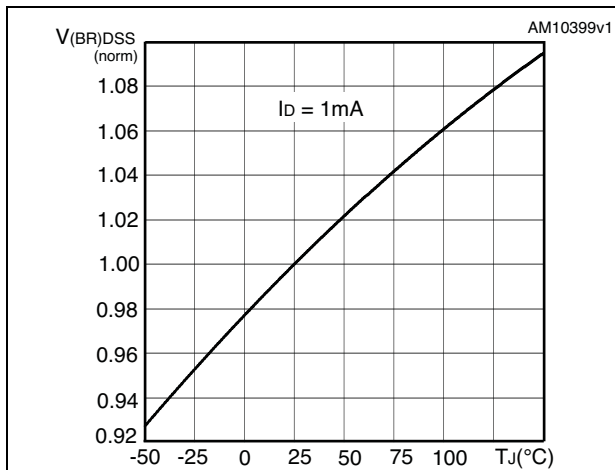
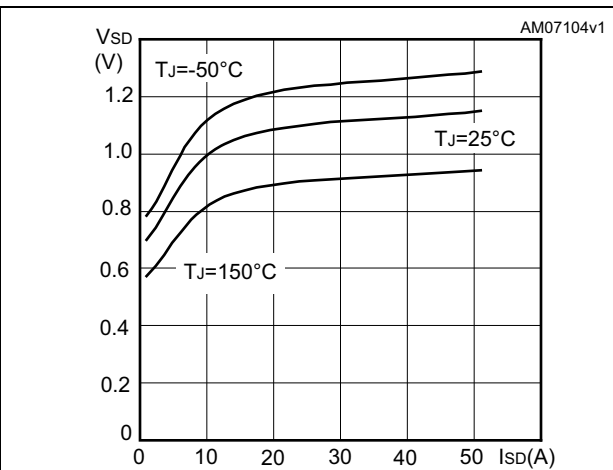


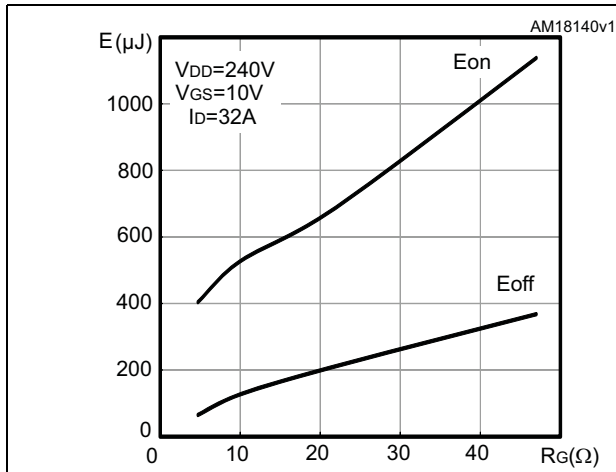
Figure 13. Source-drain diode forward characteristics



Electrical characteristics

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Figure 14. Switching losses vs gate resistance (1)



1. E_{on} including reverse recovery of a SiC diode

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Test circuits

3 Test circuits

Figure 15. Switching times test circuit for resistive load

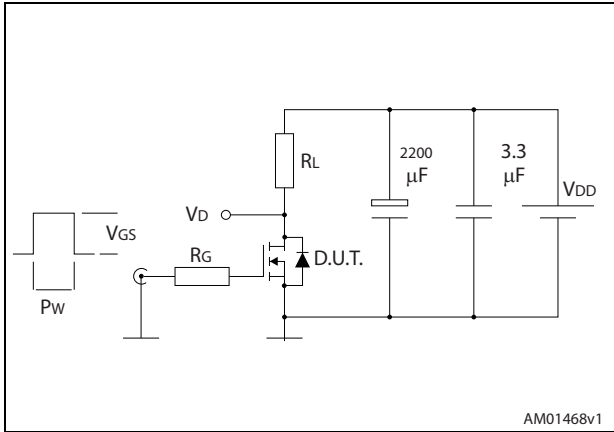


Figure 16. Gate charge test circuit

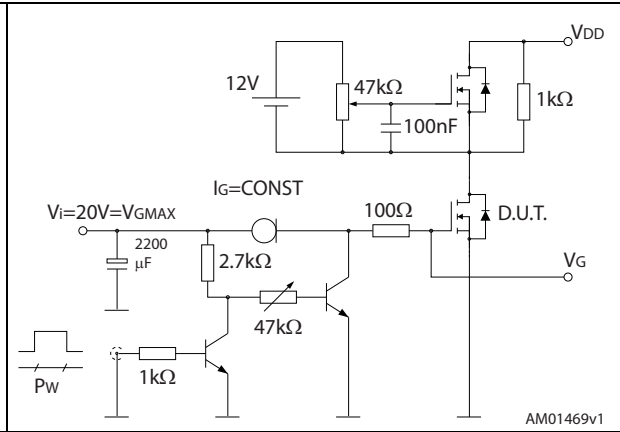


Figure 17. Test circuit for inductive load switching and diode recovery times

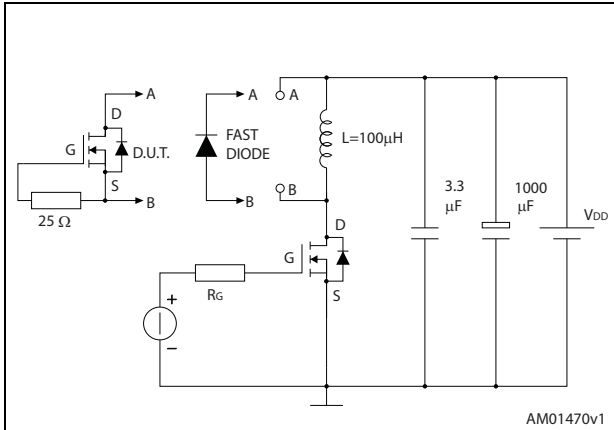


Figure 18. Unclamped inductive load test circuit

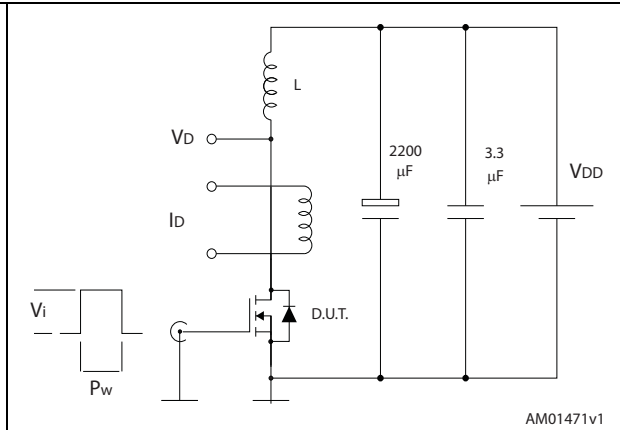


Figure 19. Unclamped inductive waveform

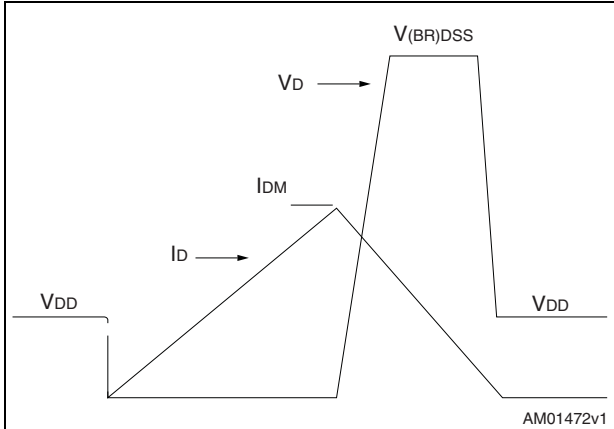
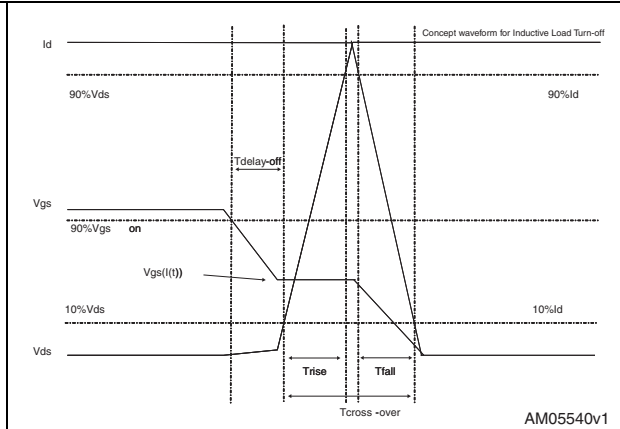


Figure 20. Switching time waveform



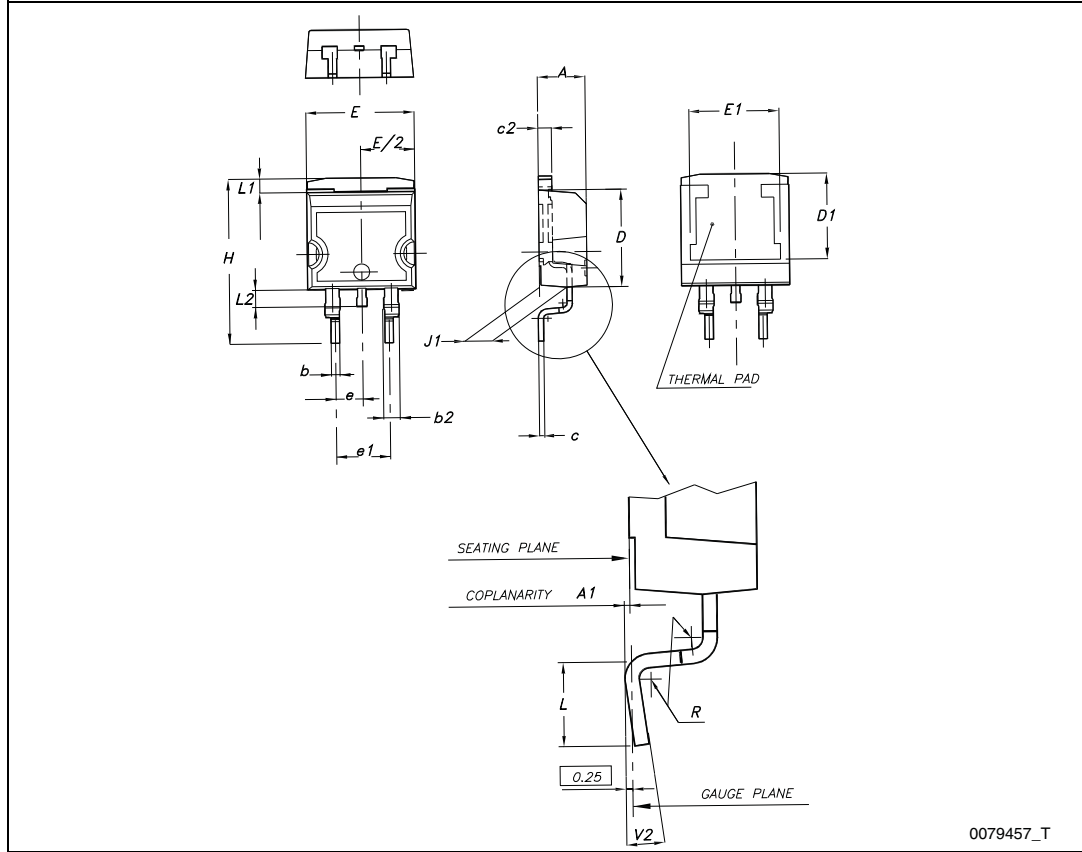
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

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Package mechanical data

Figure 21. D²PAK (TO-263) drawing



Package mechanical data

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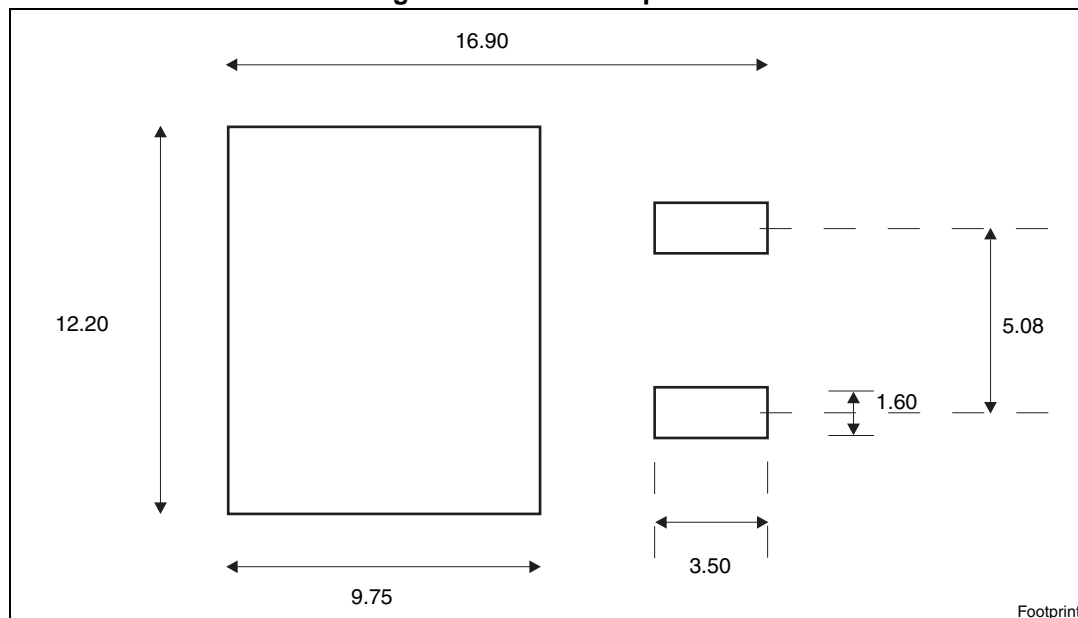
Table 9. D²PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

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Package mechanical data

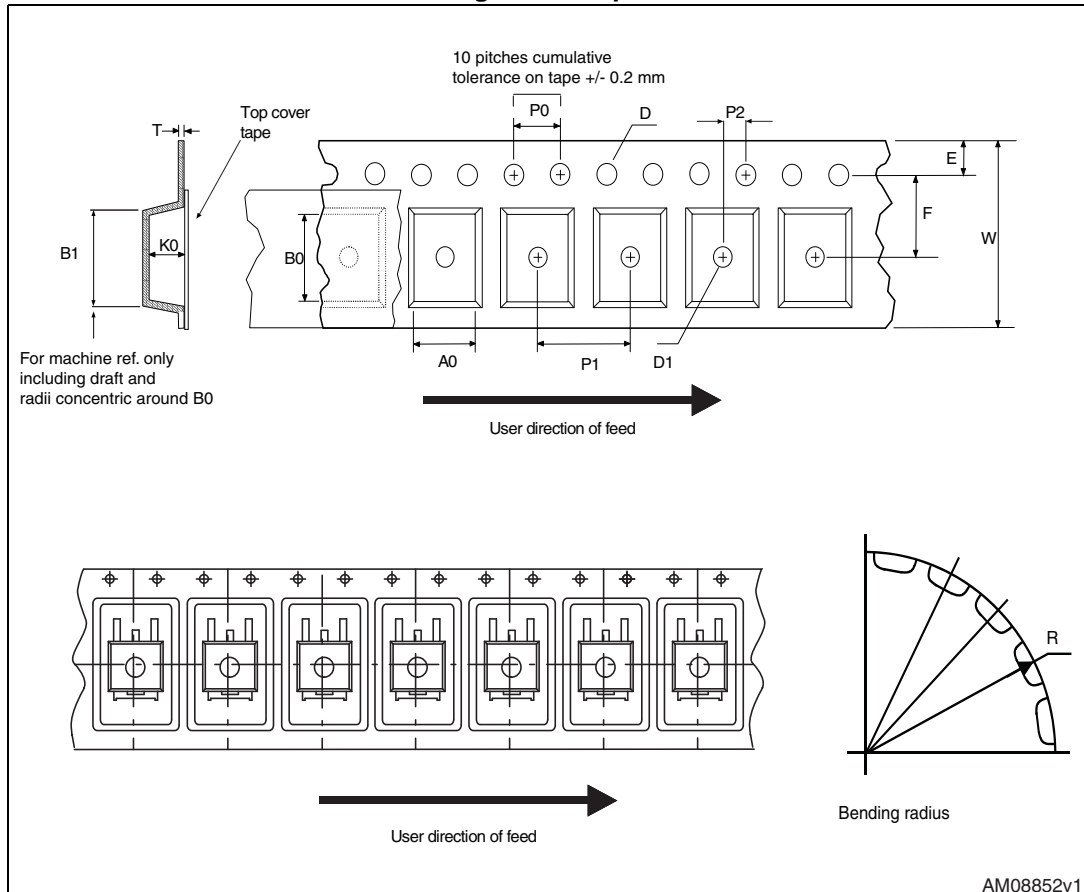
Figure 22. D²PAK footprint^(a)



a. All dimension are in millimeters

5 Packaging mechanical data

Figure 23. Tape



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Packaging mechanical data

Figure 24. Reel

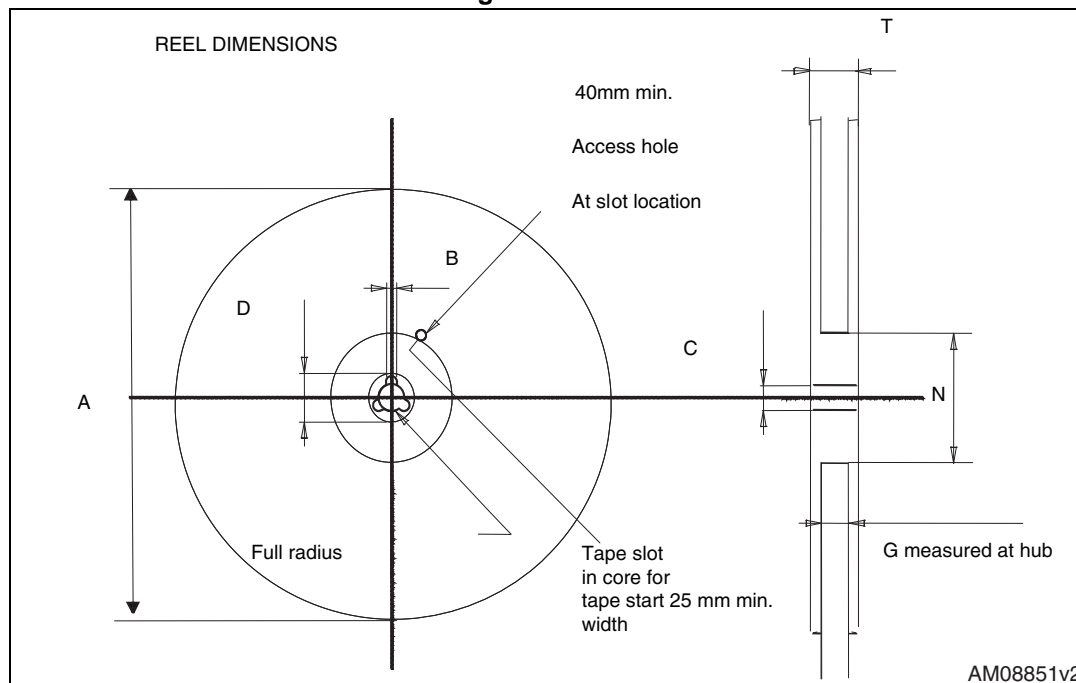


Table 10. D²PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

6 Revision history

Table 11. Document revision history

Date	Revision	Changes
24-Mar-2014	1	Initial release.
11-Apr-2014	2	<ul style="list-style-type: none">– Document status promoted from preliminary data to production data– Minor text changes

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