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Hands-on Workshop: Designing Applications with the S12 MagniV Family

AMF-AUT-T0665

Derrick Klotz
Regional FAE
Senior Member of Technical Staff

November 2013

Agenda

- Automotive Body Electronics
- MagniV Solutions and Roadmap
- Lab 1 ————————
  - Getting Started with CodeWarrior 10.4

- S12Z Enhanced CPU Core
- S12ZVM for BLDC Motor Control
- S12ZVL for General Purpose LIN
- S12ZVC for General Purpose CAN
- Lab 2 ————————
  - Developing a Project for the S12ZVL

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Automotive Market Trends – Sensors and Actuators

- **Reduction of power consumption**
  - LIN to reduce cables weight
  - Smarter motor control techniques
  - Smarter and more sensors

LOCAL INTERCONNECT NETWORK

- **Reduction of physical size**
  - Electro-mechanical integration
  - High temperature >125°C Ta

- **High Growth**
  - Driven by affordability of LIN
  - Driven by comfort and convenience features

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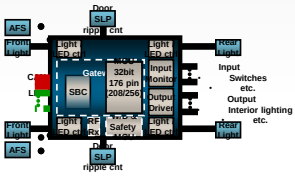
What's Behind Body Electronics?


Integrated BCM Gateways






Comfort Features	Vehicle Networking	Safety Related	Security
• Door Module • Window Lift • Seat Module/position • HVAC • Electric sunroof/shade • Interior lighting	• Central Body Control Module • Central Gateways: CAN, LIN, Flexray, Ethernet, MOST	• Steering column lock • Steering column adjustment • AFS • Anti-pitch power windows • Wipers and rain sensors	• Immobilizer • Keyless Entry • Preventing hacking and counterfeit modules

- Body systems embrace a broad variety of applications inside the cabin
- Body systems cover the widest range of performance requirements
  - Small 8-bit controllers and watchdogs
  - General purpose 16-bit controllers
  - High performance 32-bit compute engines

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Body Market Trends and Challenges

- More complex Gateways with higher performance and multicore usage (Expanding memory)
- Ethernet and wireless communication
- Personalization options driving LIN nodes

- Functional Safety - ISO26262
  Several body-apps need ASIL A/B (some C/D)
- Reduced ASIL-assessment effort
- Security/Cryptography for Gateway and BCM modules

- Power management in stop and run modes
- Autosar SW management of partial/pretended networking
- EC-motors, LED-lighting

- Cost reduction via ECU integration
- Electrification of the car replacing mech. components
- Scalability of hardware and software
- Auto generated code to decrease dev costs

Software Integration:

- Autosar:
  - Multicore-support
  - OS
  - MCAL
- Safety:
  - SW-routines supporting self-test (Core/Memory)
- Security:
  - Cryptography algorithmic support
- Application-support
  - Motor Control-library
  - Reference designs

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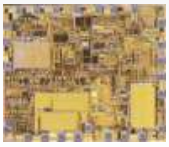
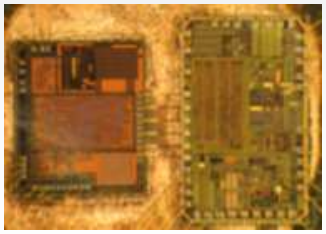
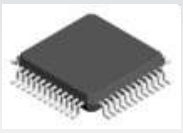
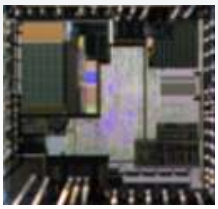
Automotive Microcontroller Portfolio

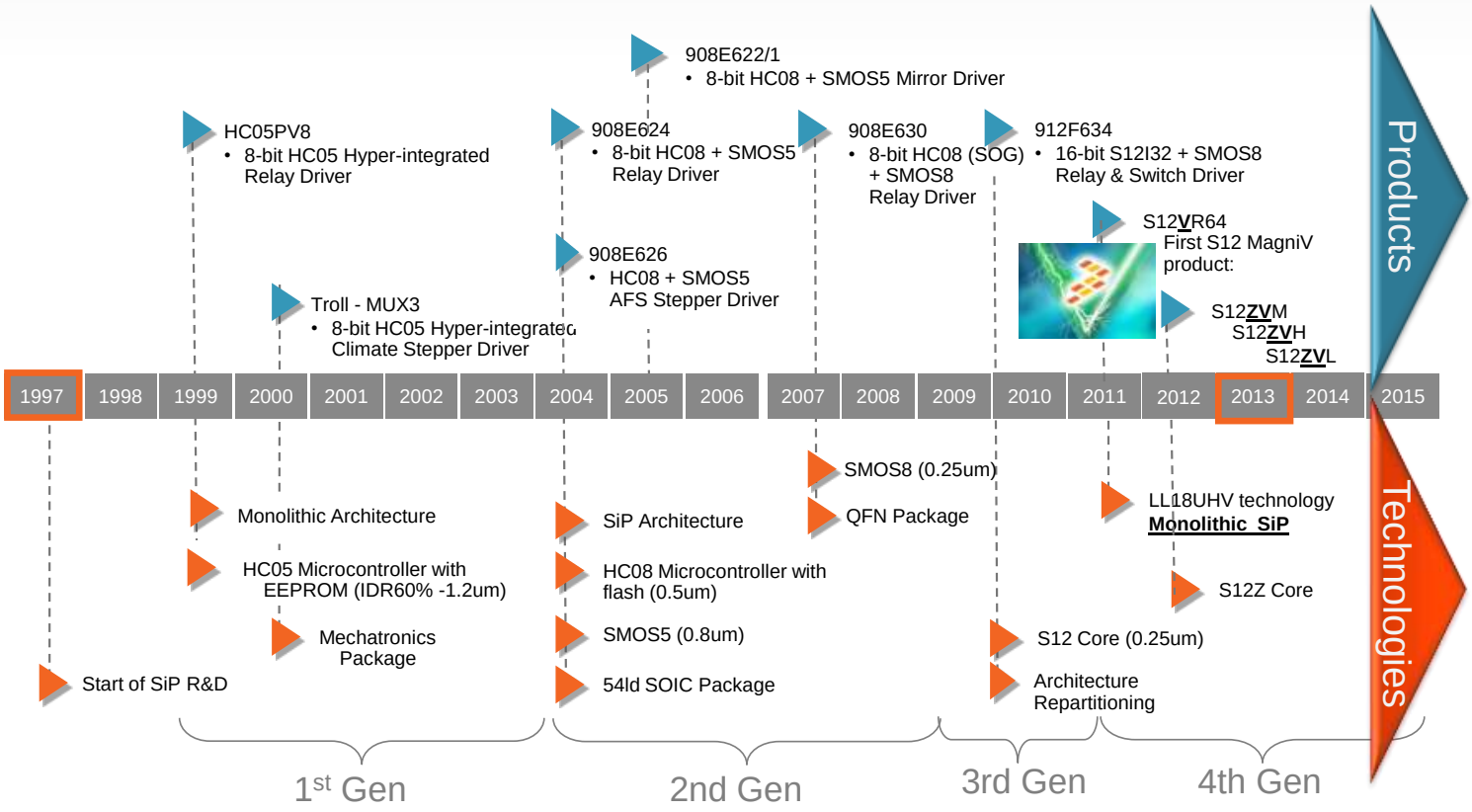
				Target Applications
MPU	i.MX 	Multimedia processors	Multicore and graphics performance	• Center stack • Instrument cluster • Telematics
32-bit MCU	Qorivva 	Highest-performance automotive MCU	Multicore with integrated safety and security	• Powertrain • Safety & chassis • Central body • Vehicle networking
16-bit MCU	S12 	An industry-leading 16-bit architecture	MagniV: Most integrated MCU	• Body electronics • Instrument cluster LIN slaves
8-bit MCU	S08	15-year automotive workhorse	Most optimal and robust solution	• Sensor/Actuators • Switch and touch panels • Companion MCUs

What is S12 MagniV?

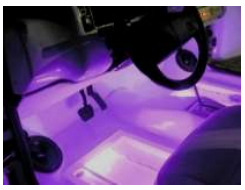
SiP = System in Package

Semi-Discrete Solution	Multi-die SiP	Monolithic SiP
• Standard MCU  • Application Specific Analog IC (ASIC) 	• Single package • Die-to-die bonding  	• MCU and Analog on the same die  

ver 15 Years of System in Package (SiP) Experience



LL18UHV Technology Summary for S12 MagniV



Existing
Low Leakage 180nm CMOS+NVM

40V UHV Devices

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MagniV building blocks

High-Voltage Components

- VREG for tot. supply:
  - 70mA w/o ext comp. or
  - 170mA with ext. ballast
- LIN-PHY
- CAN-PHY
- V-BAT SENSE
- V-SUP SENSE
- HVI (12V-input with ADC)
- LS-drivers
- HS-drivers
- Charge Pump
- 4-6ch MOSFET Predriver (50-100nC)

Digital Components

- MS-CAN
- SCI
- SPI
- IIC
- GPIO
- PGPIO 20mA
- NGPIO 25mA
- BDM/BDC
- Key Wakeups
- Win Wdog
- RTC
- Timer 16Bit (25-64MHz)
- PWM 8/16Bit (25-50MHz)
- Motorcontrol PWM With Fault protection
- Prog. Trigger Unit
- Sound Generator
- Segment LCD (4x40)
- Stepper Motor Driver with SSD

MCU Core and Memories

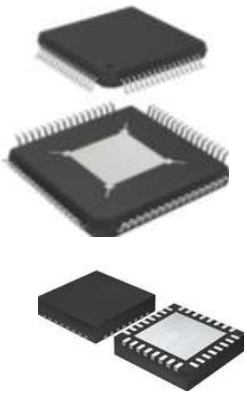
- S12- or S12Z-CPU 25/32/50MHz bus
- Flash (ECC) 8kB – 128kB
- EEPROM (ECC) 128B – 4kB
- RAM (ECC) 512B - 8kB

5V Analogue Components

- ADC 10-12Bit resolution 1-2 S/H-units Up to 16ch total
- Temp Sense
- Current Sense (2 x Op-Amp)
- Pierce Osc.
- RCosc. +/-1.3%
- PLL

Packaging

- LQFP: 32/48/64/100/144-pin
- LQFP-EP: 48/64-pin (150° C)
- QFN: 32-pin (5x5mm)



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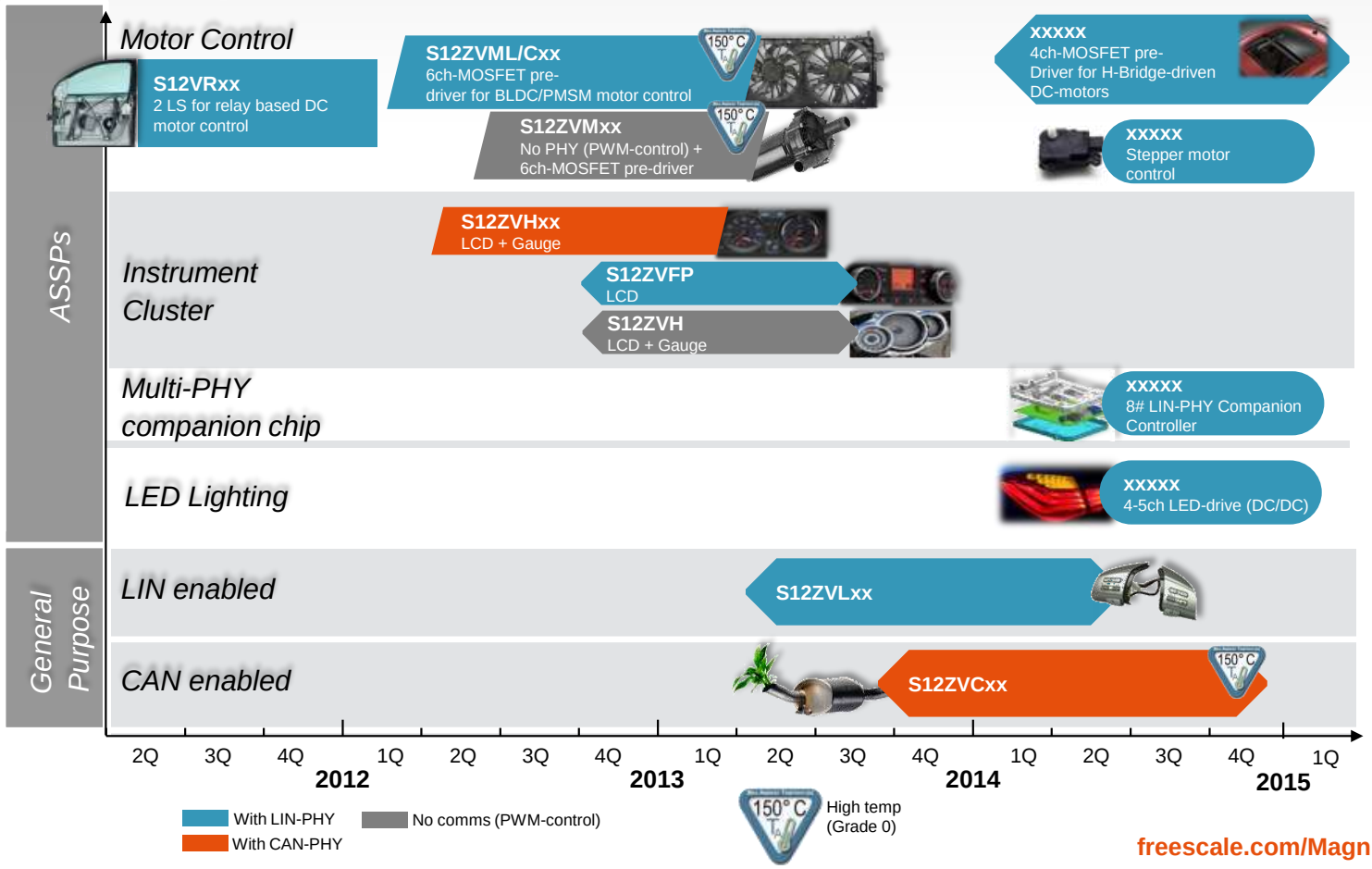
S12 MagniV Roadmap



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Agenda

Automotive Body Electronics
MagniV Solutions and Roadmap

Lab 1

Getting Started with CodeWarrior 10.4

S12Z Enhanced CPU Core
S12ZVM for BLDC Motor Control
S12ZVL for General Purpose LIN
S12ZVC for General Purpose CAN

Lab 2

Developing a Project for the S12ZVL

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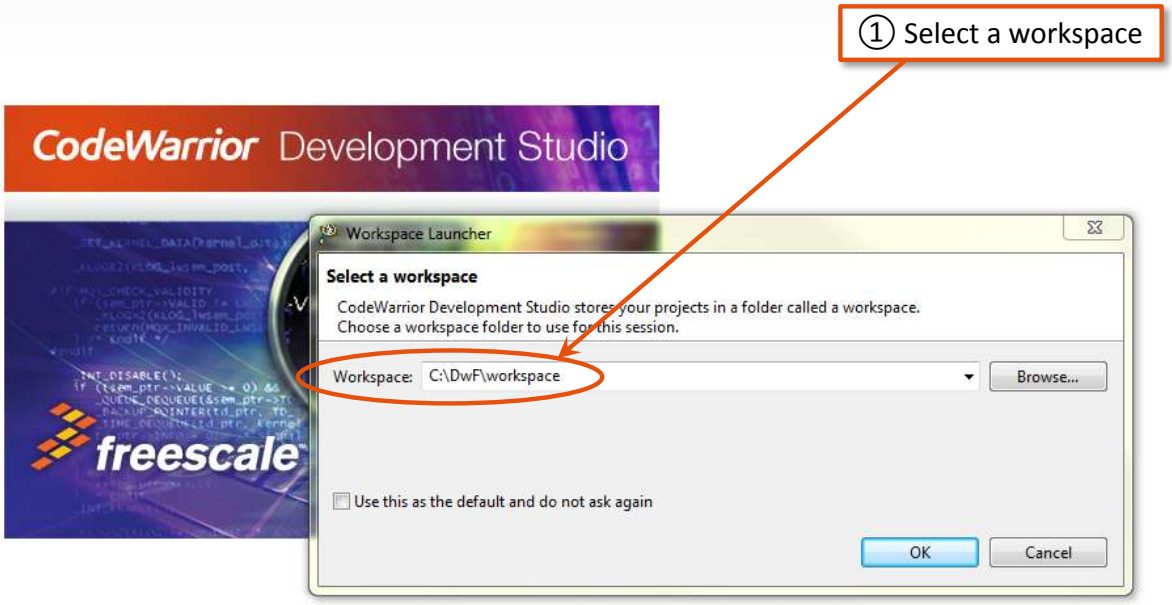
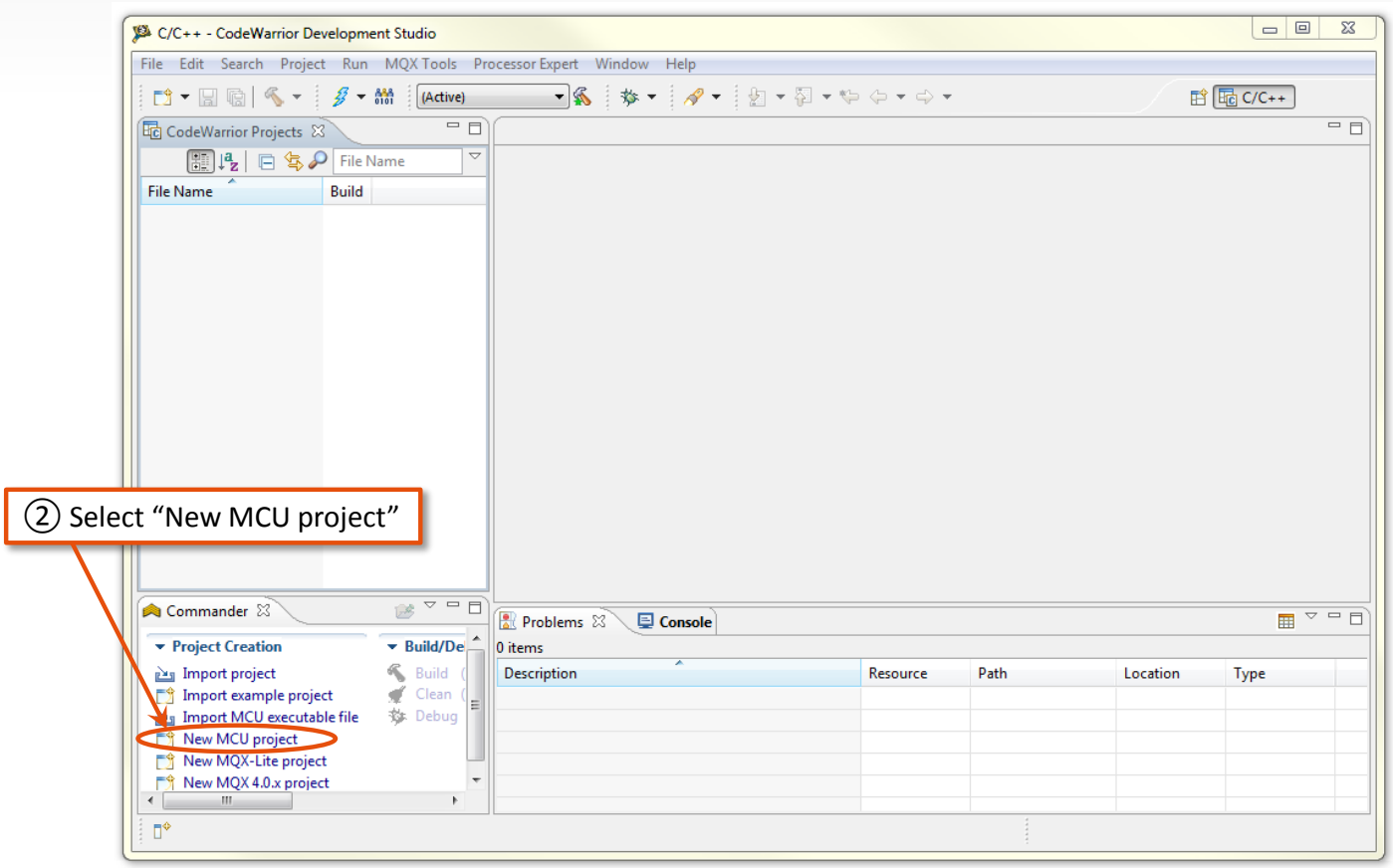
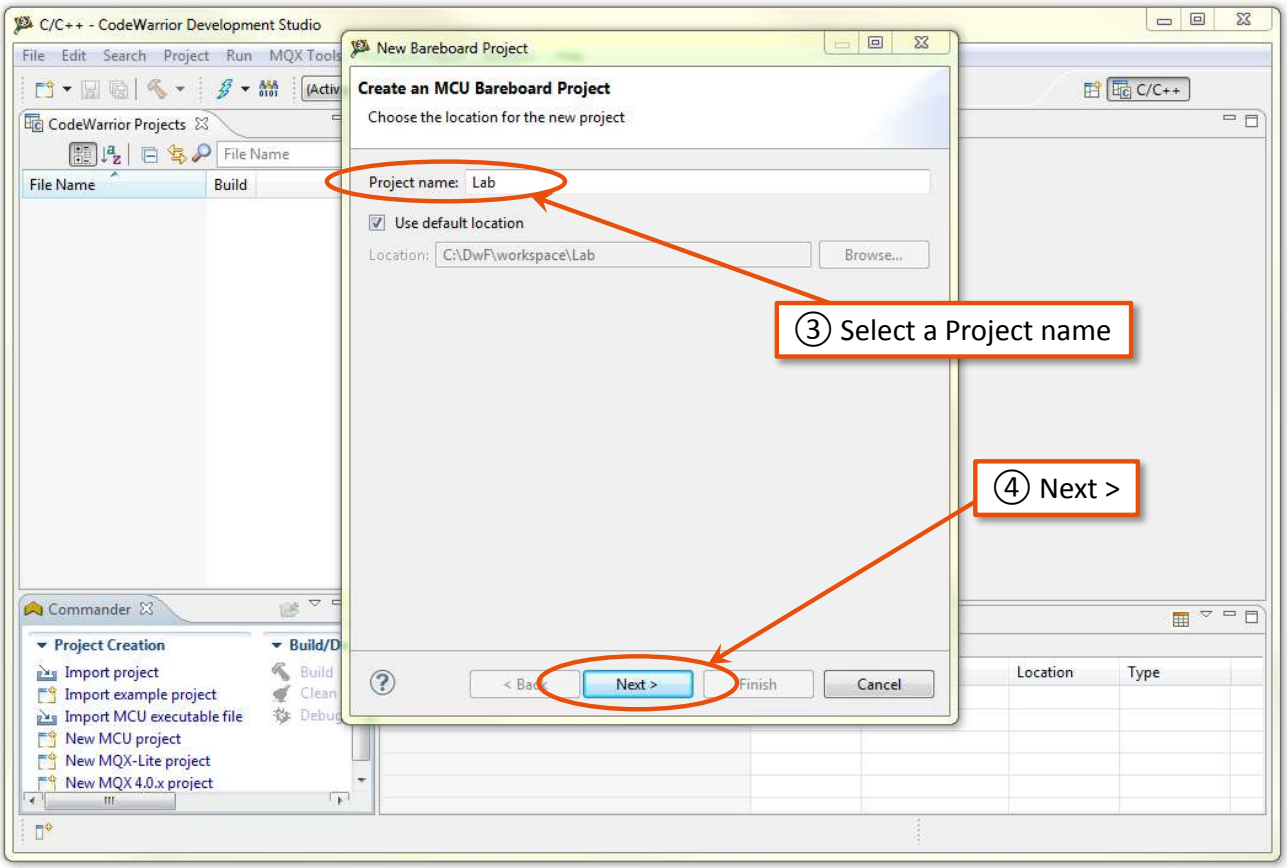
Launch CodeWarrior 10.4



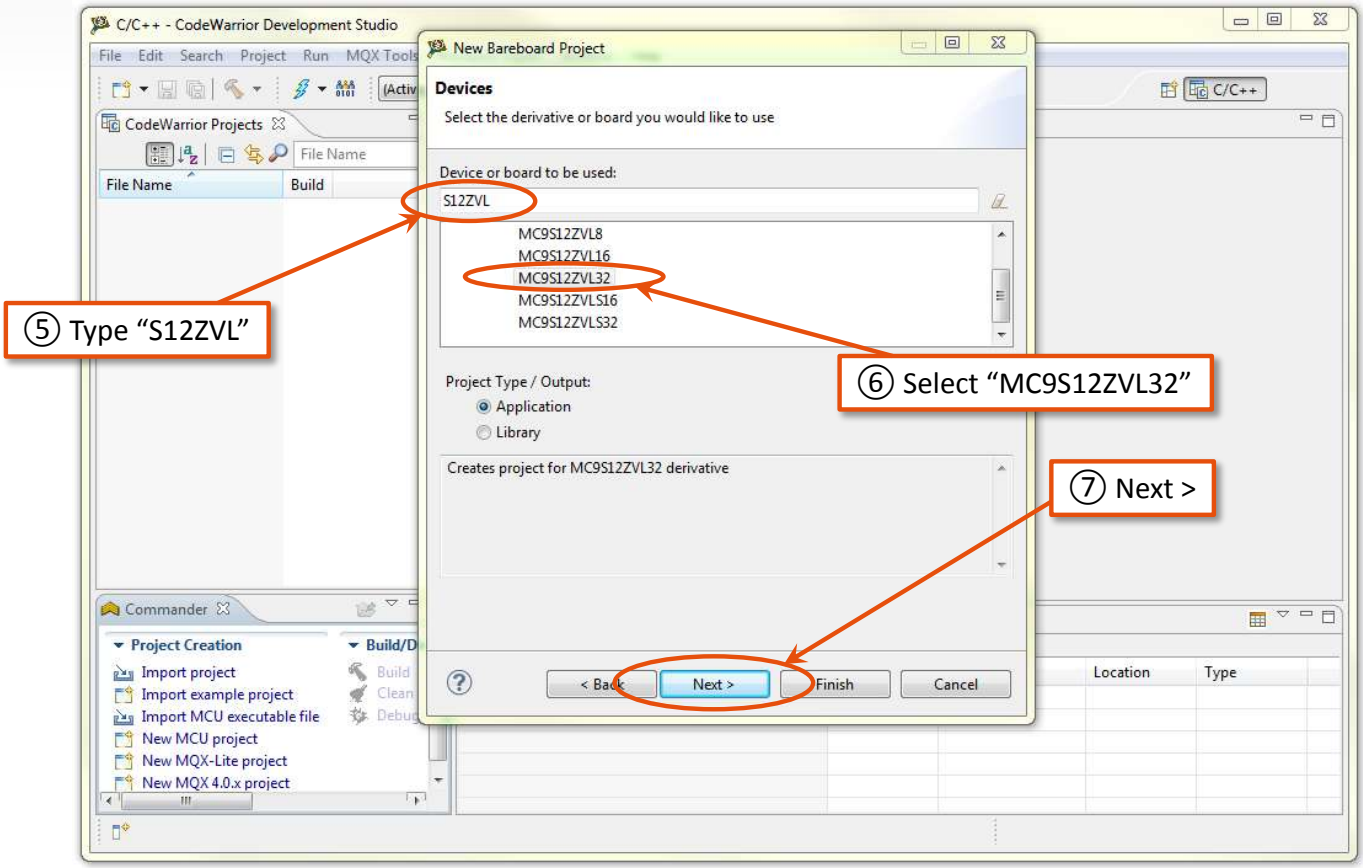
The C/C++ Perspective



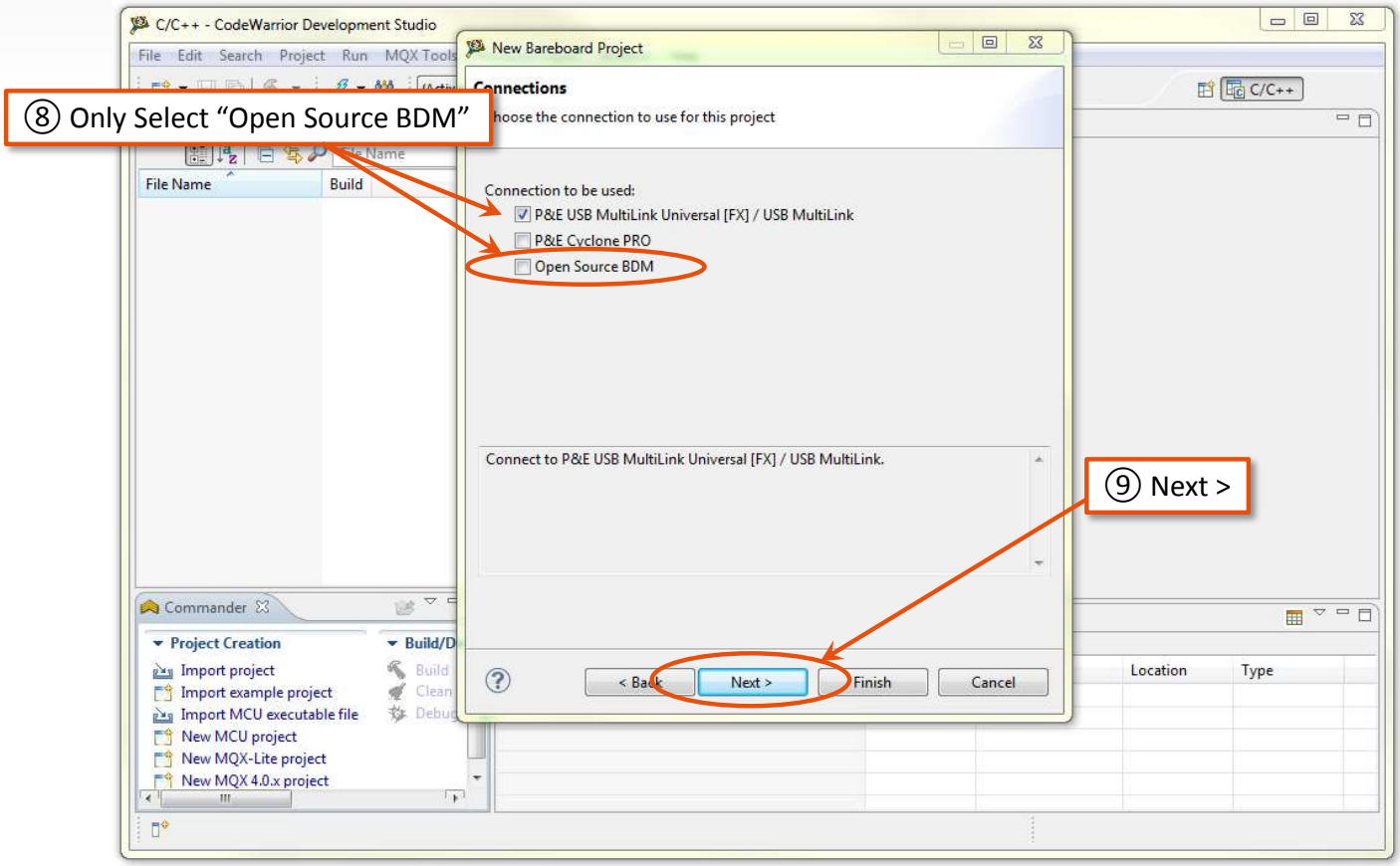
Start a New Project – “Lab”



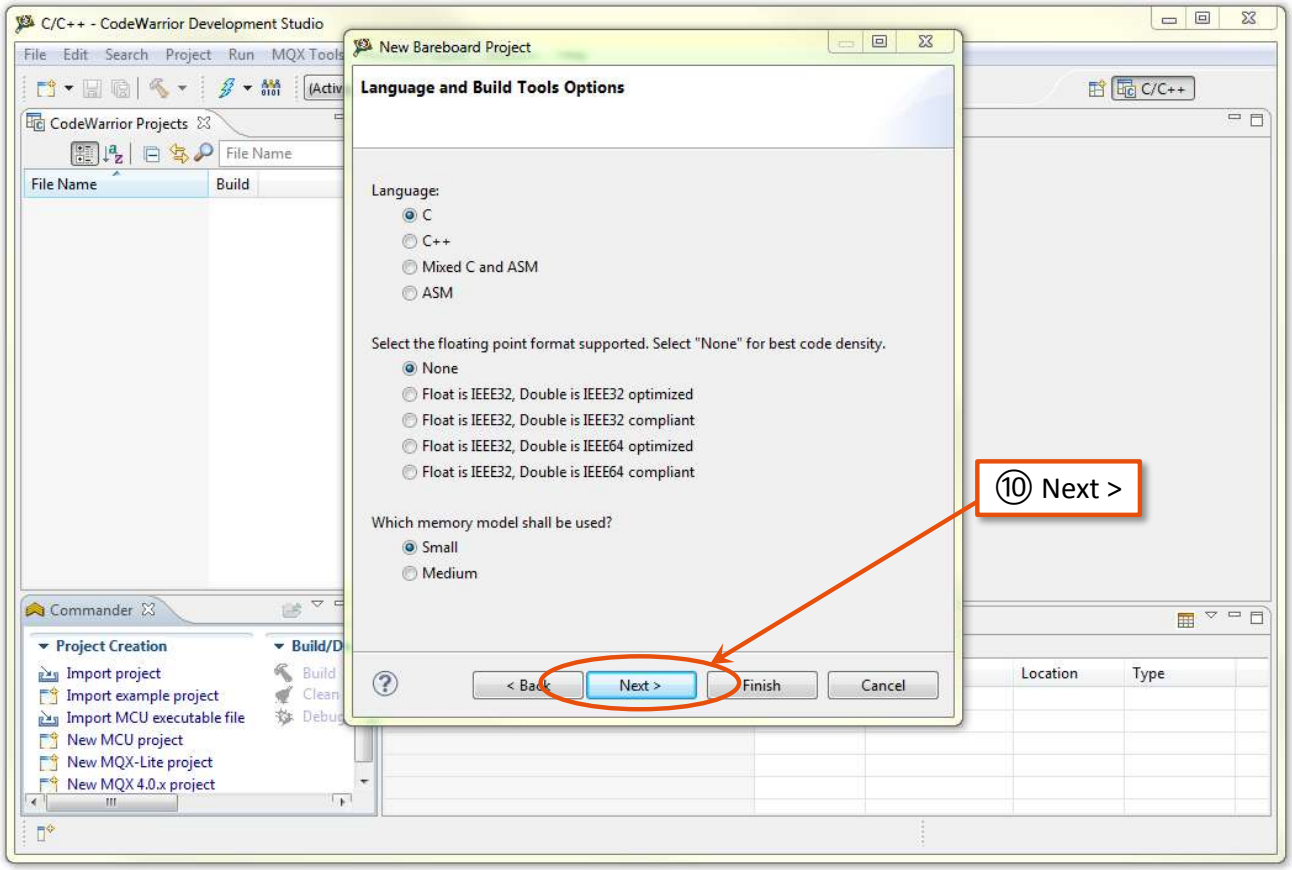
Select the Target Device



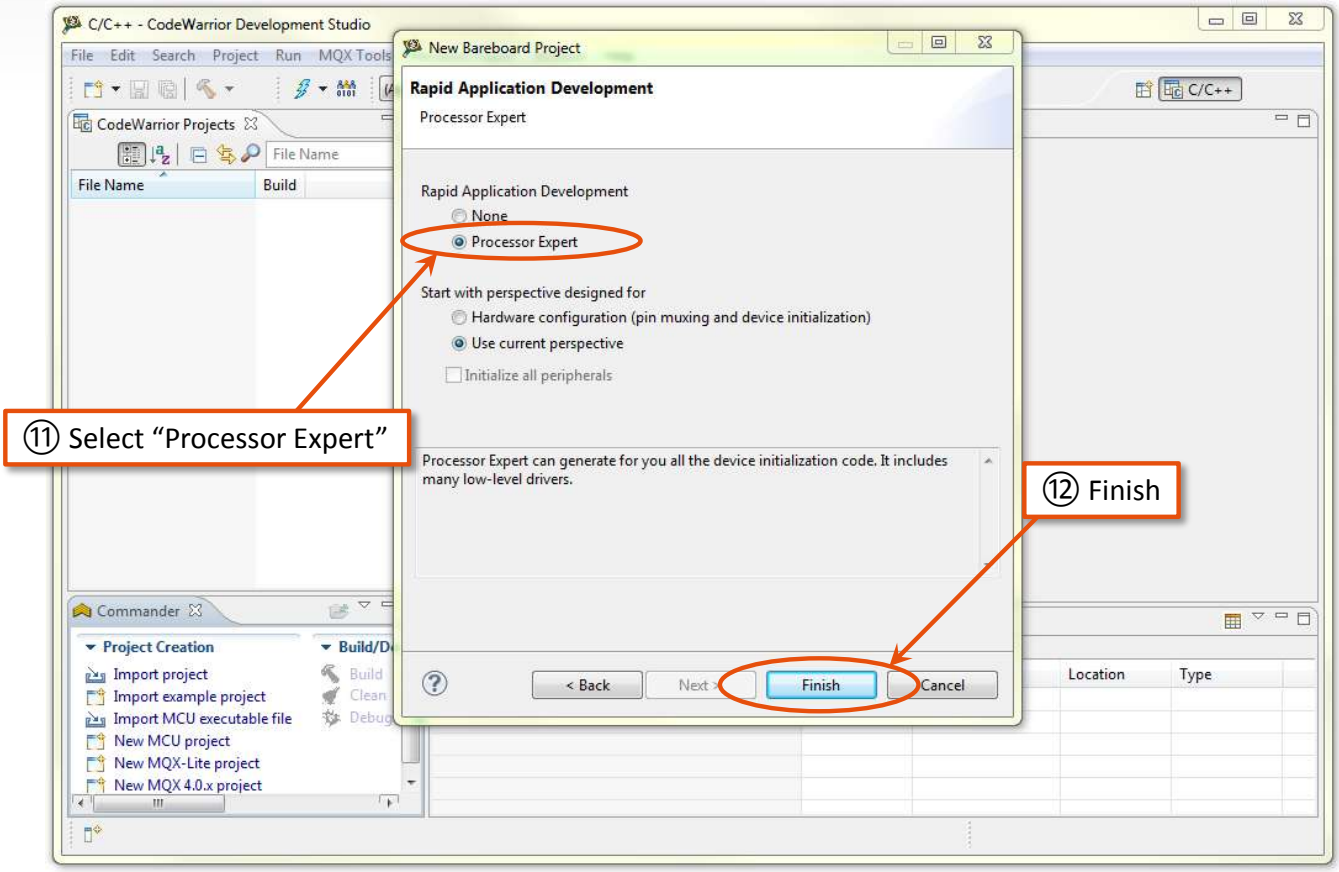
Select the Debug Connection



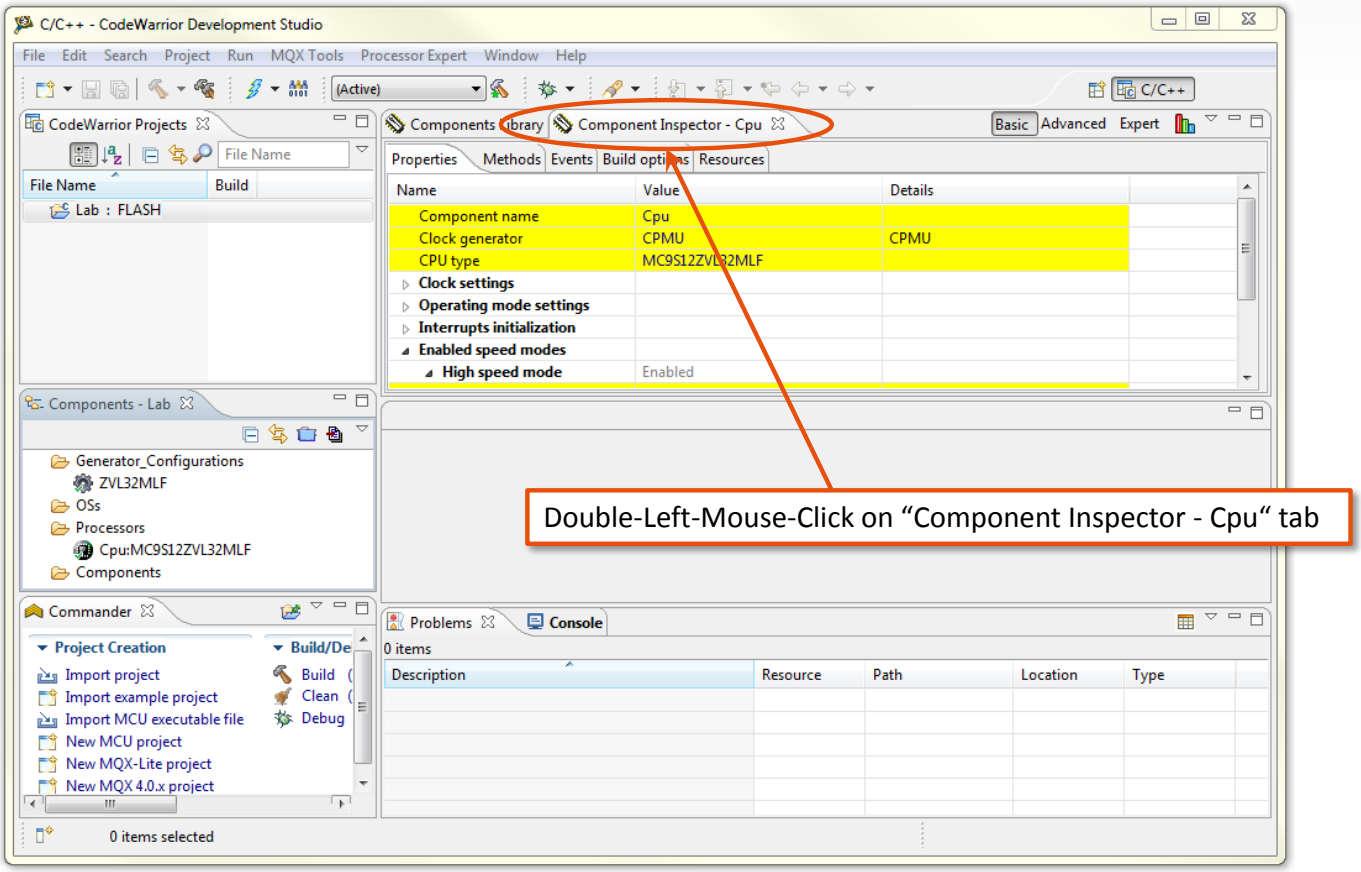
Language and Build Options



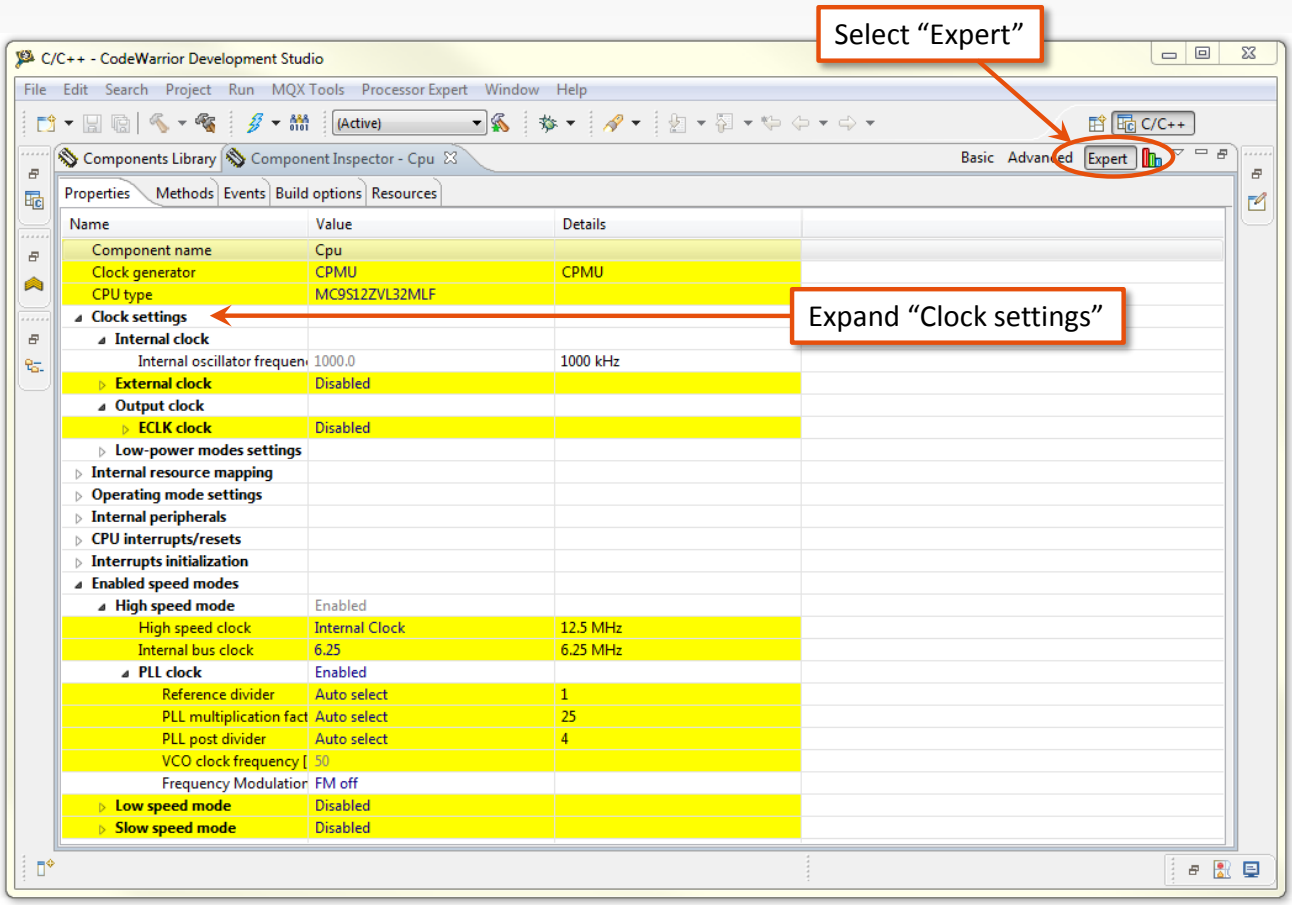
Enable Processor Expert



The C/C++ Perspective with Processor Expert



Component Inspector - Cpu



S12 Clock, Reset and Power Management Unit

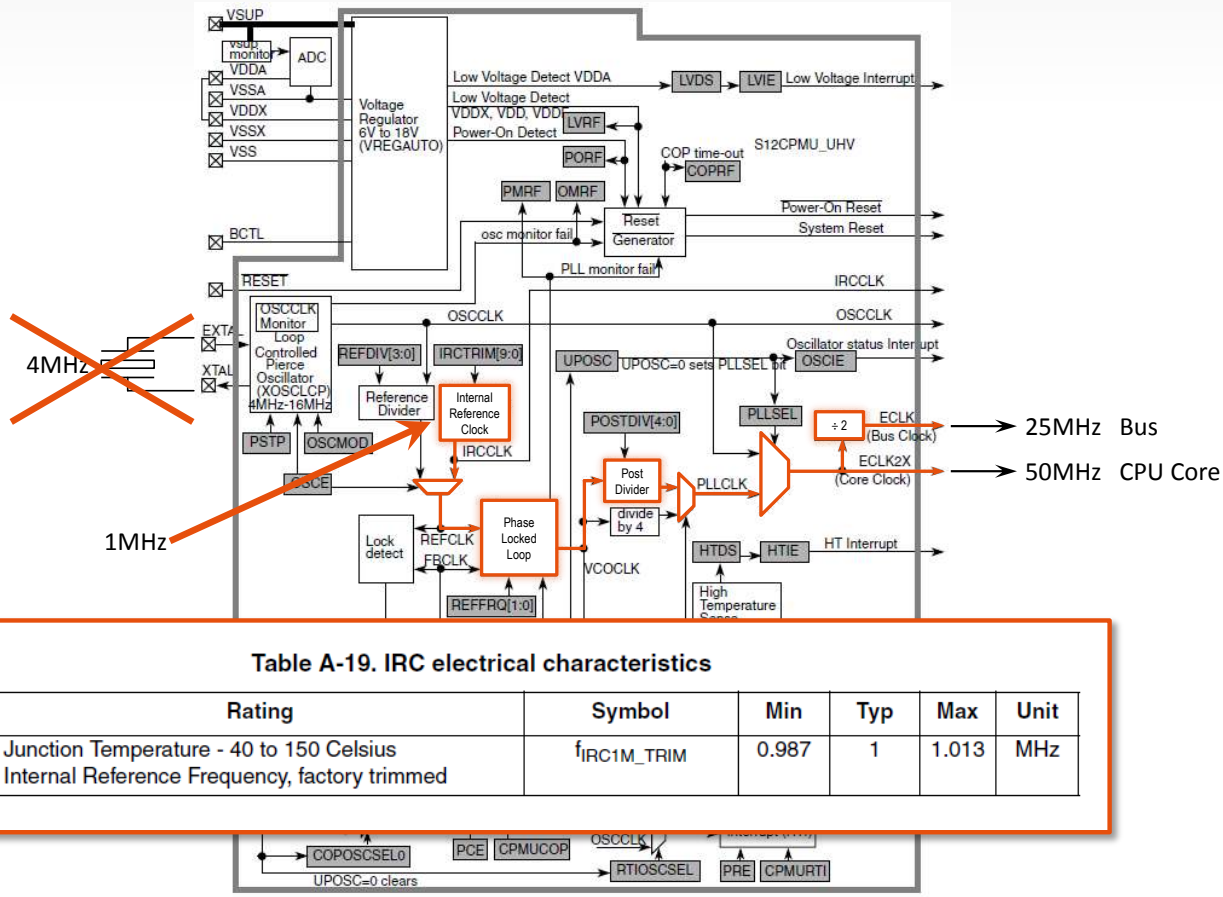
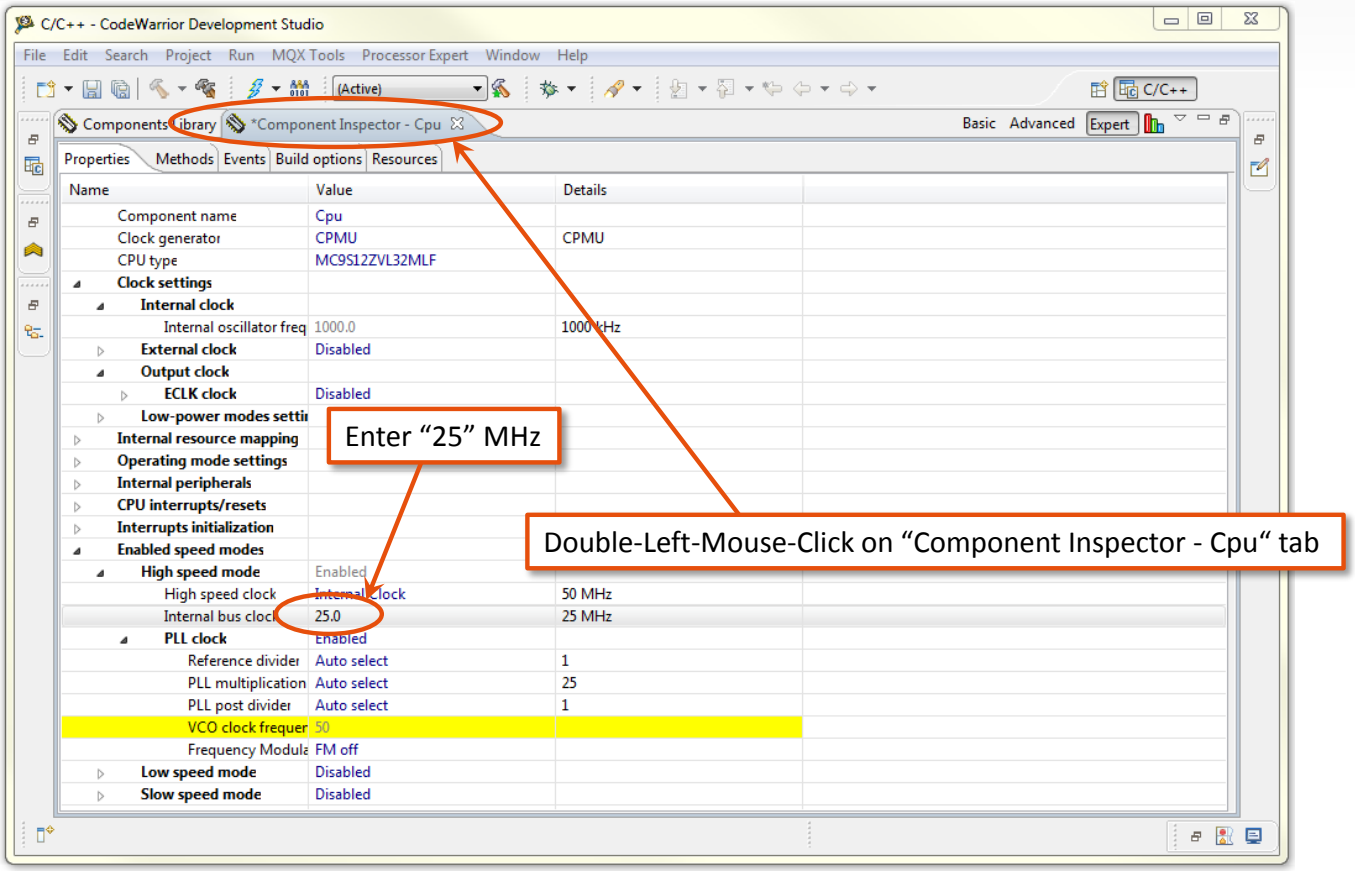


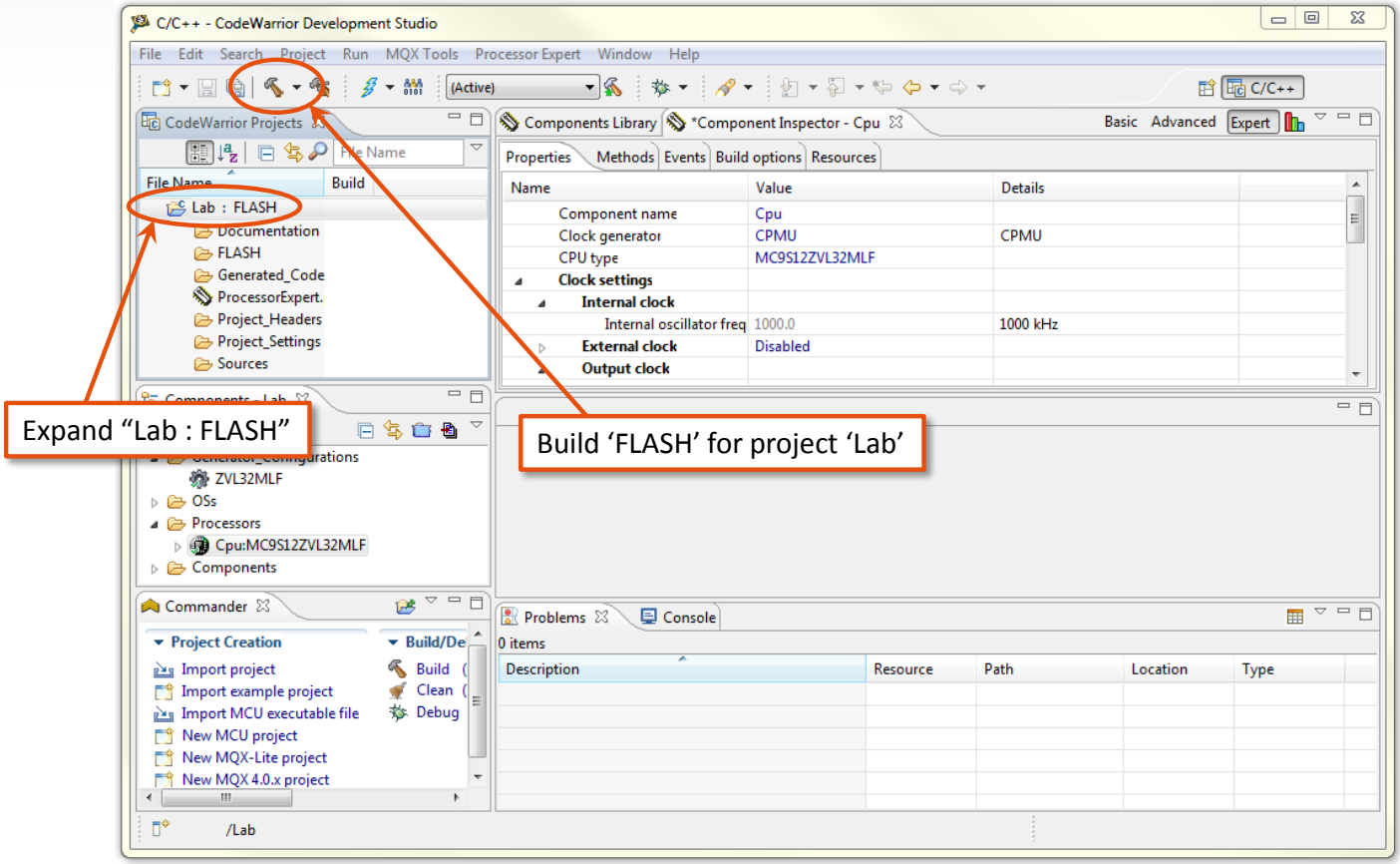
Table A-19. IRC electrical characteristics

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	P	Junction Temperature - 40 to 150 Celsius Internal Reference Frequency, factory trimmed	f_{IRC1M_TRIM}	0.987	1	1.013	MHz

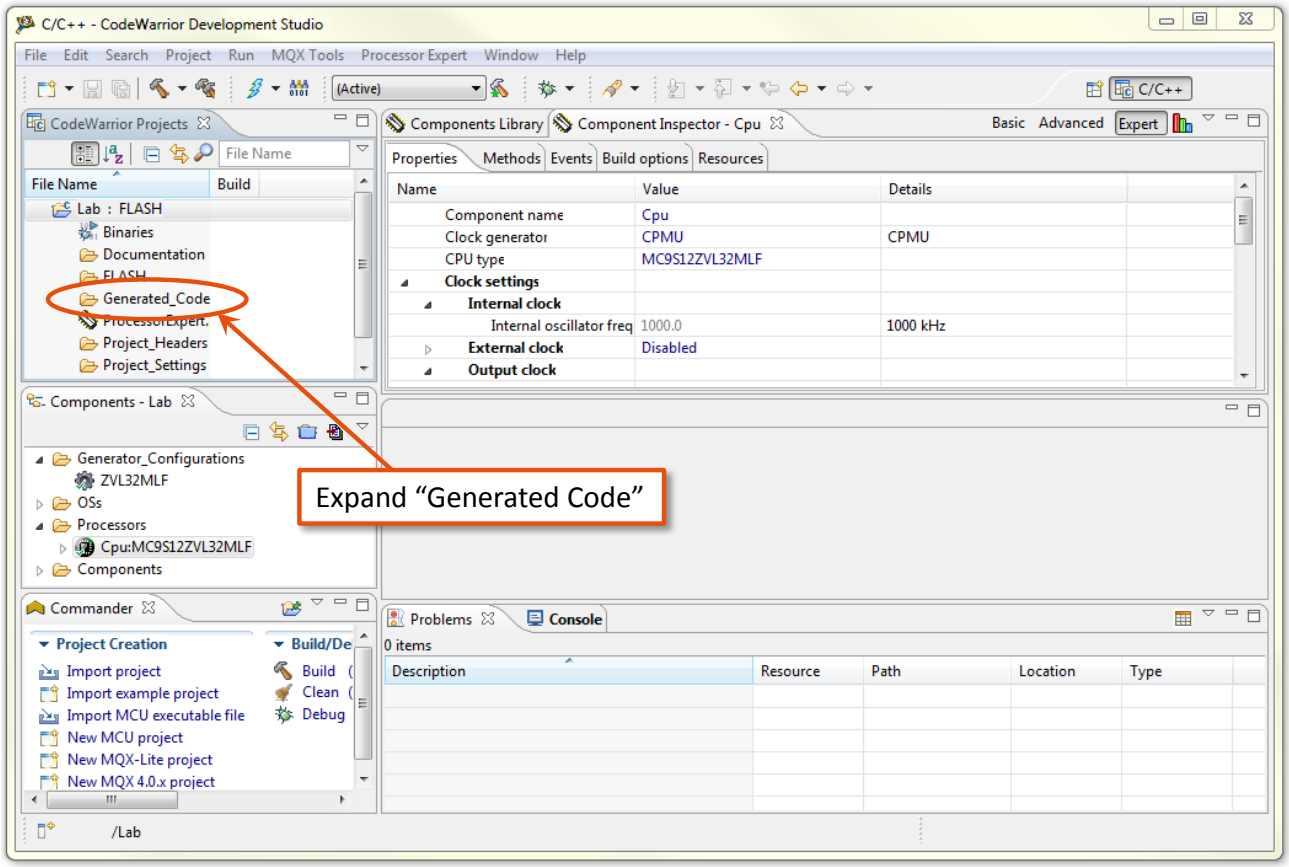
Component Inspector - Cpu



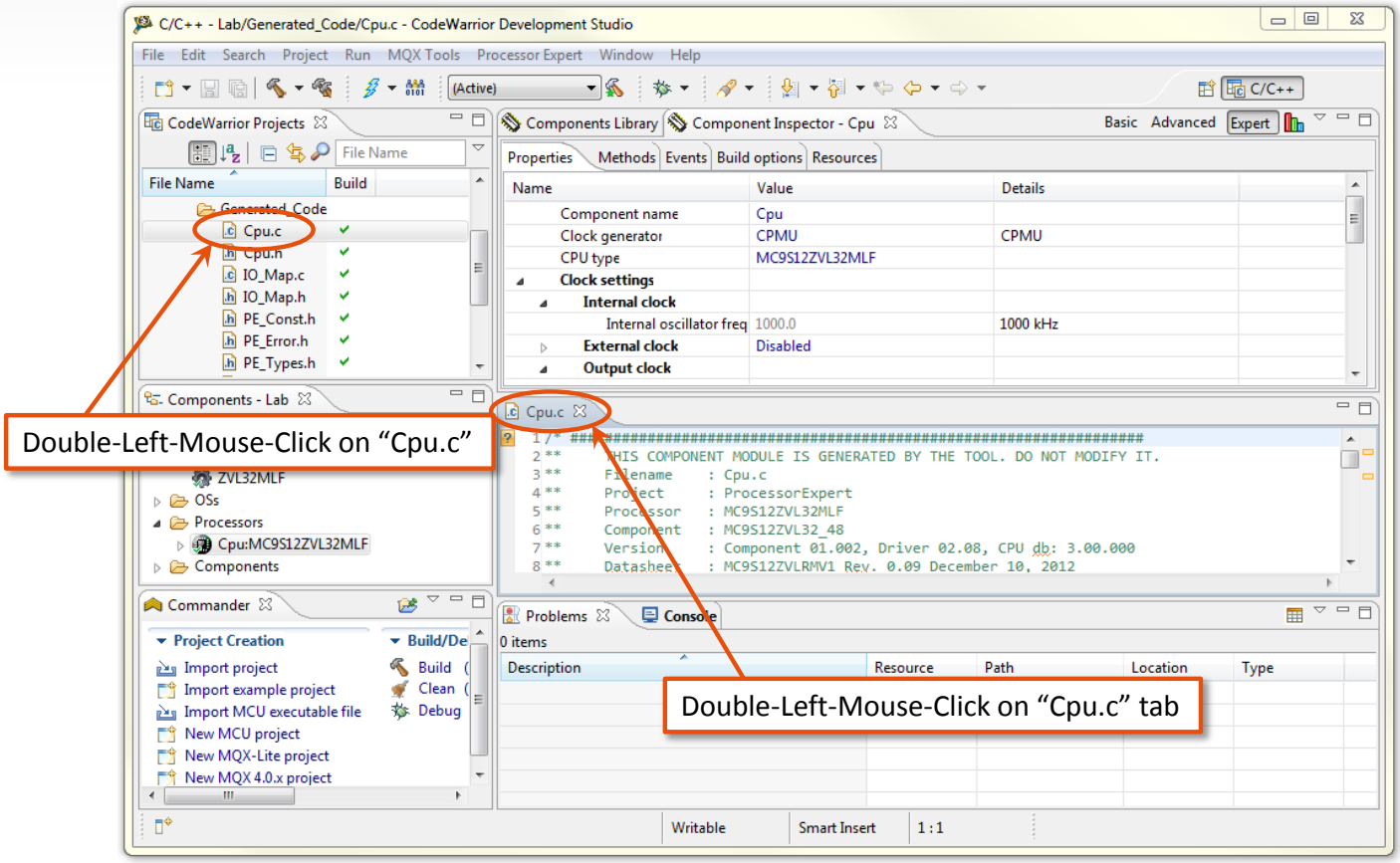
Build Project “Lab”



Investigate Processor Expert Generated Code



…vestigate Processor Expert Generated Code – “Cpu.c”



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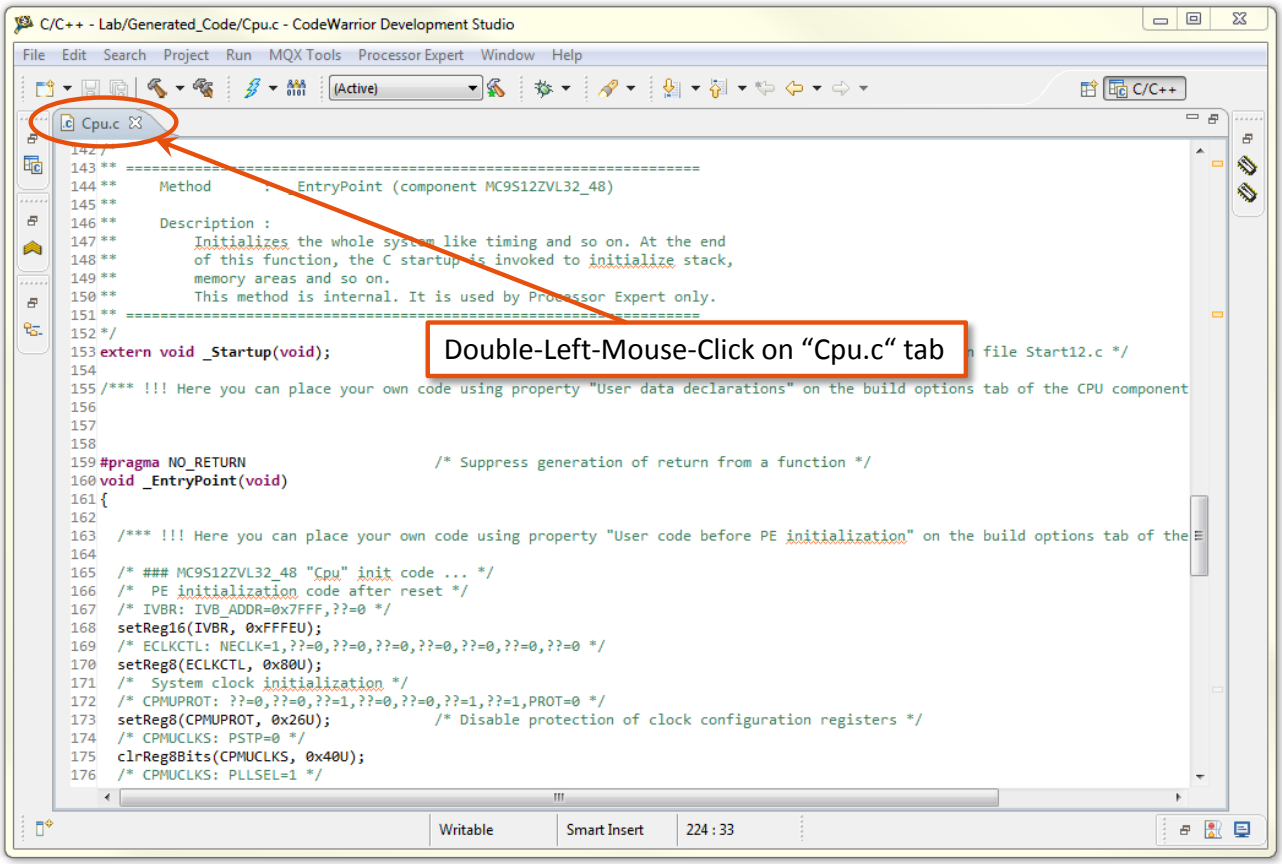
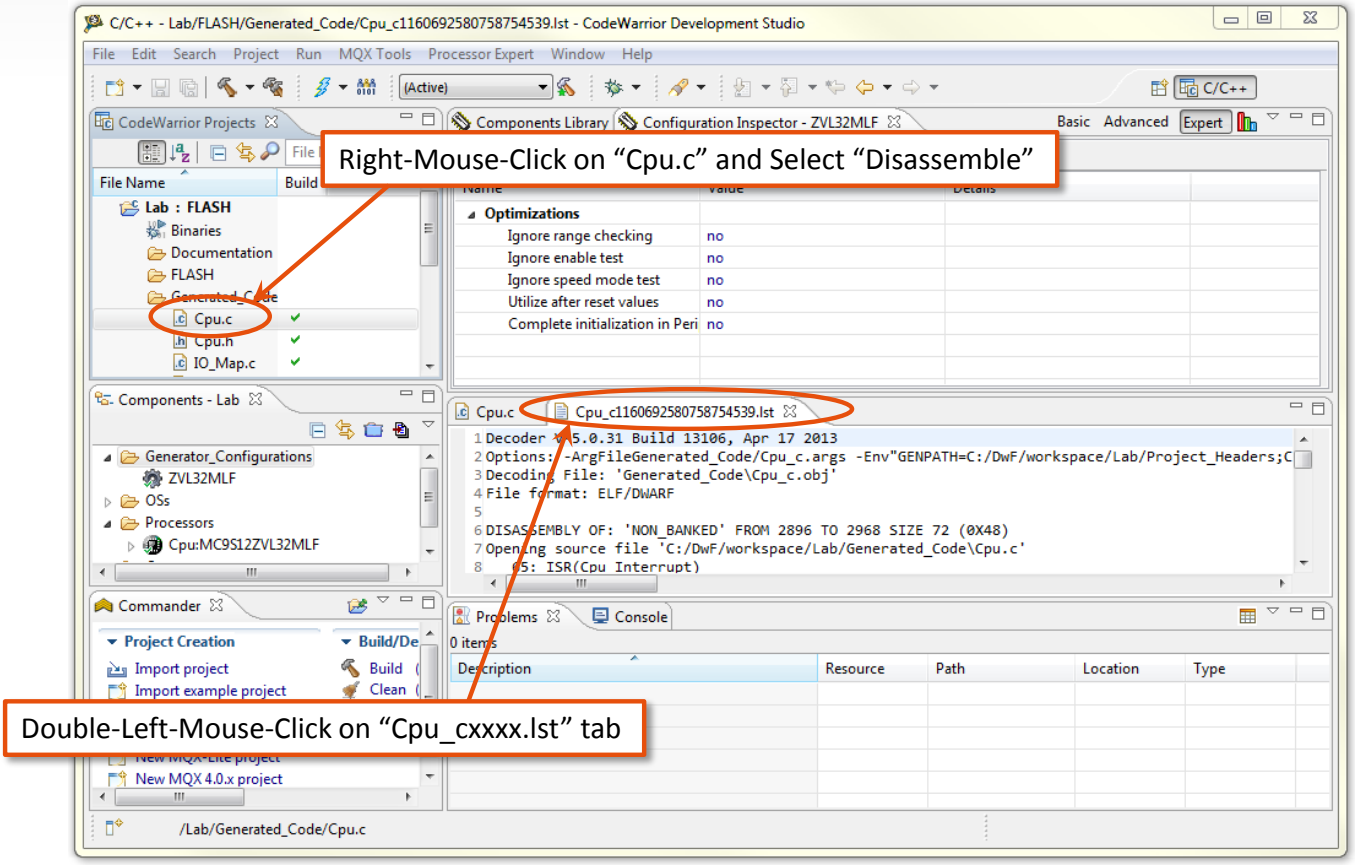
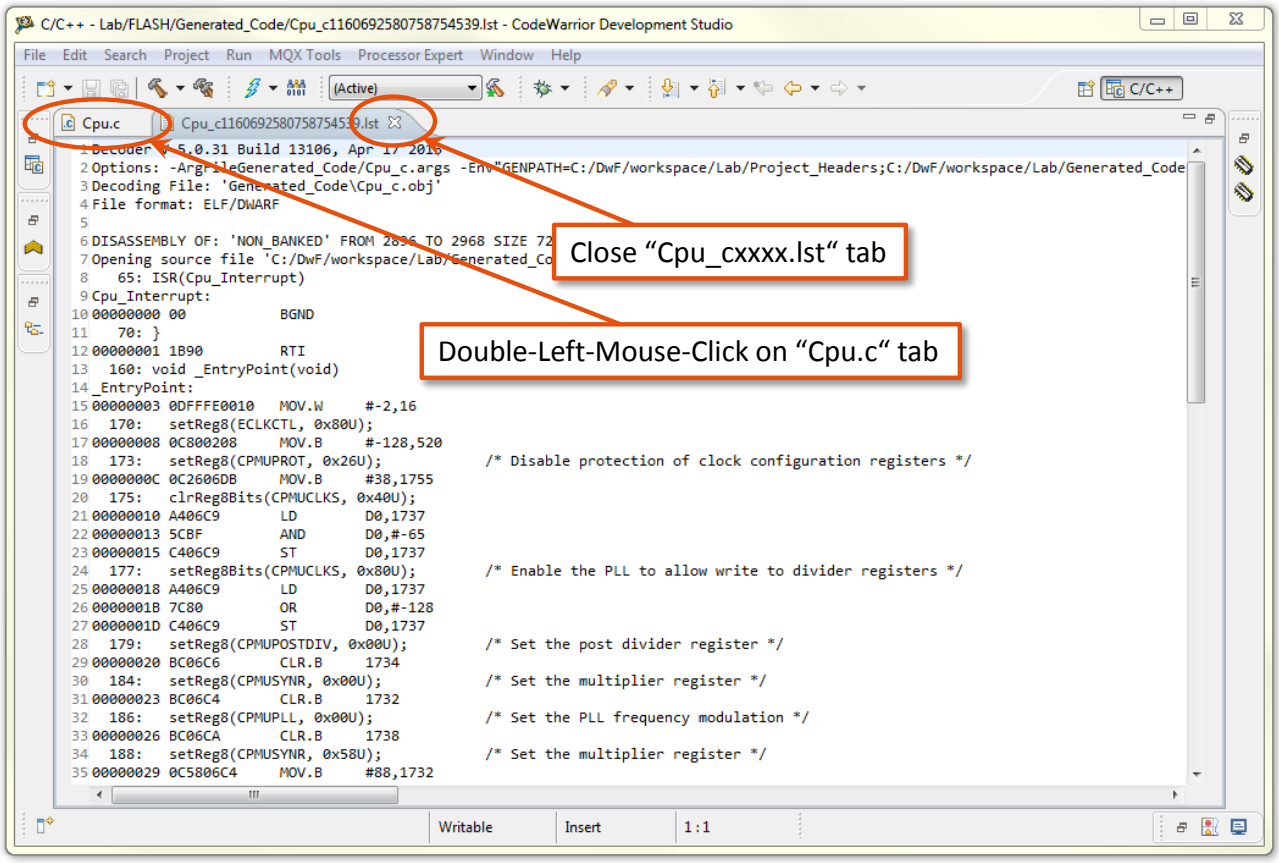


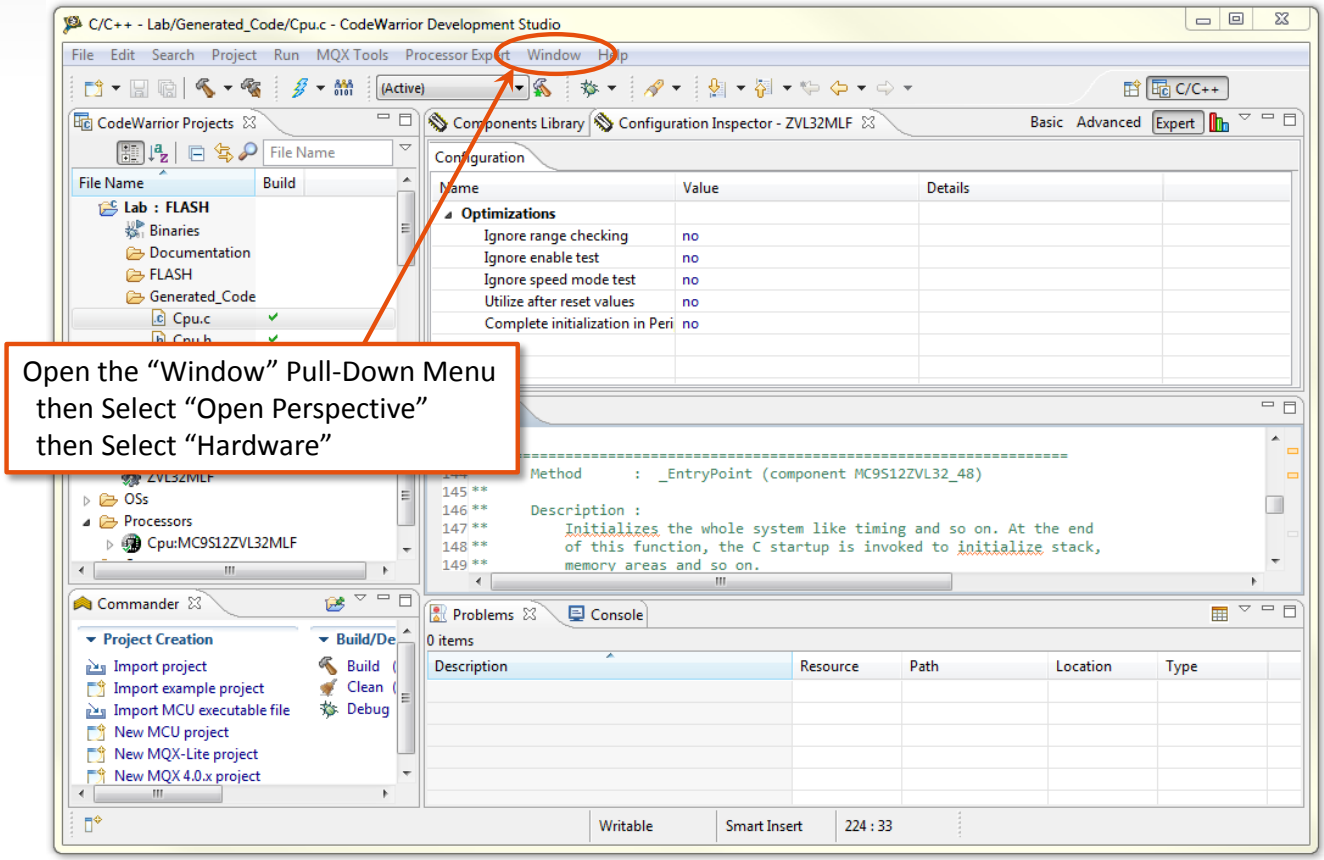
Disassemble “Cpu.c”



Investigate Assembly Language Code



The Hardware Perspective



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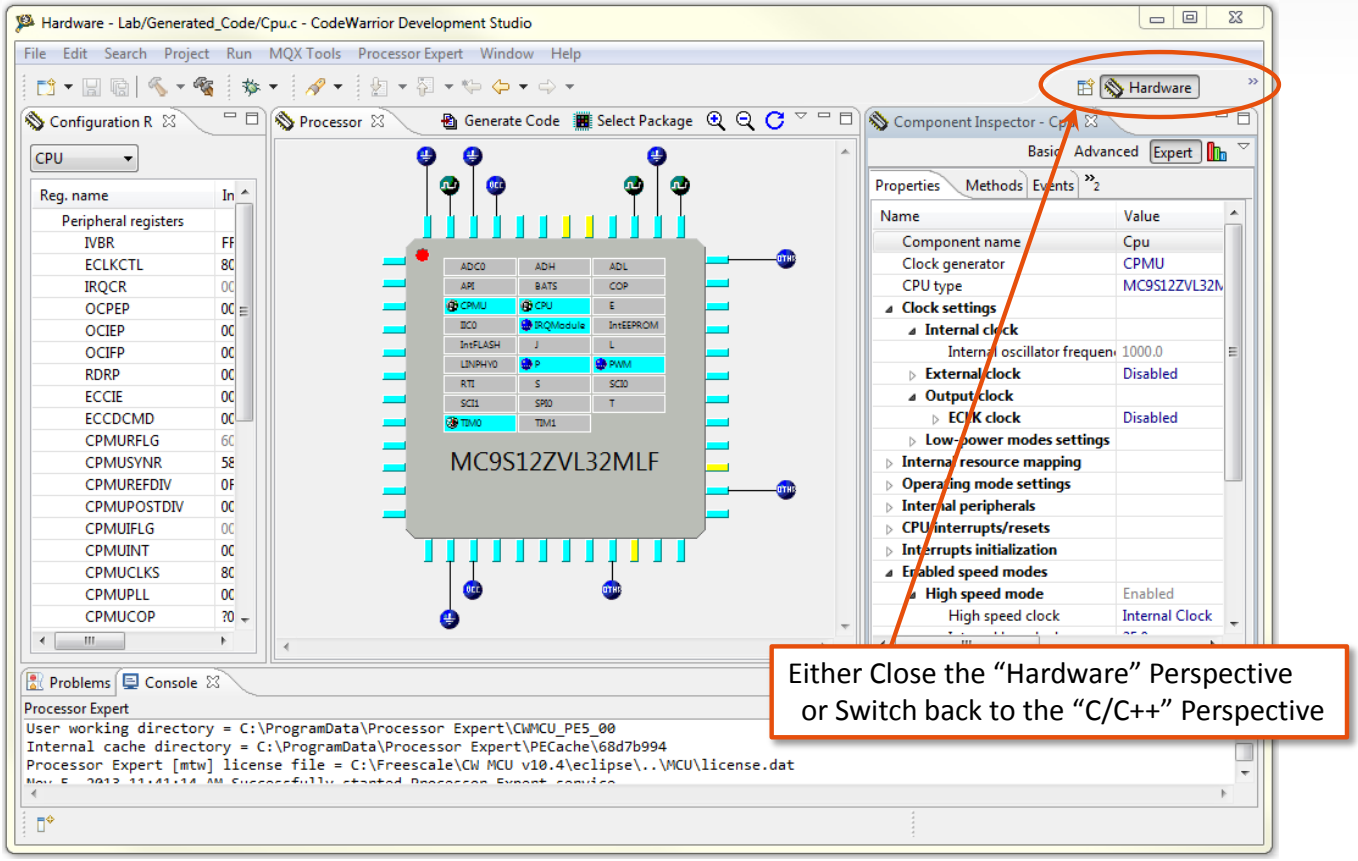
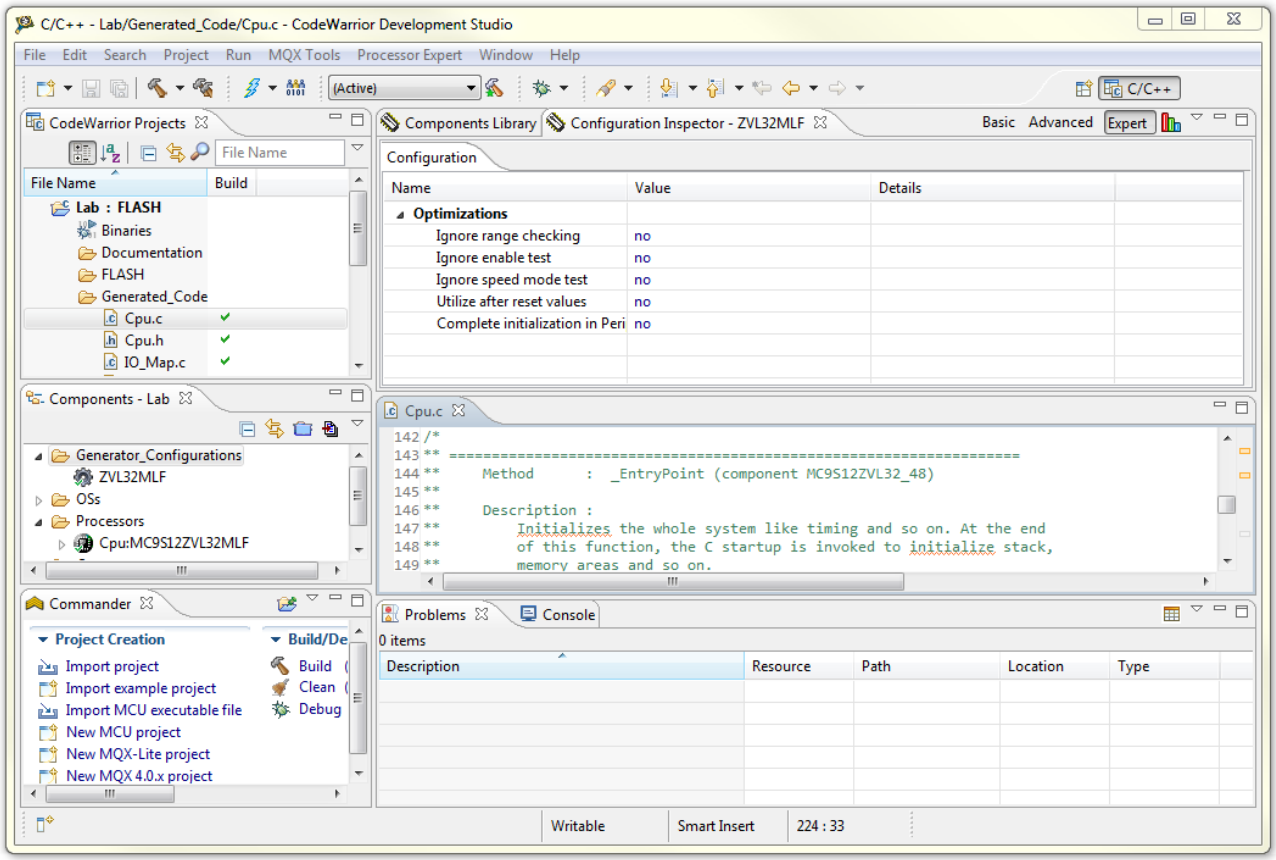


Ready for the Next Part of the Lab



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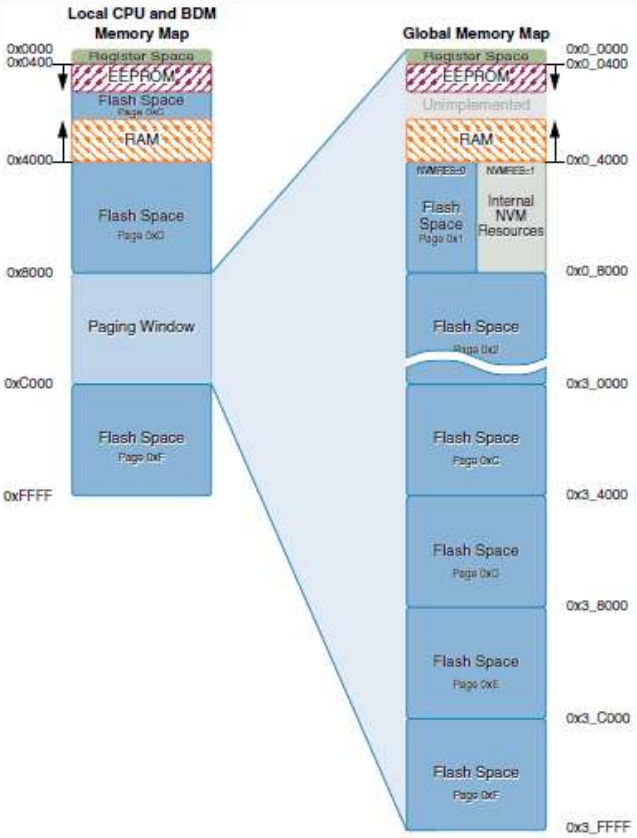
S12Z Core Overview

- The S12Z CPU is the next generation of CPU in the CPU12 line.
  - High-speed 16-bit processor with an expanded programmers model
  - Improved addressing modes support efficient use of the 16MB (24-bit) linear address space.
  - Improved support for C code-size efficiency and overall performance

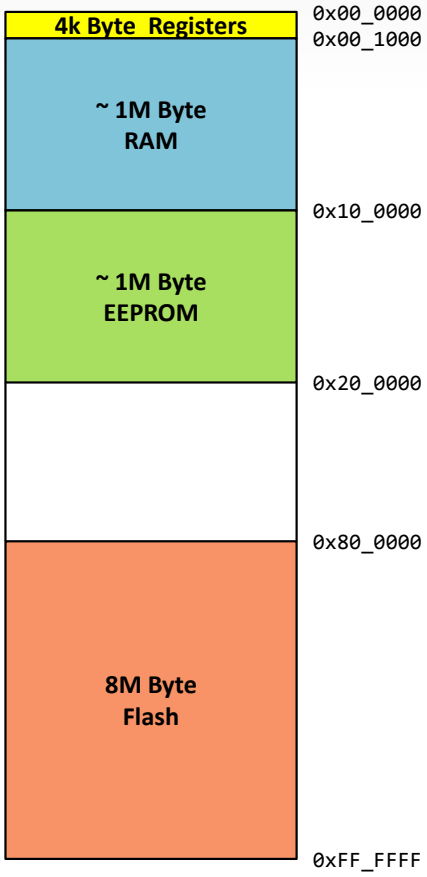
Linear vs. Paged Addressing Mode

- S12 MCUs typical architecture provides 64KB memory space
  - To achieve extended memory sizes, a paging mechanism is needed
    - 256 pages of 16kB each = 4MB maximum
  - Paging is one of the biggest dissatisfiers from customers' perspective

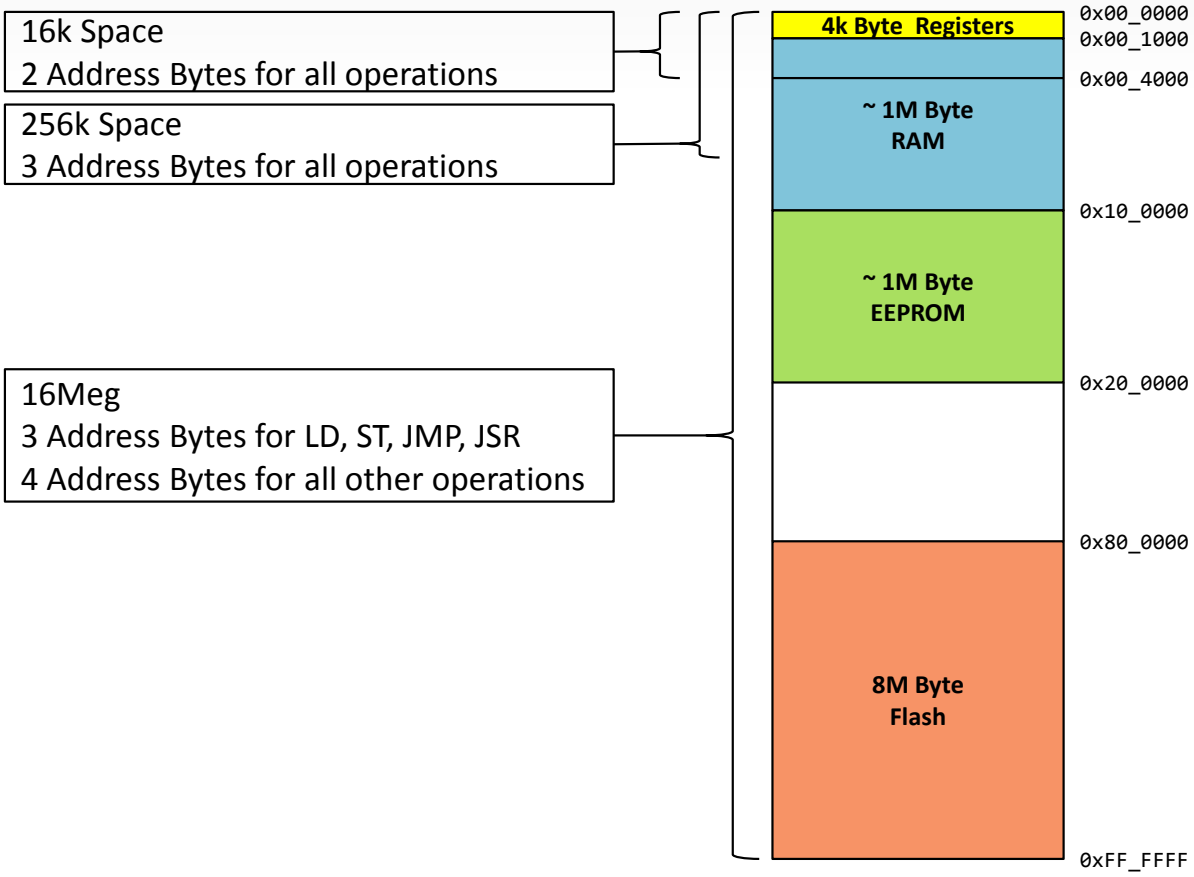


Linear vs. Paged Addressing Mode

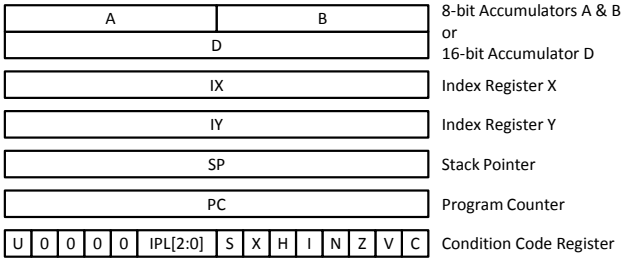
- The S12Z CPU includes a 24-bit address bus, which provides up to 16MB memory space
- Linear addressing simplifies memory accesses



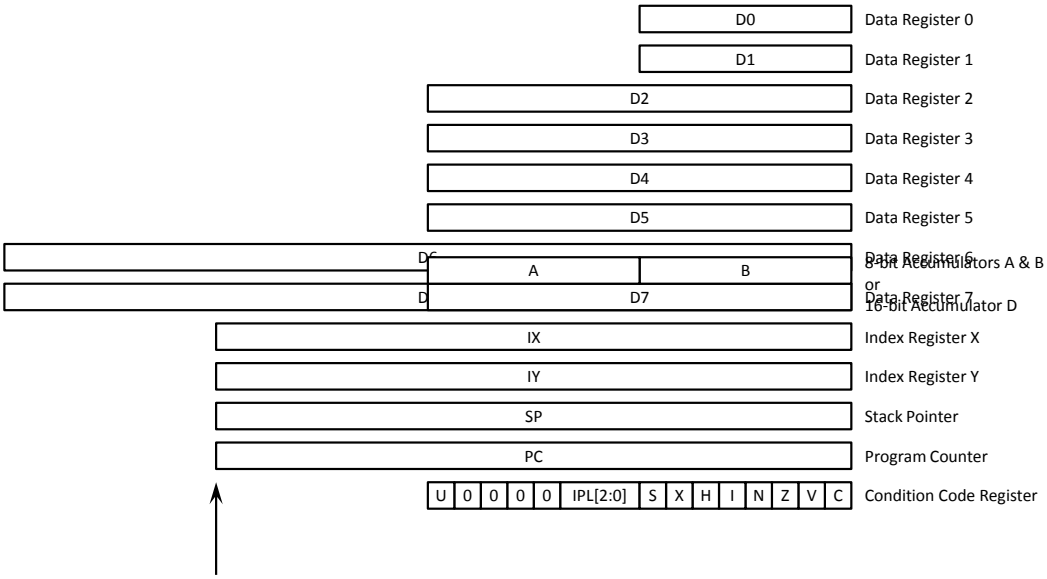
S12Z – Absolute Addressing



S12(X) CPU



S12Z CPU

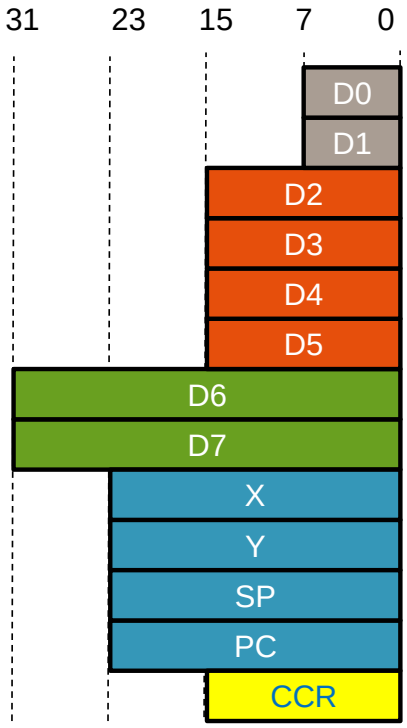


2^{24} = 16Mbyte Address Space

S12Z Core Architecture … a 16-bit MCU?

- It uses 32-Bit data paths, ALU, Data registers
  - Single-cycle 16x16 multiply (2.5 cycles 32x32)
  - MAC unit 32bit += 32bit*32bit (3.5 cycles)
  - Hardware divider 32bit = 32bit/32bit (18.5 cycles)
  - Single cycle multi-bit shifts (Barrel shifter)
  - Fractional Math support
- It uses a 24-bit address bus, Stack Pointer, Program Counter and Index registers
- Its native “int” data type is 16-bit, with 16-bit I/O data path
- It can handle 8-Bit data and indexes better than S12X
- CPU operates at 100MHz
  - Optimized bus architecture with 100MHz load and store to RAM
  - NVM works with 1 Wait-state => effective 20ns accesses
- Harvard Architecture => parallel code and data access
  - Instructions and addressing modes optimized for C programming and compiler

Expanded programmer’s model



S12Z Optimized Opcode Set

- Most used instructions are 8-bit opcodes
  - First Page

LD ST MOV MUL ADD SUB AND OR CMP BSET
Shifts BCLR BTGL INC DEC BRA JMP JSR

- Less used opcodes are 16-bit and require the prefix
  - Second Page

MAC MIN MAX ABS DIV MOD ADC SBC EOR

Bit Operations

- Bit operations were massively changed
  - BSET, BCLR, BRSET, BRCLR test only a **single bit** to save code space
    - Bit takes a maximum of **5 bits** instead of a mask for 32Bit takes 4 bytes!
    - >**90%** of all codes test/set/clear only one bit!
  - The bit number is either an **immediate** value or defined by an **accumulator**.
  - They can operate on a **memory location** but also on an **accumulator**.
  - The size of a memory operand can be 8, 16 or 32-bits or an accumulator
    - Example:

```
j = 1 << n; => CLR D2; LD D3,#n; BSET D2,D3
```

  - Bitfield operations were added: BFEXT, BFINS can extract or insert a bitfield
    - Example:

```
BFEXT    D7,D6,#7:23    => extracts 7 bits #23 from D6 into D7
```

S12Z – Enhanced Multiplication Instructions

S12(X):

MUL	(A) × (B) → A:B
EMUL(S)	(D) × (Y) → Y:D

S12Z:

MULU	(D*j*) × (D*k*)	→ D*d*	QMULU	(D*j*) × (D*k*)	→ D*d*
	(D*j*) × IMM	→ D*d*		(D*j*) × IMM	→ D*d*
	(D*j*) × (M)	→ D*d*		(D*j*) × (M)	→ D*d*
	(M1) × (M2)	→ D*d*		(M1) × (M2)	→ D*d*
MULS	(D*j*) × (D*k*)	→ D*d*	QMULS	(D*j*) × (D*k*)	→ D*d*
	(D*j*) × IMM	→ D*d*		(D*j*) × IMM	→ D*d*
	(D*j*) × (M)	→ D*d*		(D*j*) × (M)	→ D*d*
	(M1) × (M2)	→ D*d*		(M1) × (M2)	→ D*d*

Fractional Math

Fractional Math Support - Instructions

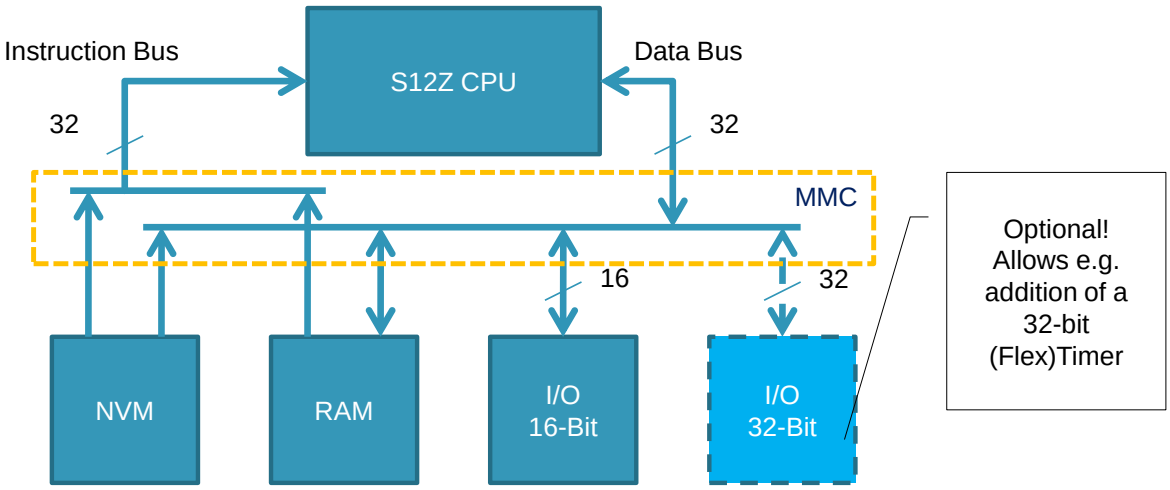
- Fractional Multiply (Signed & Unsigned)
  - Multiplies two signed/unsigned fractional two's complement operands and stores the signed fractional two's complement result to register Dd.

- Saturate
  - Saturate the content of the operand register using the information stored in the overflow (V-) and negative (N-)flags by a previous instruction.

- Count-Leading-Bits
  - Counts the number of leading sign-bits in the source register, decrements this number and then copies the result into the destination register.

S12Z Platform Architecture

- Harvard Architecture (Parallel Data and Code access)



S12Z vs. S12X – Features

Attribute	S12Z	S12XE
Architecture	Harvard	Von Neumann
Address space	16MByte Linear	64KByte Linear (up to 4MByte Paged)
Data Bus Width	32-Bit RAM & Flash, 16-Bit I/O	16-Bit
ALU Width	32-Bit	16-Bit
Data Registers	2 x 8-Bit, 4 x 16-Bit, 2 x 32-Bit	2 x 8-Bit (can be used as a single 16-Bit accumulator)
Pointers	2 x 24-Bit	2 x 16-Bit

S12Z vs. S12X – Performance

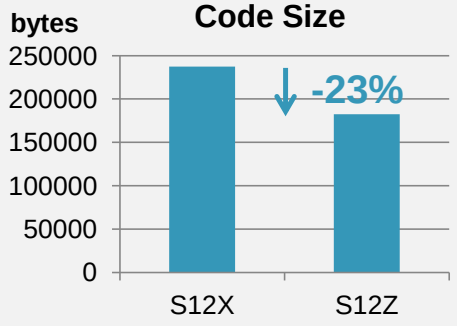
Attribute	S12Z		S12XE	
Bit Shifter	32-bit multi-bit	1 cycle	16-bit single-bit	2cycles
Multiplier	32*32 16*16	2.5cycles 1cycle	16*16	1cycle
Divider	32 = 32/32	18.5cycles	32 = 32/16	11cycles
MAC	32 += 32*32	3.5cycles	32 += 16*16	13cycles
Fractional math support	Yes		No	
Bus speed	50MHz		50MHz	

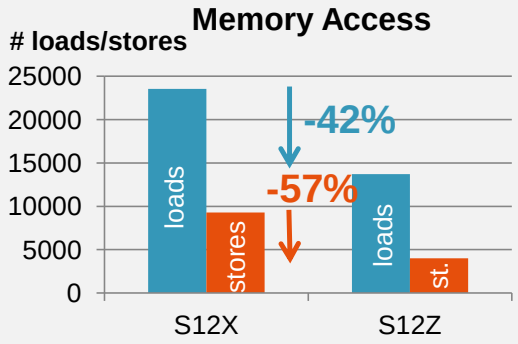
- CPU operates at up to 100MHz, bus at 50 MHz
  - RAM bus can load and store w/ 100MHz
  - I/O buses @50MHz to reduce power consumption and die area

S12Z Benchmarks Results

- **S12Z typically saves 20% code size versus S12X**
- **S12Z typically uses 30% less memory accesses than S12X which saves power**

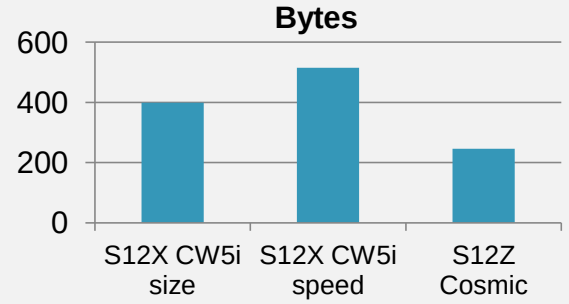
Large Application Code Example:

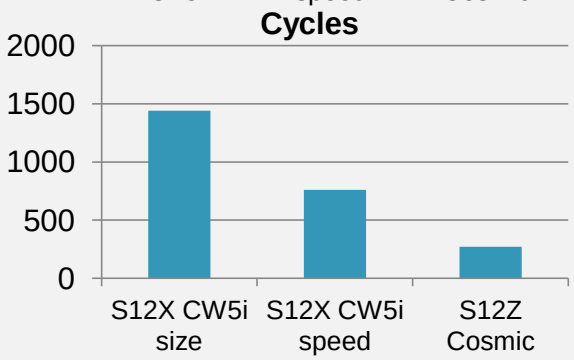




Digital Filter:

S12Z is faster and denser than any optimization option of S12X





In Depth Code Size Analysis

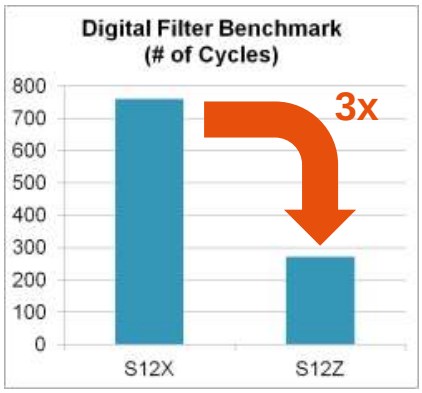
Feature	S12X	S12Z	Comment
Code Size	237277	182362	-23%
pg1	86.3%	96.9%	Shows well chosen pg1 instructions
Loads	23550	13725	-42%
Stores	9280	4015	-57%
Moves	4347	4332	About equal

- Code is about 200k byte large Body Application
  - Significant code size savings
  - Large reduction of memory instructions (not accesses!)
    - => Power Savings expected

S12Z Performance Benefits

Improved Performance for Motor Control

- 100 MHz CPU @ 50 MHz bus speed
- Harvard architecture accelerates data handling



- Fractional math instructions added

Improved Software Friendliness

- 24-bit linear address map to ease software development and porting
- Added 8- and 32-bit registers to allow further compiler code size optimization

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- S12ZVL for General Purpose LIN
- S12ZVC for General Purpose CAN
- Lab 2
  - Developing a Project for the S12ZVL

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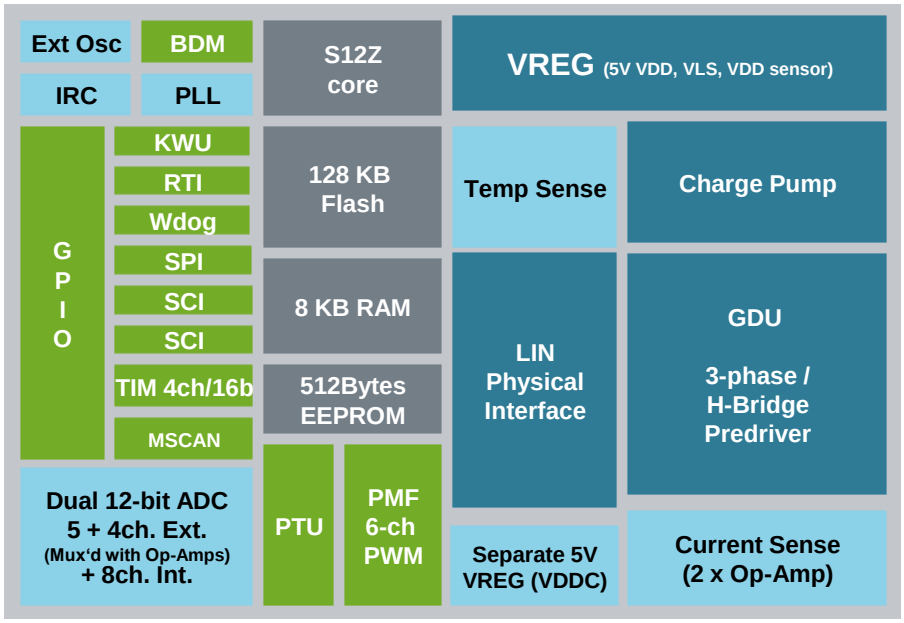
Overview of S12ZVM Feature Set

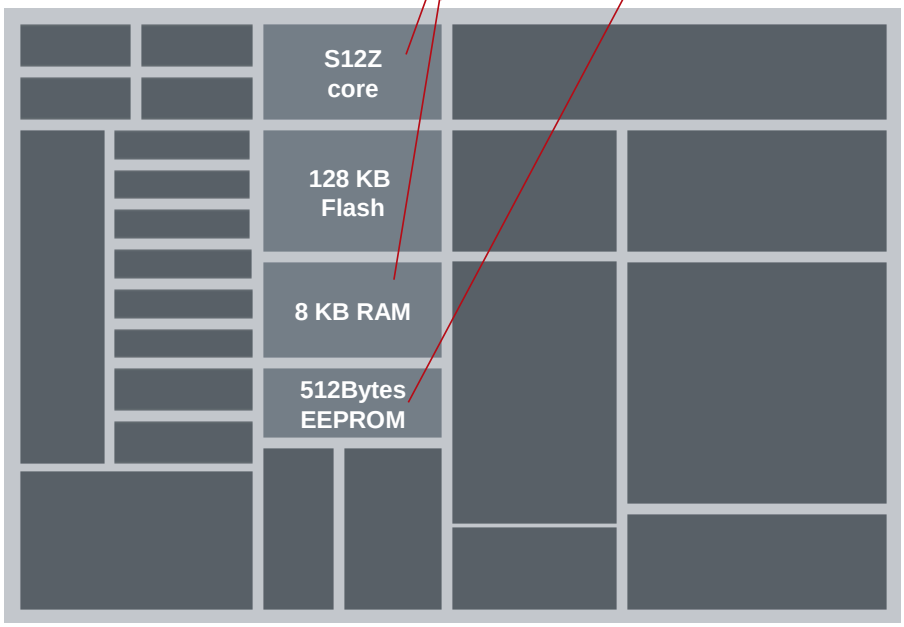


Overview of S12ZVM Feature Set

New S12Z CPU
- Up to 100MHz
- 32-bit ALU & 32bit MAC unit,
- Optimized 32-bit math. operations

Safe RAM
- ECC

Flash& EEPROM
- ECC
- Memory Protection
- Margin Read



Overview of S12ZVM Feature Set

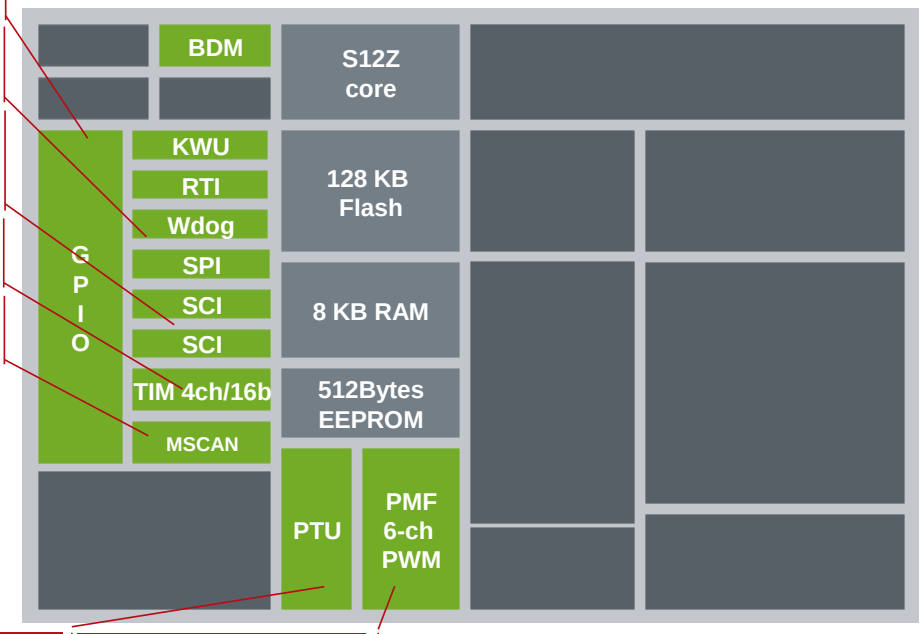
Sensor Supply
• 20mA I/O for sensor

Window Watchdog
• Independent RC osc

2 UARTs
• one linked to LIN Phy
• 2nd as test interface

Multiple timers
• IOC/periodic wakeup

CAN Option
• CAN controller

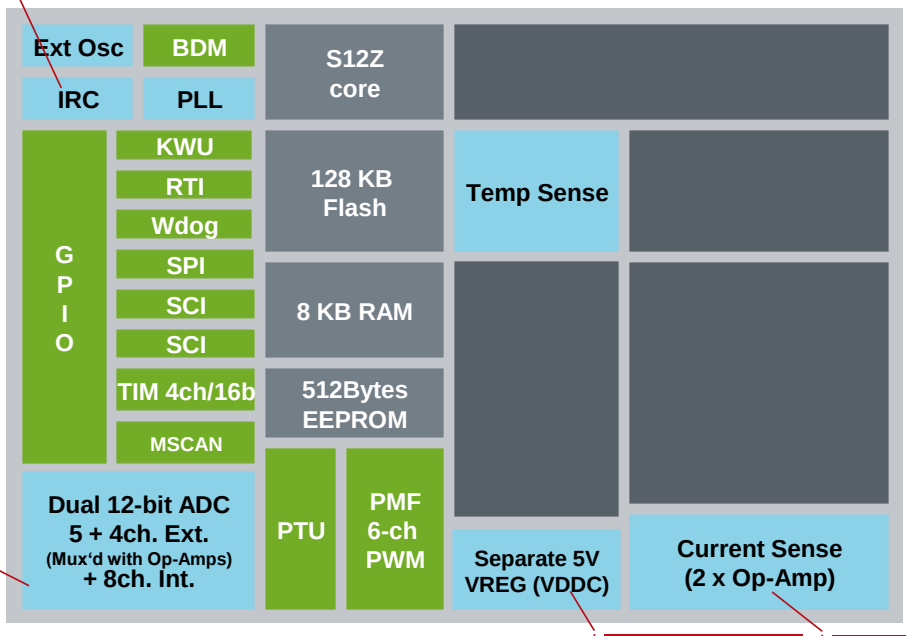


Programmable Trigger Unit
• synchronize ADC to PWM
• Trigger Command list with up to 32 triggers per cycle

PWM Module
• Complementary mode with deadtime ctrl.
• Fault protection
• Double-Switching

Overview of S12ZVM Feature Set

Internal RC osc.
• +/-1.3% over tmp

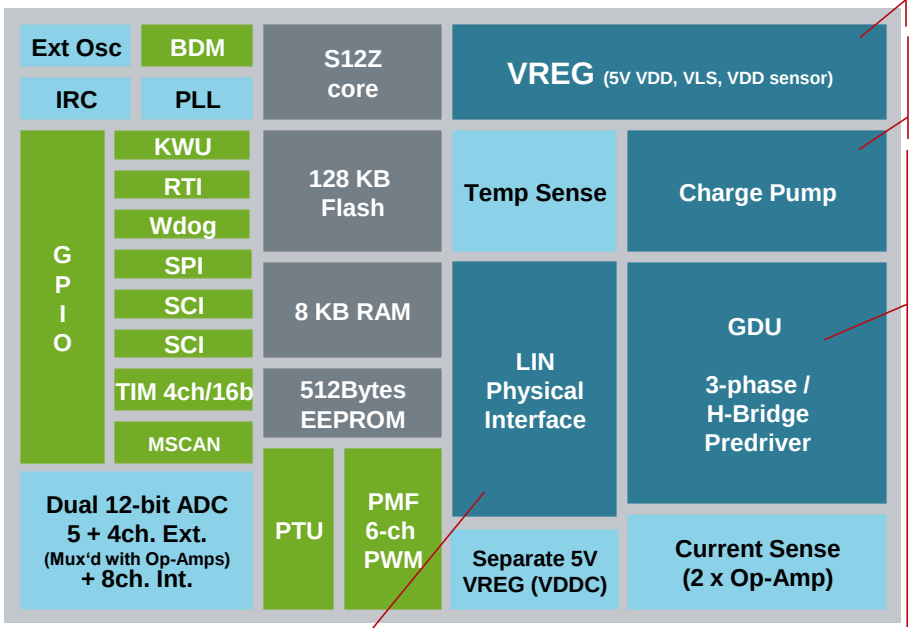


Two 12-bit ADC
• List Based Architecture allows flexible definition of order and number of conversions
• 2.5µs conv. time

CAN Support
• 5V Vreg controller for external transceiver

Current Sense Amplifiers
• 2-shunt system supported with additional selectable over-current protection comparator

Overview of S12ZVM Feature Set



Voltage Regulator
- Boost Option
- Support for external ballast transistor
- Vbat sense

Charge Pump
- Optional to support 100% duty cycle

Gate Drive Unit
- Operational from 3.5V to 26V
- Bootstrap circuit based
- 11V Vreg
- Phase comparators
- Desaturation comp. for HS/LS protection
- Under-/Over-voltage detection
- DC-link and phase voltage internally accessible on ADC
- Selectable HS/LS slew rate

LIN Phys. Interface
- 250kb/s fast mode
- +/-6kV

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• +/-1.3% over tmp

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• 20mA I/O for sensor

Window Watchdog
• independent RC osc

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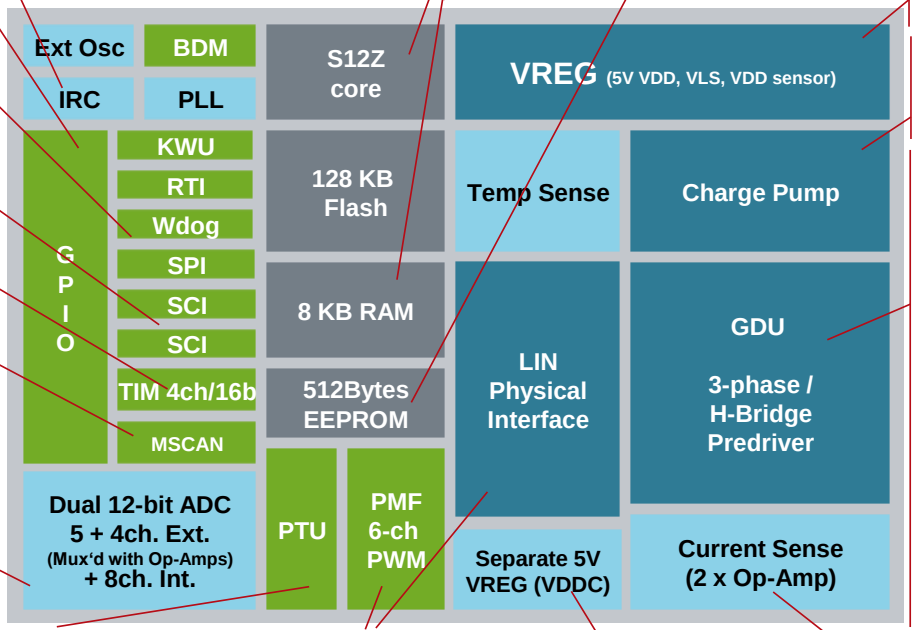

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• +/-6kV

CAN Support
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Current Sense Amplifiers
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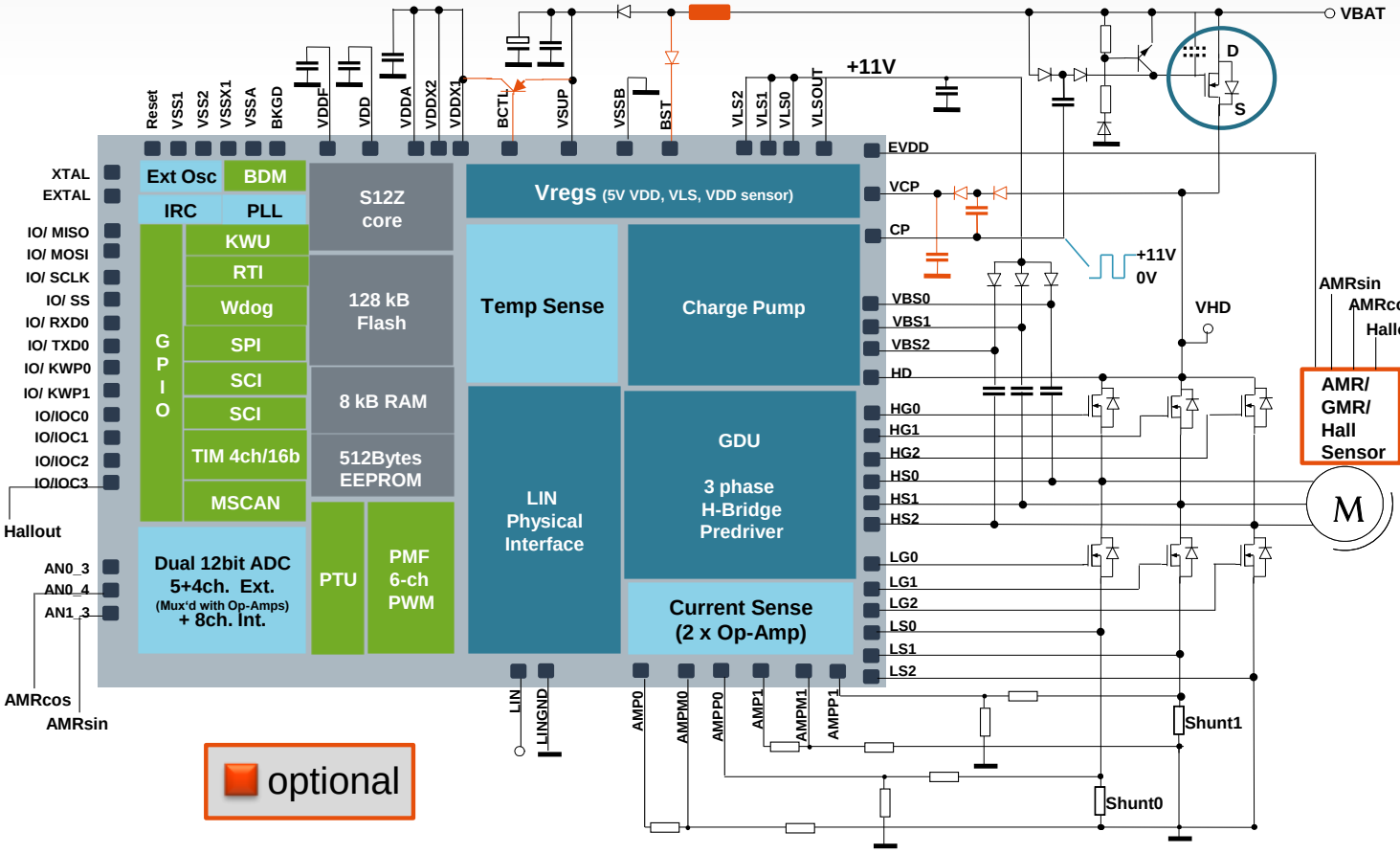
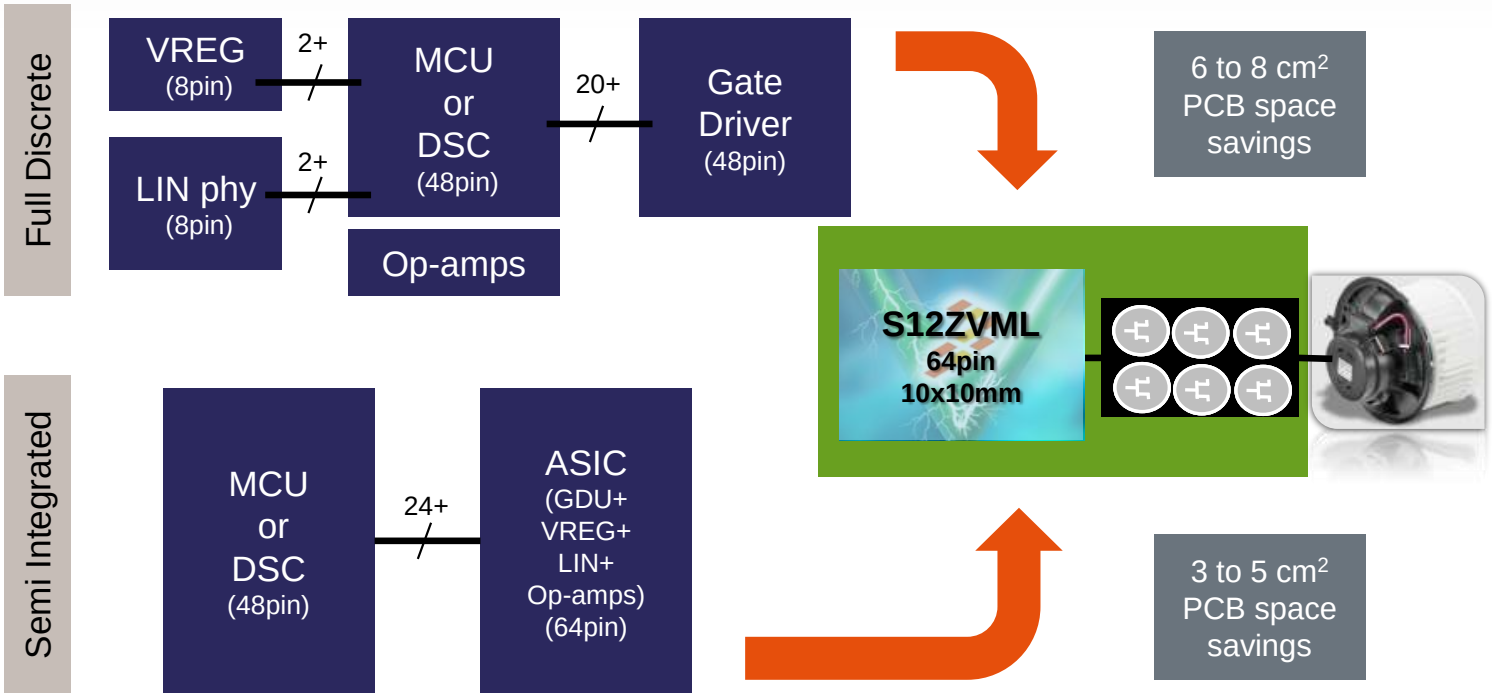
S12ZVML Application Schematic

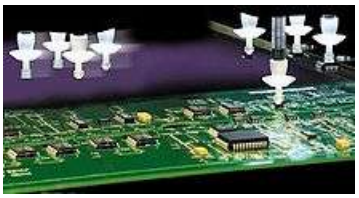


Space Savings with S12ZVML



Manufacturing Cost Benefits

Multiple effects of eliminating ICs or passive components:
- Material : PCB space, Cu tracks, test points, soldering
- Pick & place
- Testing at board level
- Inventory management

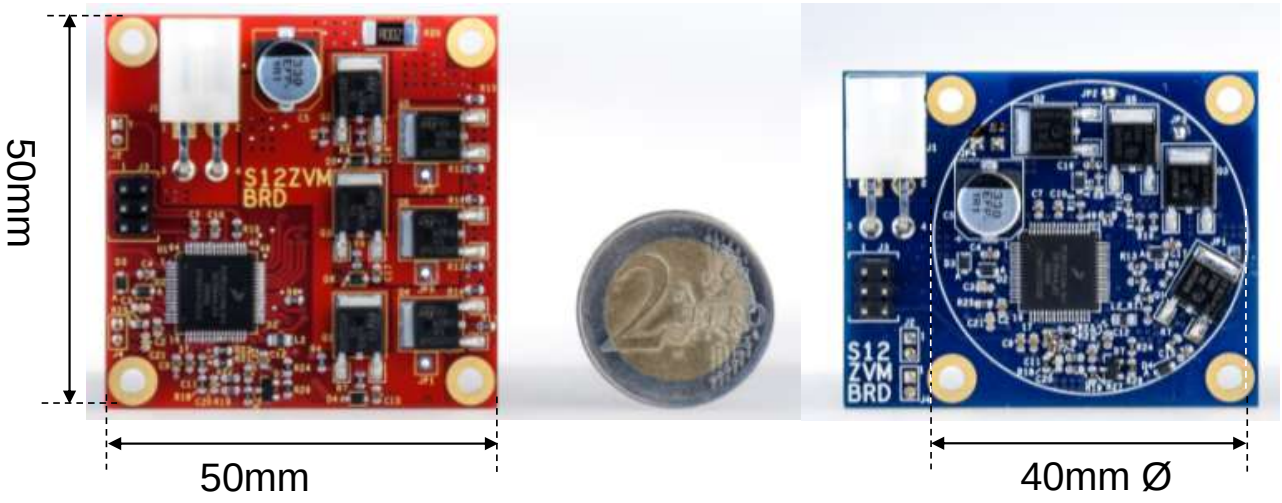


SMTA
Surface Mount Technology Association

SMTA (Surface Mount Technology Association):
- NMACPCs (Non-Material Assembly Cost Per Component) range from $0.01 to $0.15 per component assembled
- NMACPI/O (Non-Material Assembly Cost Per Input/Output) range from $0.005 to $0.01 per I/O assembled.

Highest level of Integration

Of your BLDC system:



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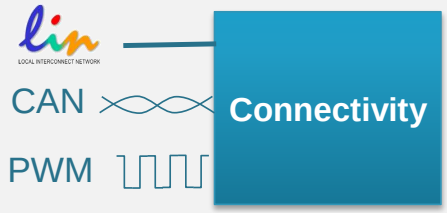
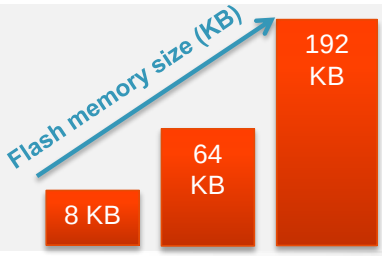
Ultimate Flexibility and Scalability



CAN or LIN support with on-chip physical interface

On-chip 12 V voltage regulator for flexible on- and off-chip supply



Range of memory options address multiple applications and allow for platform design

True platform solutions through hardware and software reuse

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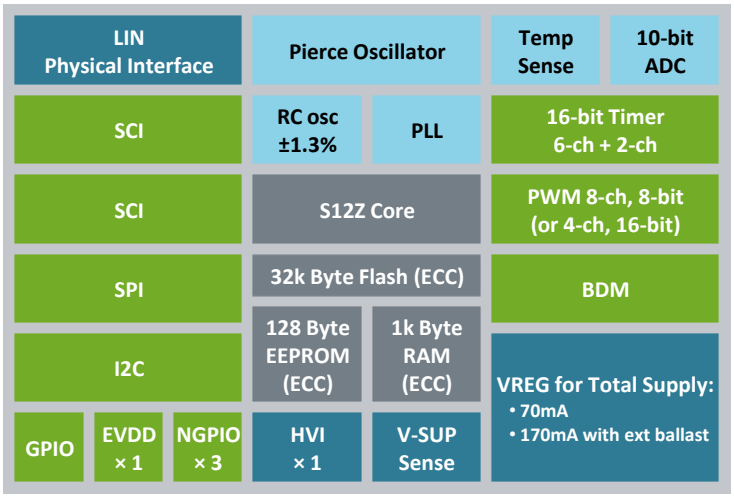
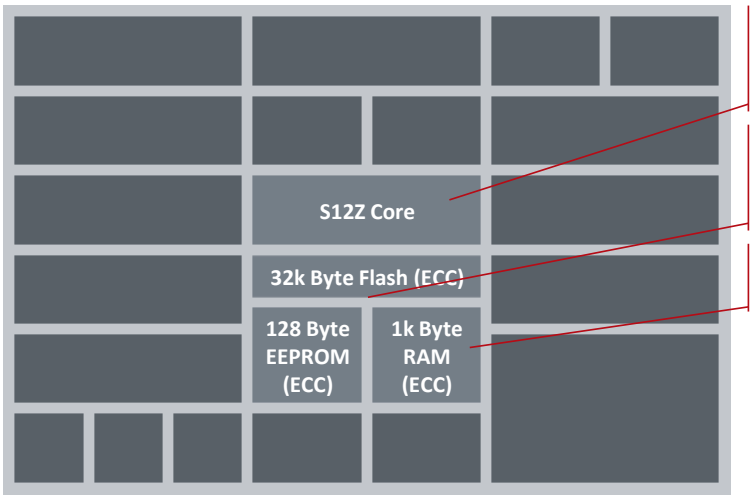
Overview of S12ZVL Feature Set



Overview of S12ZVL Feature Set

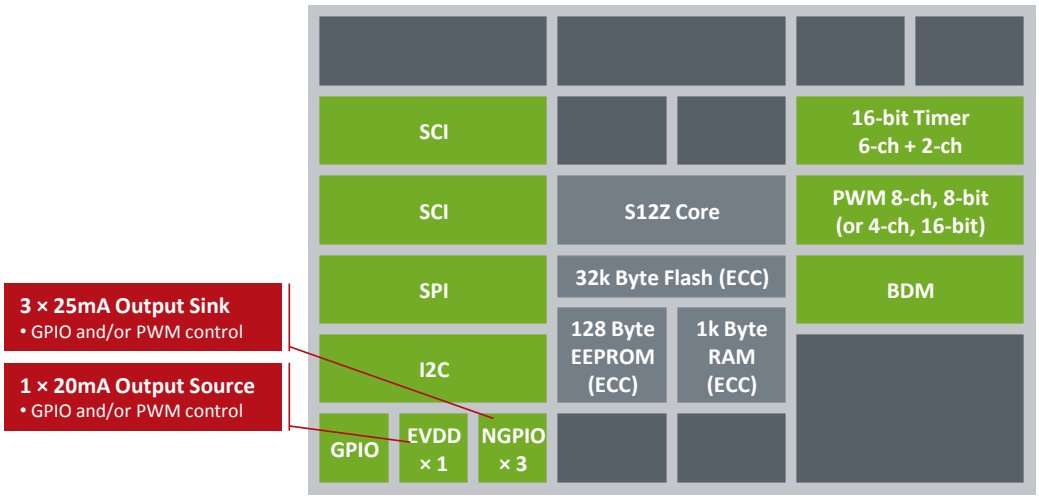


New S12Z CPU
- up to 50MHz
- 32-bit ALU & 32-bit MAC unit
- Optimized for 32-bit math operations

Flash & EEPROM
- with ECC
- Memory Protection
- Margin Read

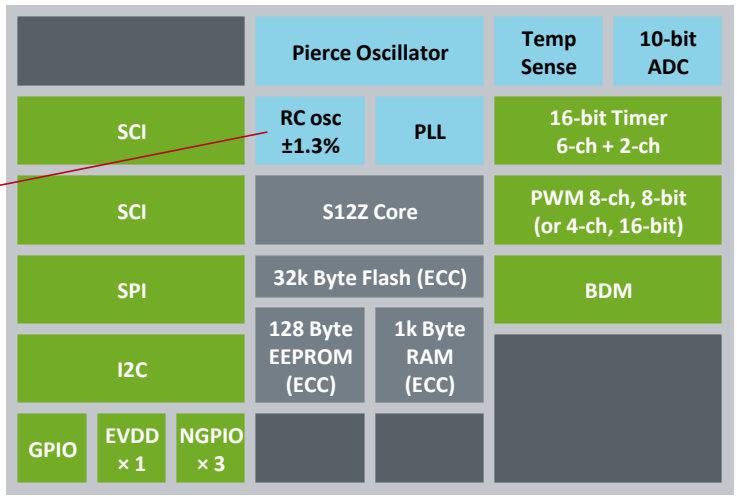
Safe RAM
- with ECC

Overview of S12ZVL Feature Set



Overview of S12ZVL Feature Set

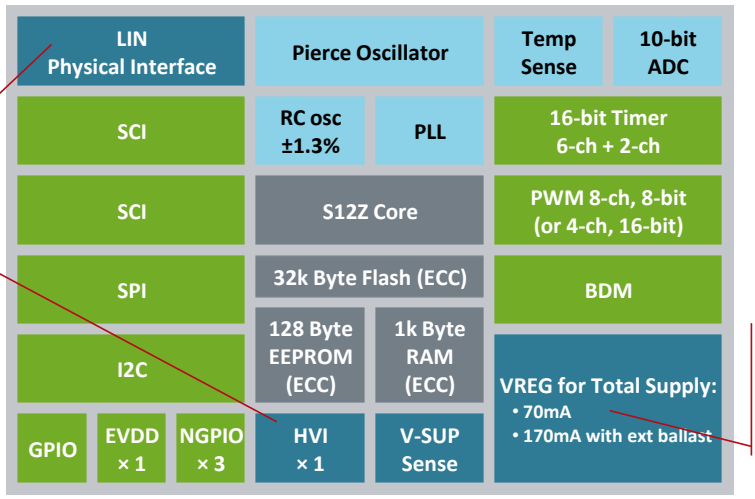
Internal RC oscillator
- ±1.3% over temp



Overview of S12ZVL Feature Set

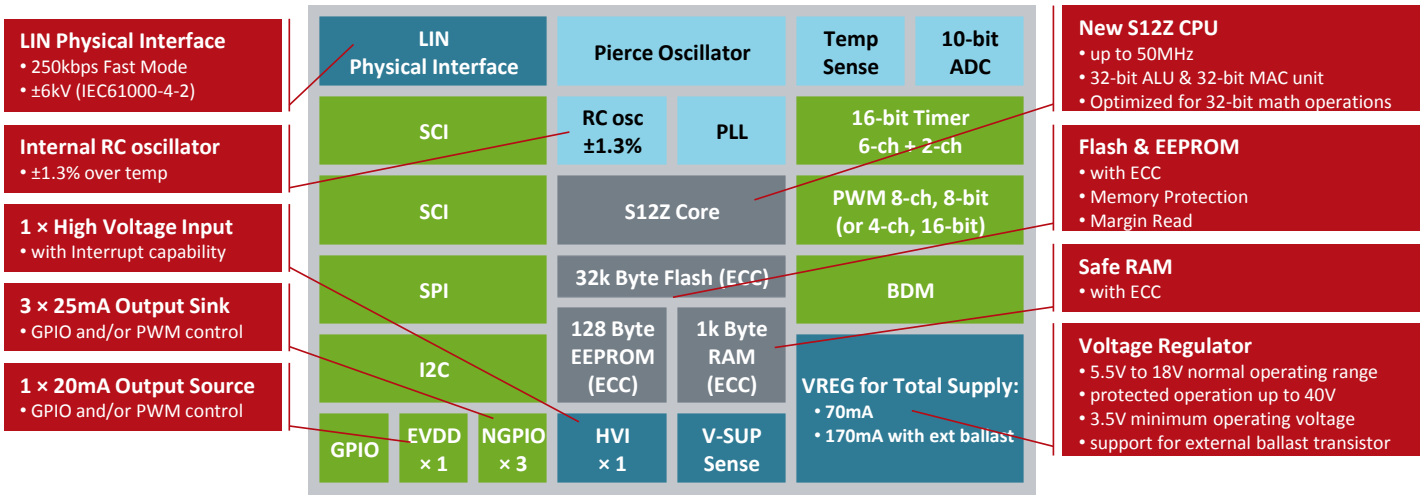
LIN Physical Interface
- 250kbps Fast Mode
- ±6kV (IEC61000-4-2)

1 × High Voltage Input
- with Interrupt capability



Voltage Regulator
- 5.5V to 18V normal operating range
- protected operation up to 40V
- 3.5V minimum operating voltage
- support for external ballast transistor

Overview of S12ZVL Feature Set



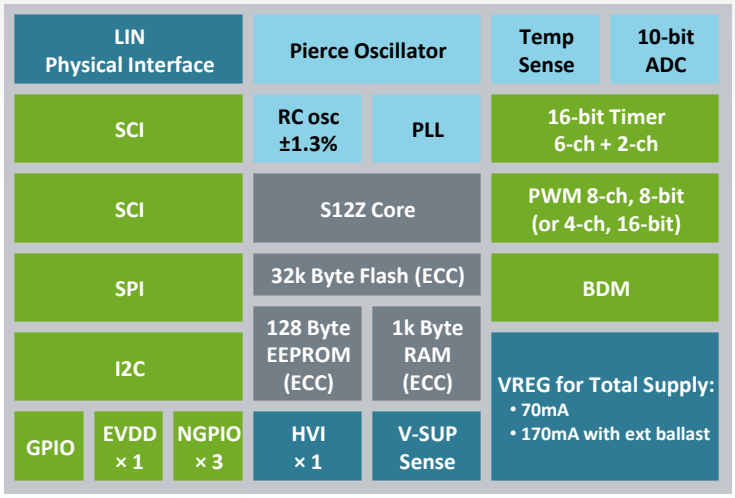
- **Functional Safety – ISO 26262 ASIL A Compliance:**
  - Developed in accordance with ISO 26262 as a Safety Element out of Context (SEooC).
  - Usable in safety relevant systems classified as ISO 26262 ASIL A.
  - MCU development process fulfills ASIL A requirements of ISO 26262.

S12ZVL Key Features

RGB ambient lighting

Sensor (airflow)

Switchpanels / Userinterfaces



Key Feature`	Benefits
S12Z core, 25 MHz Bus	Improved code-efficiency & core performance vs. S12
8 KB to 32 KB flash	Family-concept, no need for external Flash/EPROM/ROM
Up to 128 Bytes EEPROM	4B erasable page; Easier to use vs. data flash; no need for EE-emul.
all memories (Flash, RAM, EE) with ECC	Error Code Correction provides high reliability
Built-in automotive voltage regulator operating between 3.5 and 40 V	Operates directly from car-battery, no need for extra Voltage-regulator saving PCB-boardspace. handles automotive design issues, such as double battery, crank voltage and load dump conditions
Built-in LIN physical layer	No need for an external LIN physical layer device, saving space and design time. Meets automotive OEM specifications for LIN conformance and EMC requirements
NGPIO & EVDD	EVDD able to supply 5V/20 mA offchip; N-GPIO able to sink up to 3 x 25mA off Chip (useful for RGB-LED-drive)
Protected 12V input (HVI)	Allows automotive battery voltage-level inputs (with ADC-capability & ESD-protection)
on Chip RC oscillator trimmed to 1,3% tolerance	Due to accurate on chip clock generation LIN-communication can be done without external Crystal or Resonator and without the need of SW-intense synchronization

Package Options:

- 48 LQFP, 32 LQFP
- 32QFN (5 x 5 mm)

S12ZVC Key Features

Seatbelt pretention

Sensor (Powertrain)

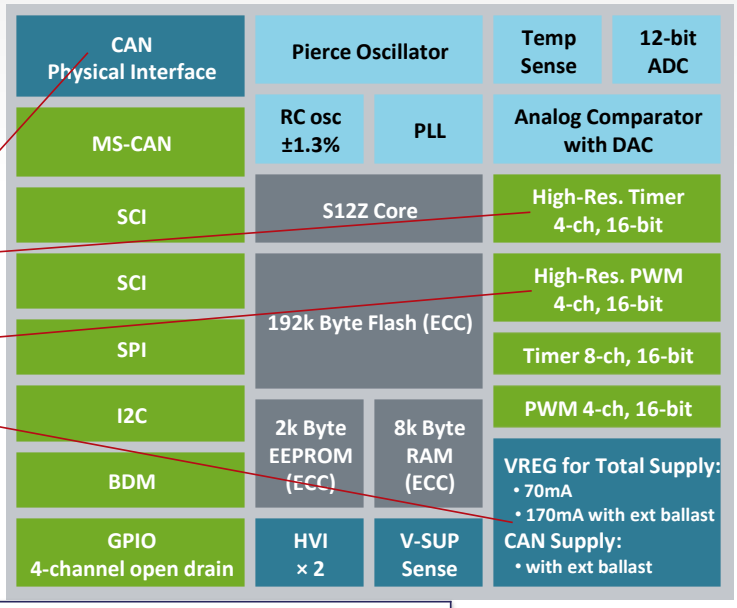
Switchpanels / Userinterfaces

CAN Physical Interface
- High Speed – up to 1Mbps
- ISO 11898-2 & ISO 11898-5

High-Resolution Timer
- 20ns with 25MHz bus

High-Resolution PWM
- 20ns with 25MHz bus

Seperate CAN Supply
- with external ballast transistor

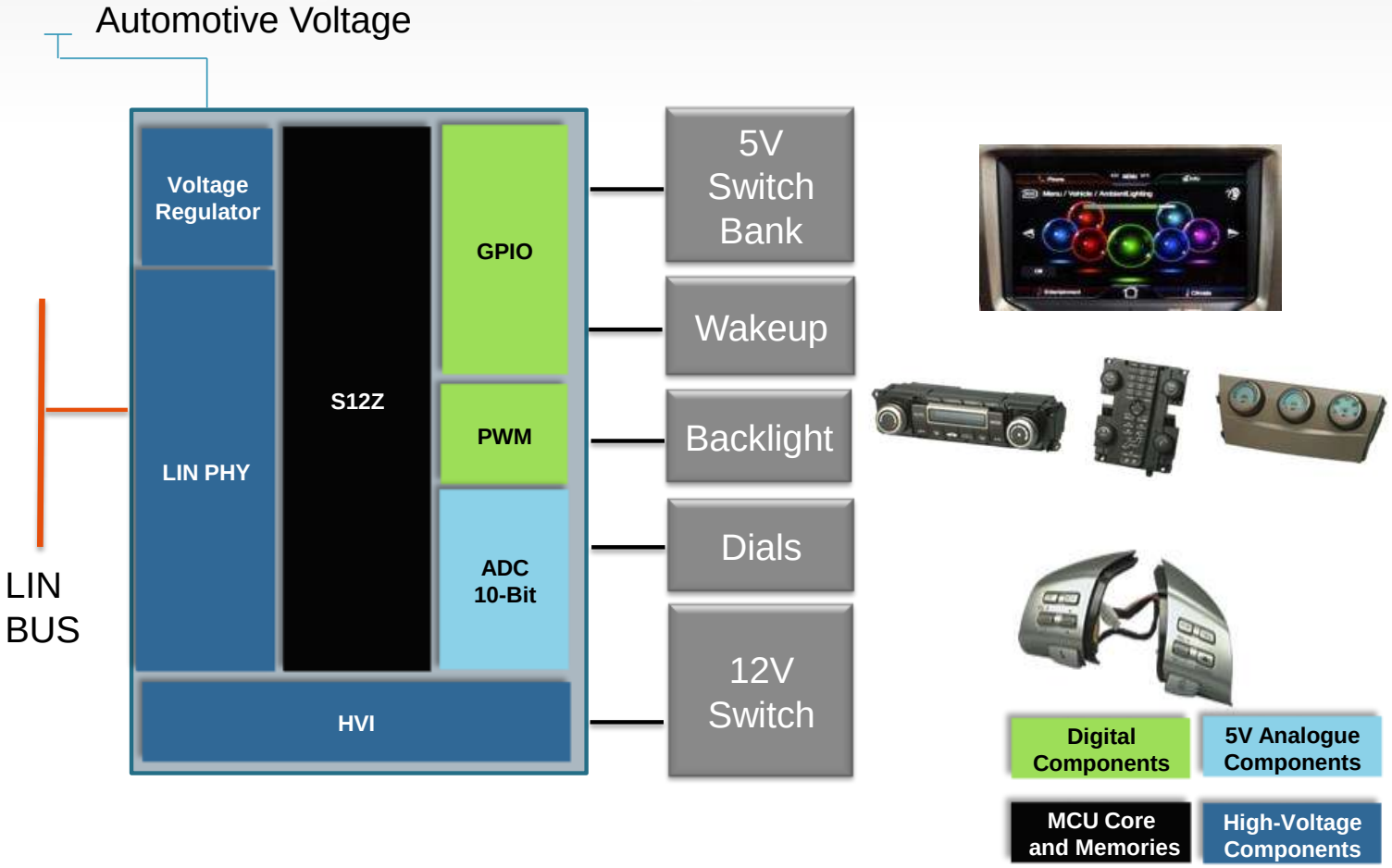


Key Feature	Benefits
S12Z core, 32 MHz Bus	Improved code-efficiency & core performance versus S12
64 KB to 192 KB flash	Family-concept, no need for external Flash/EPROM/ROM
Up to 2k Bytes EEPROM	4B erasable page; Easier to use vs. data flash; no need for EE-emul.
all memories (Flash, RAM, EE) with ECC	Error Code Correction provides high reliability
Built-in automotive voltage regulator operating between 3.5 and 40 V	Operates directly from car battery without the need for extra voltage regulator, saving PCB board space. Handles automotive design issues, such as double battery, crank voltage and load dump conditions
Built-in CAN physical layer	No need for an external CAN physical layer device, saving space as well as time & cost for design & testing. Meets automotive OEM requirements for CAN conformance and EMC.
Analog Comparator with DAC	Allows for fast reaction of ext. signals vs. preprogrammed threshold
Protected 12V input (HVI)	Allows automotive battery voltage-level inputs (with ADC-capability & ESD-protection)
12-Bit ADC; 16ns-Timer/PWM	High resolution mixed signal peripherals for many sensor-applications (e.g. ultrasonic)

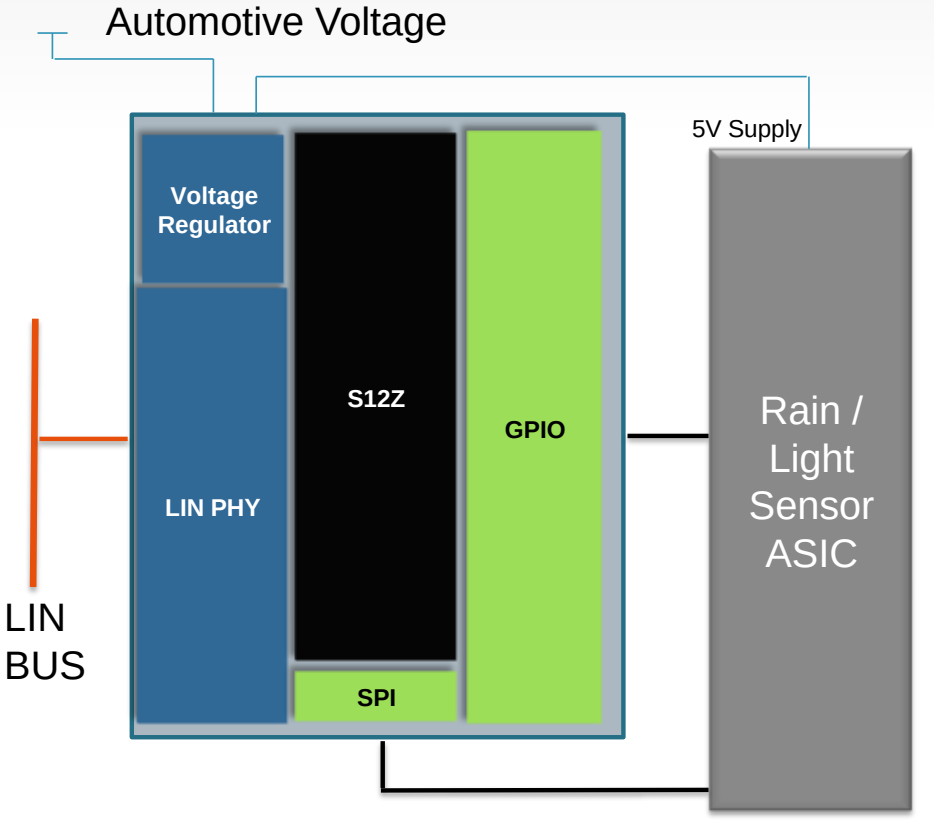
Package Options:

- 64 LQFP
- 48 LQFP

S12ZVL Application Example: Switch Panel



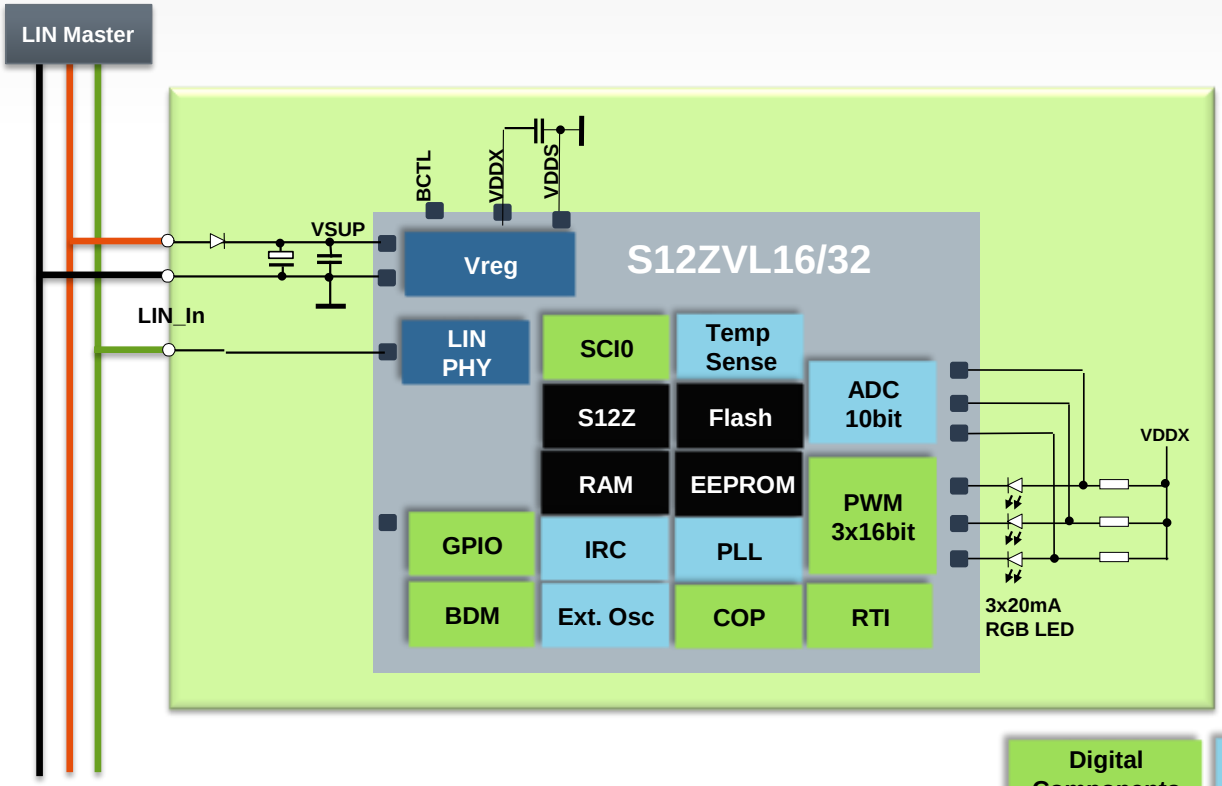
S12ZVL Application Example: Intelligent Sensor



http://www.bmw.com/com/en/insights/technology/technology_guide/articles/rain_sensor.html

Digital Components | 5V Analogue Components | MCU Core and Memories | High-Voltage Components

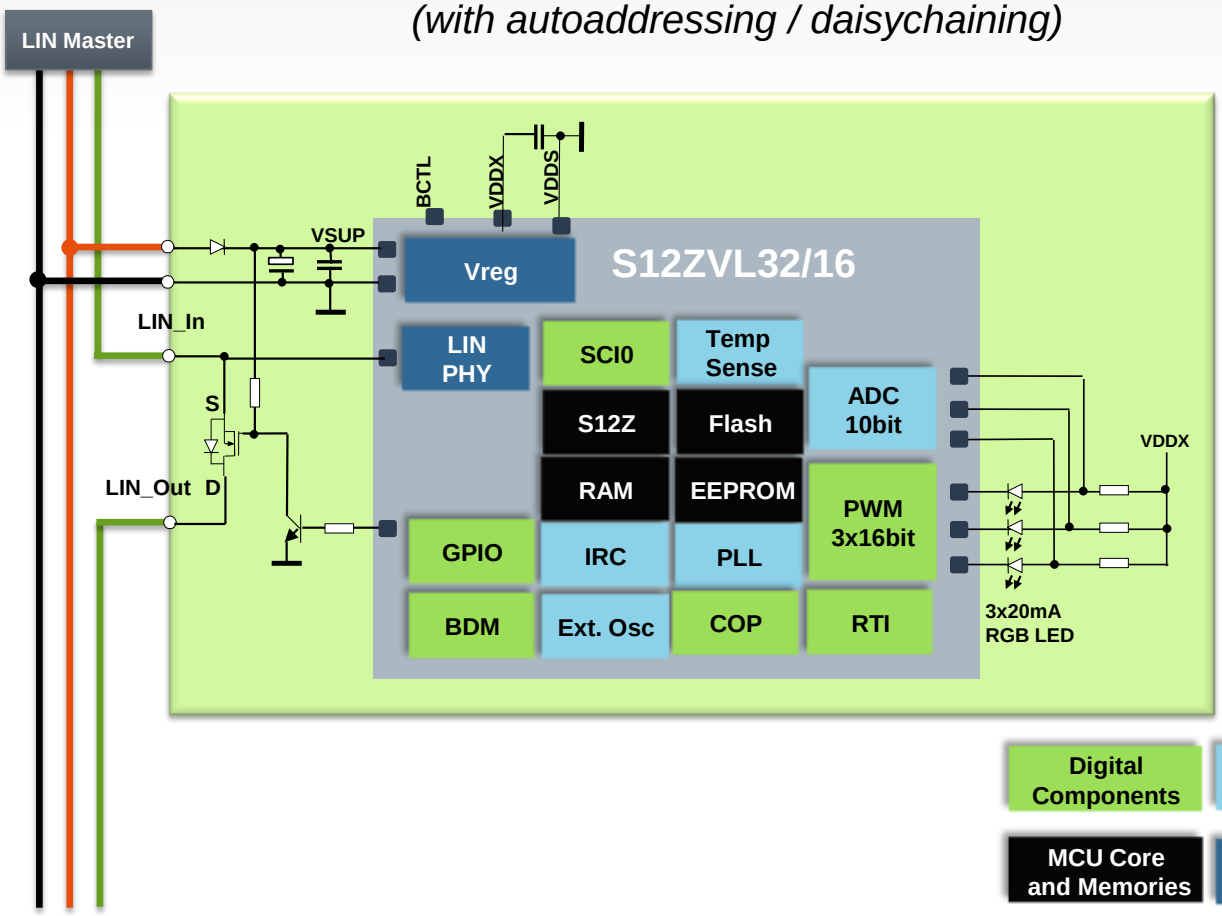
S12ZVL Application Example: LIN RGB LED



Digital Components | 5V Analogue Components
MCU Core and Memories | High-Voltage Components

S12ZVL Application Example: LIN RGB LED

(with autoaddressing / daisychaining)



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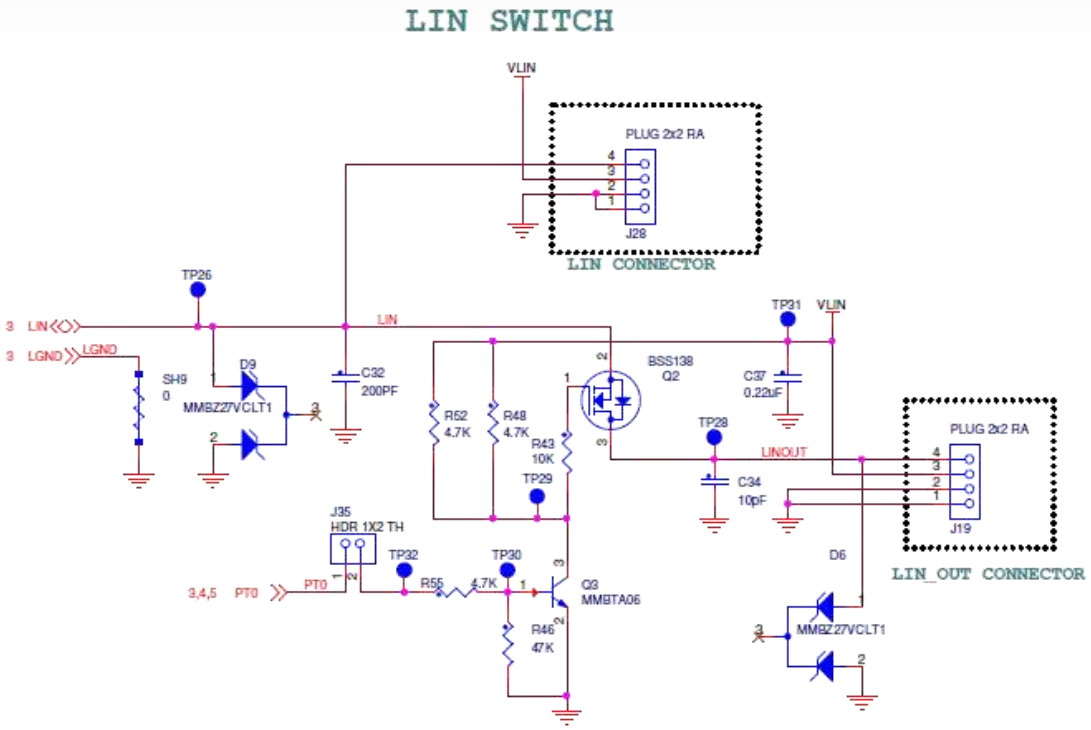
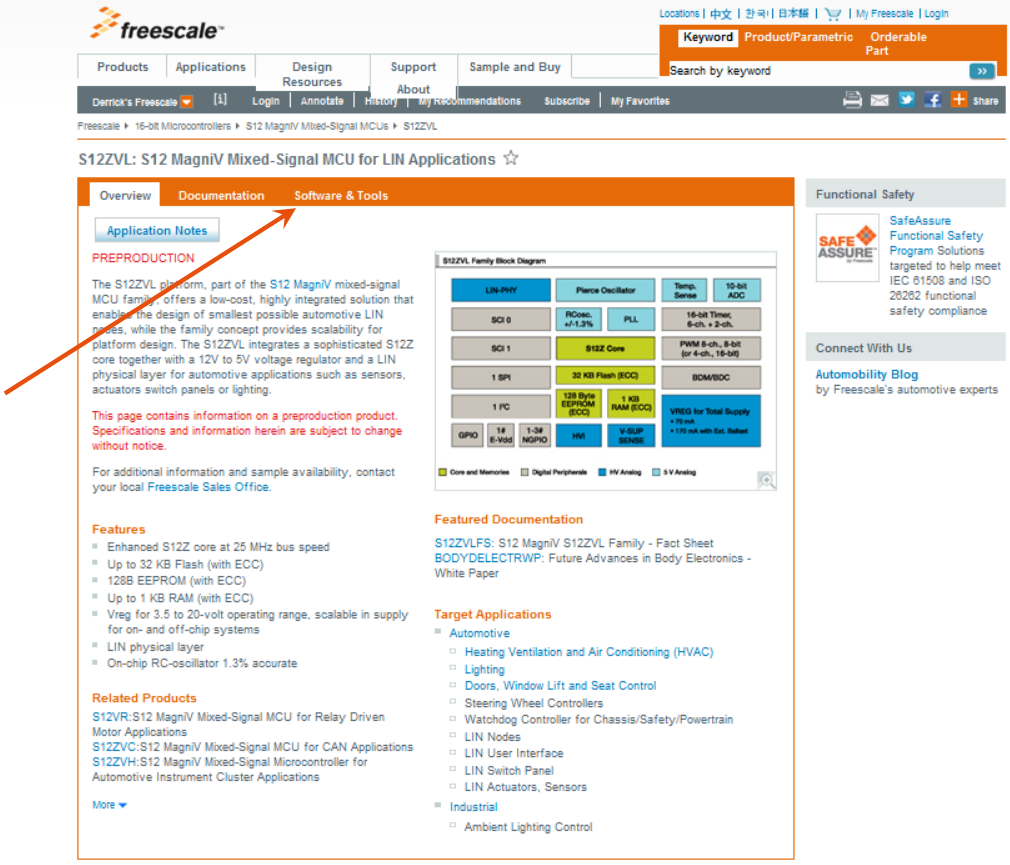
MCU Core and Memories | High-Voltage Components

TRK-S12ZVL: LIN Daisychain

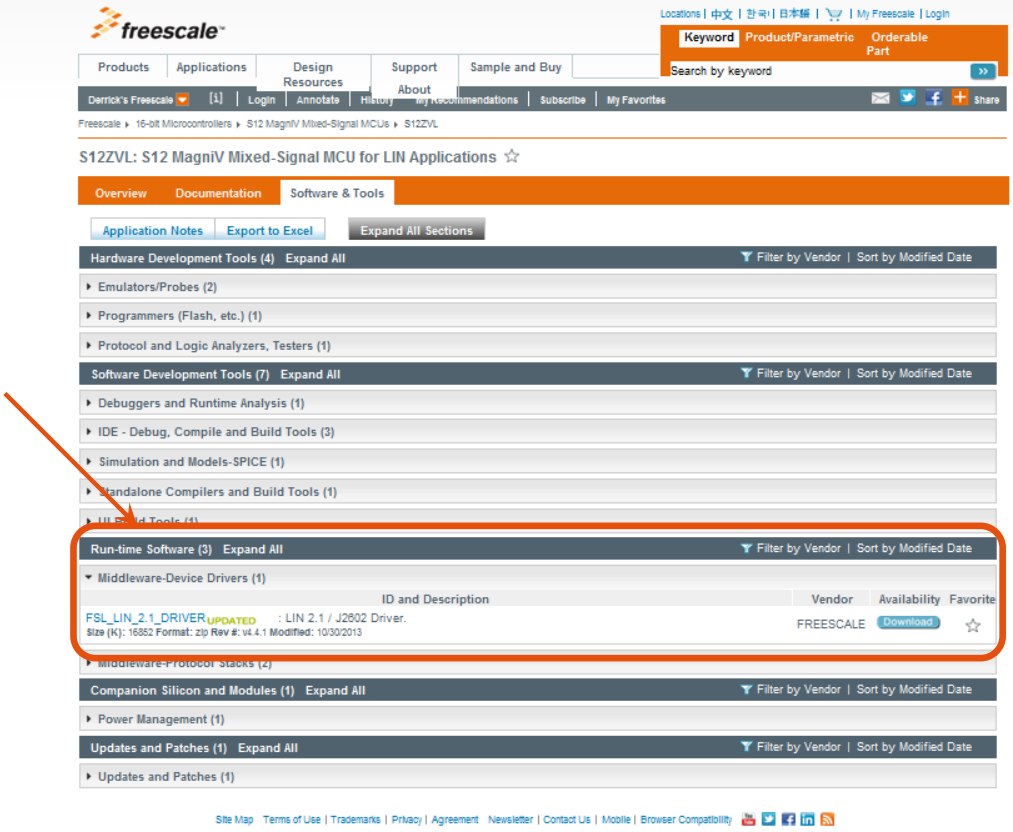


S12VL



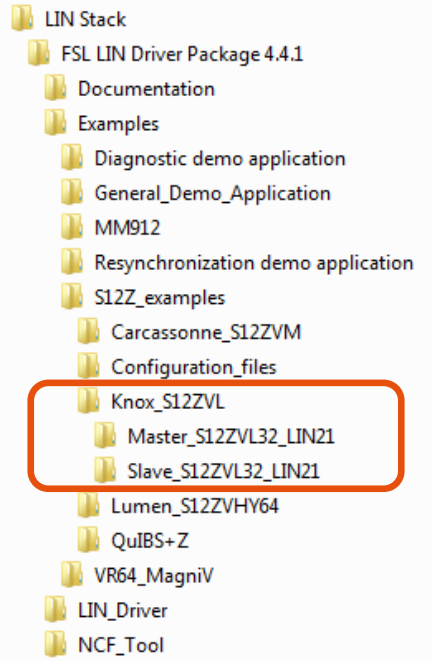
freescale.com/MagniV

S12VL



freescale.com/MagniV

Freescale LIN 2.1 Driver (version 4.4.1)



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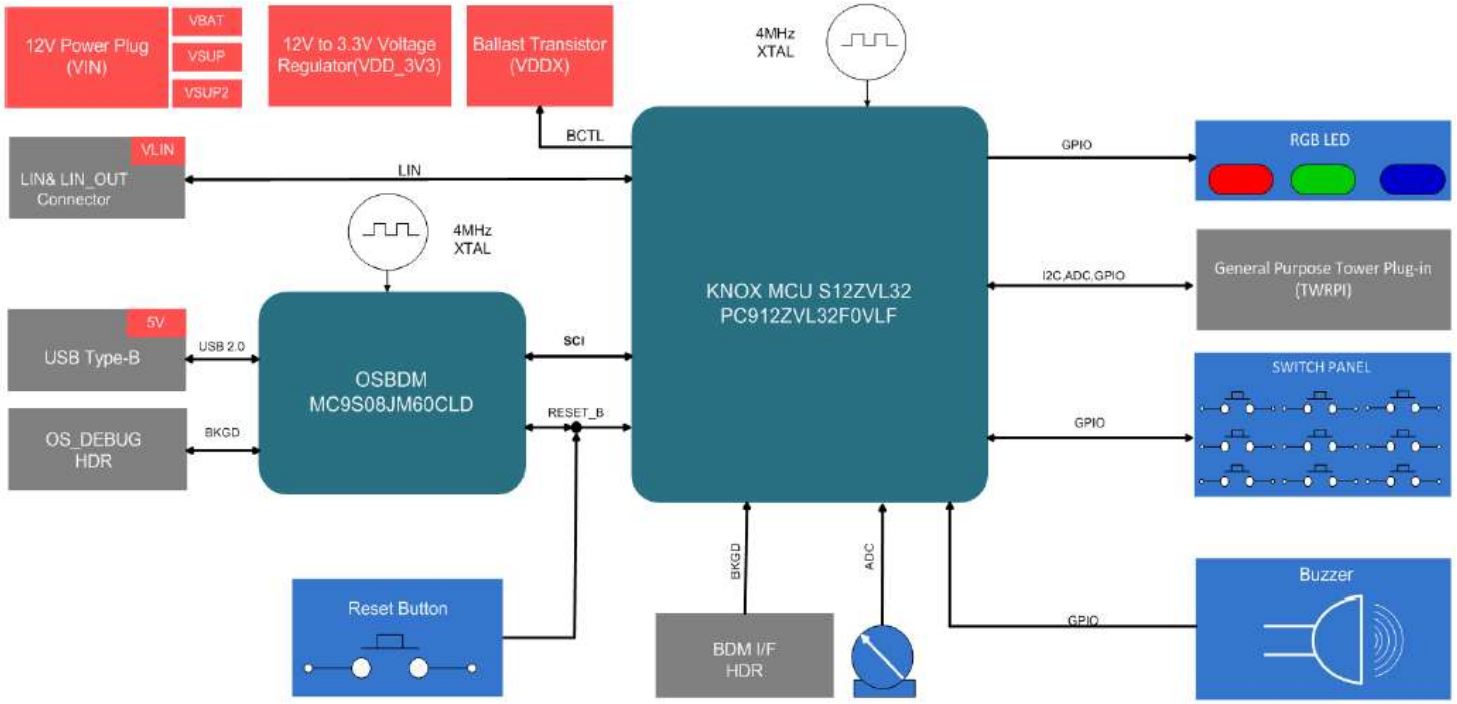
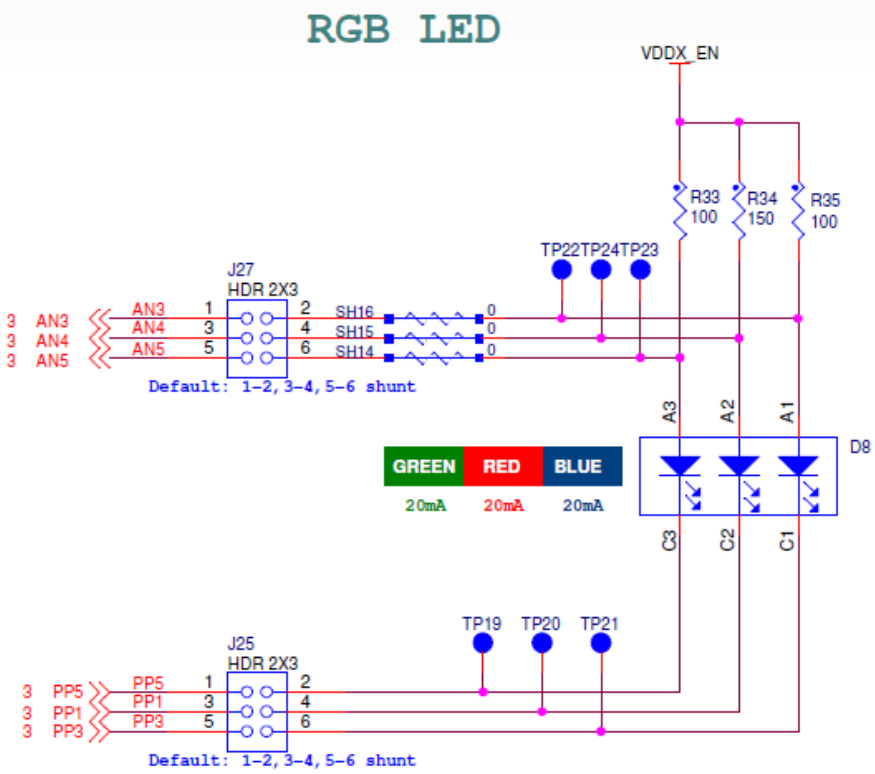
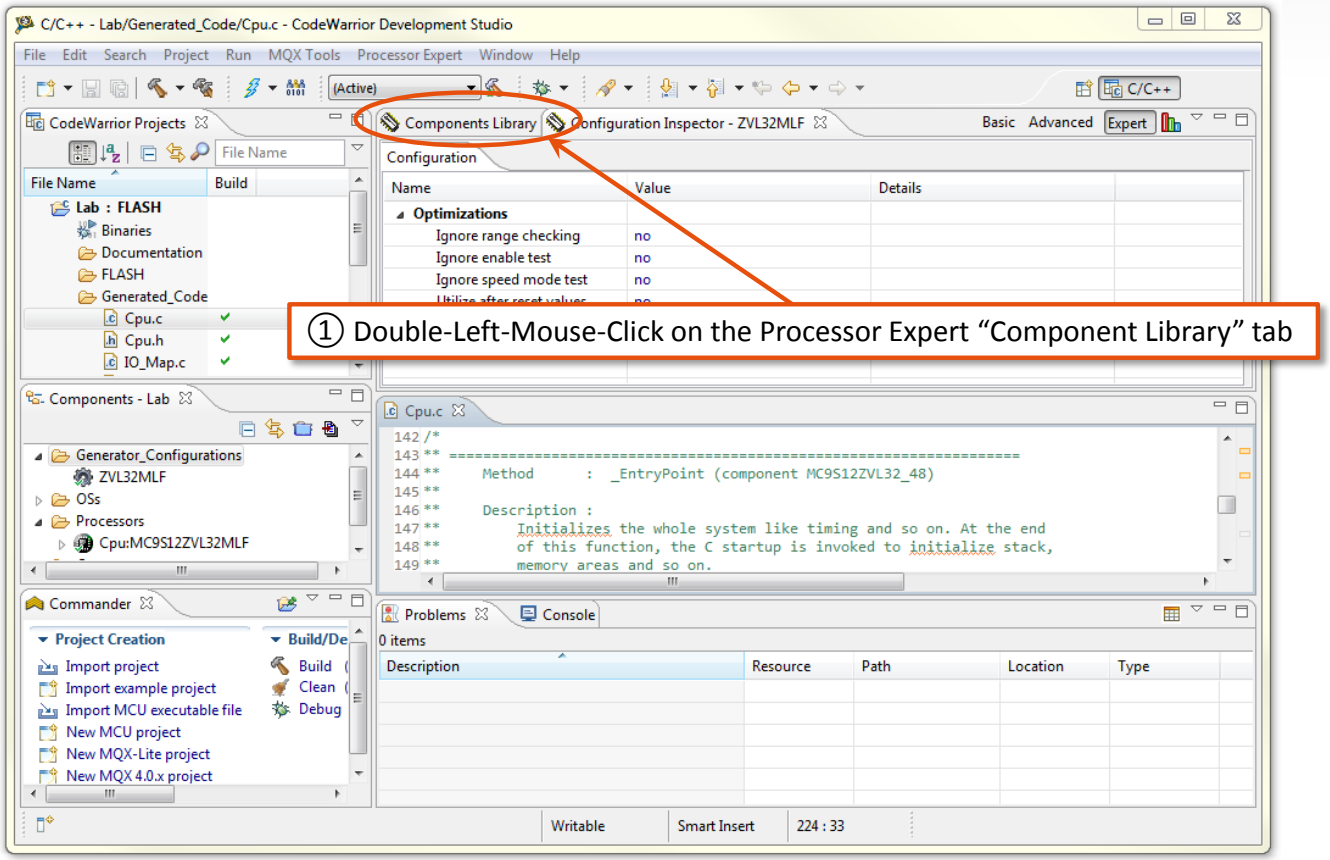
TRK-S12ZVL Block Diagram

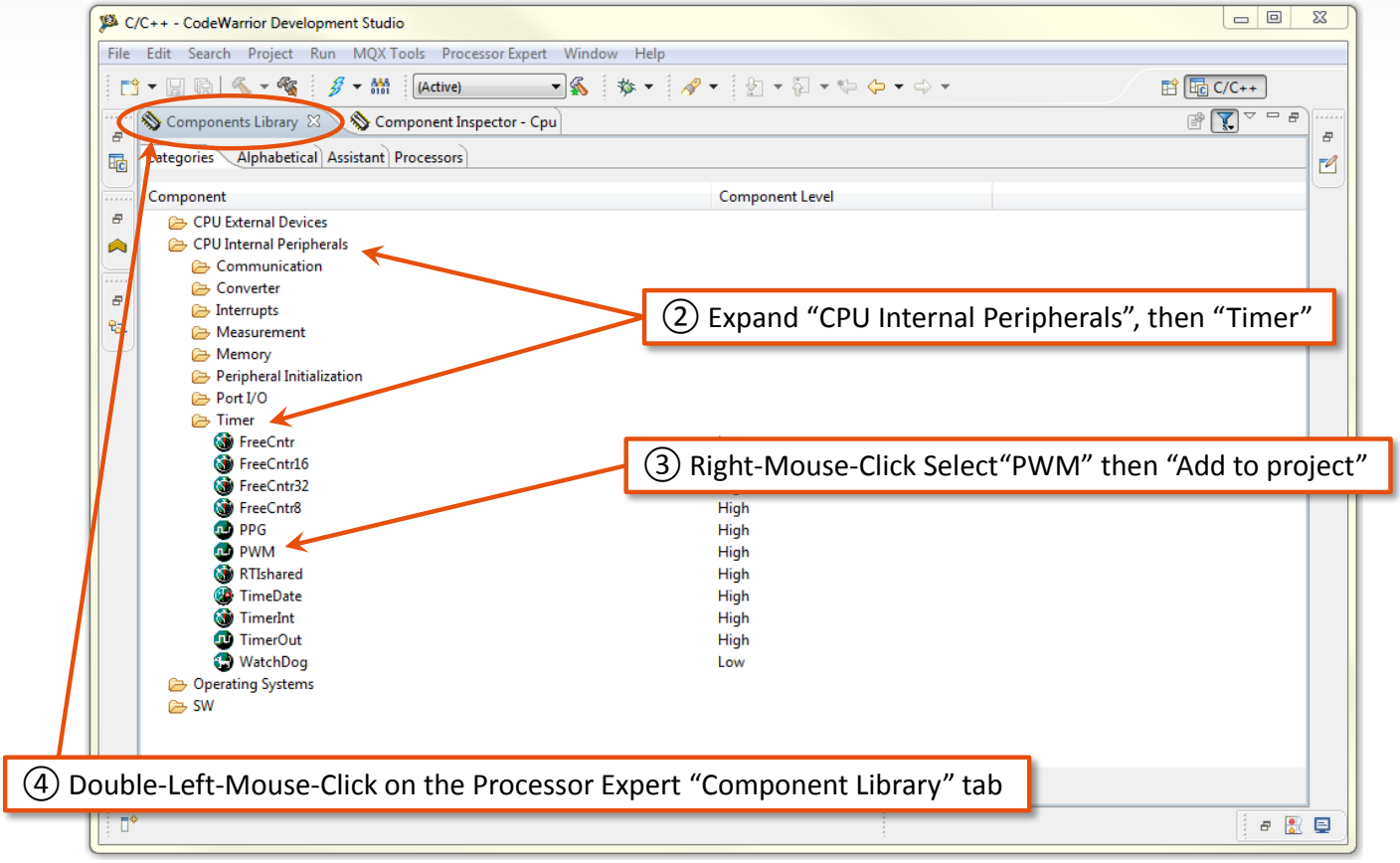




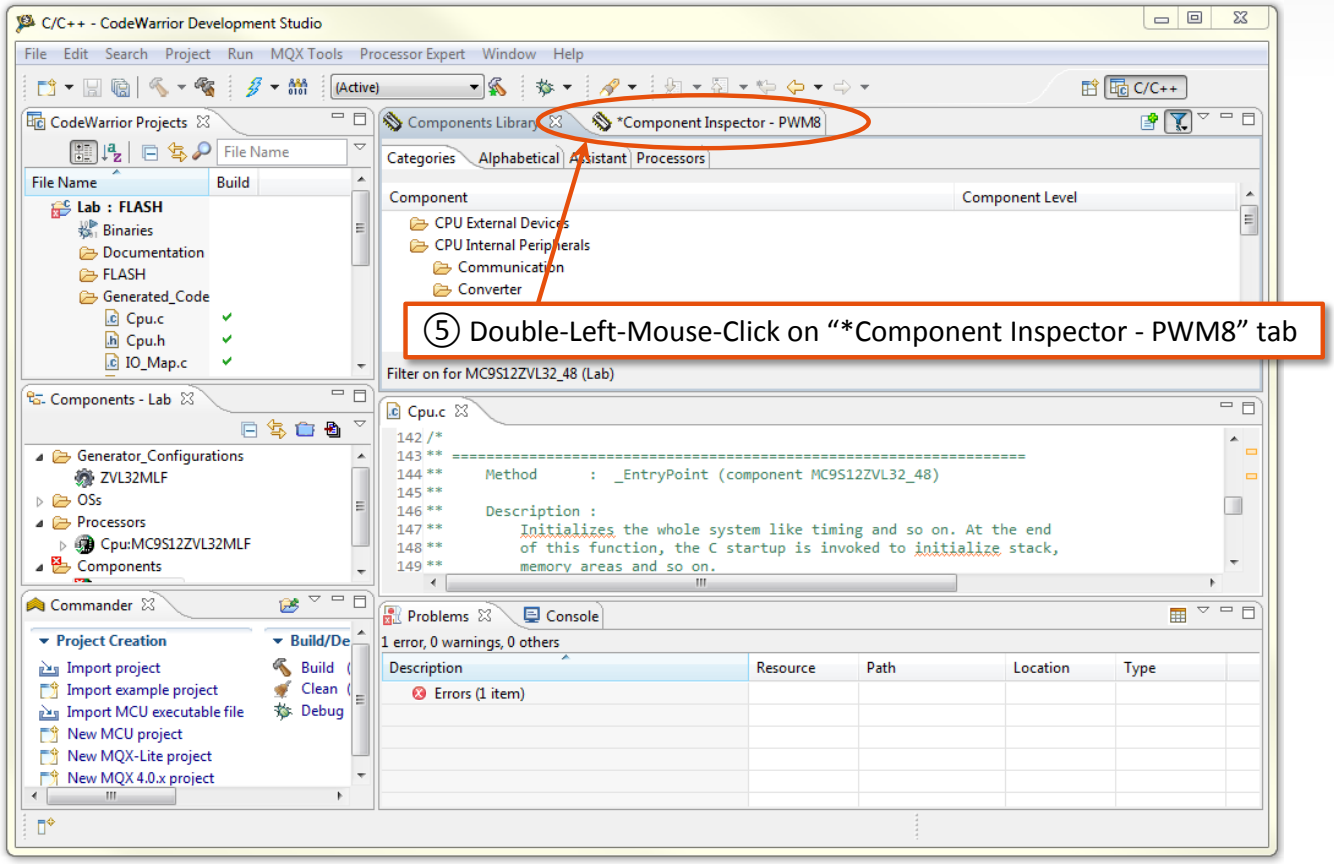
Lab Part 2: PWM LED Control



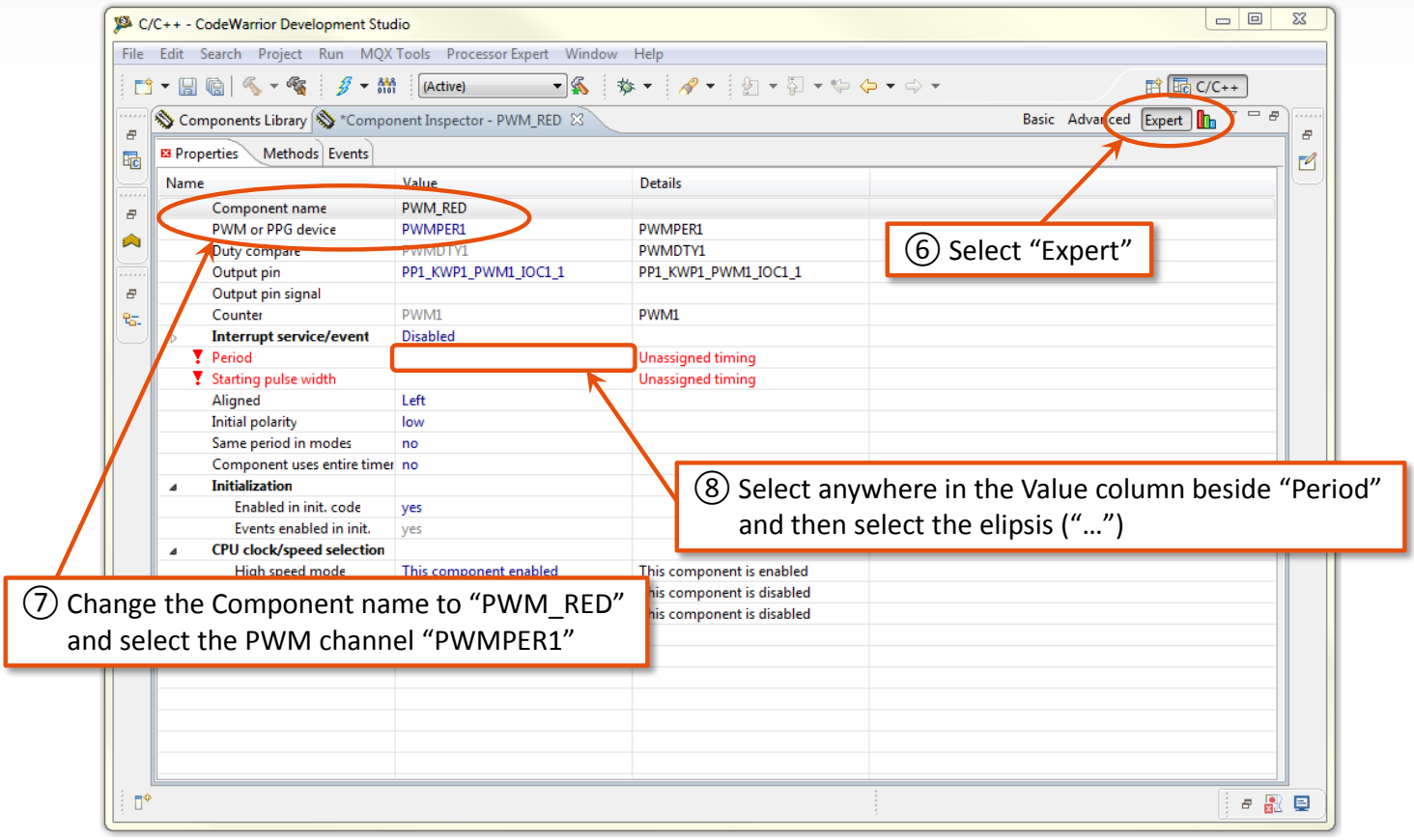
Add a PWM Component to the Project



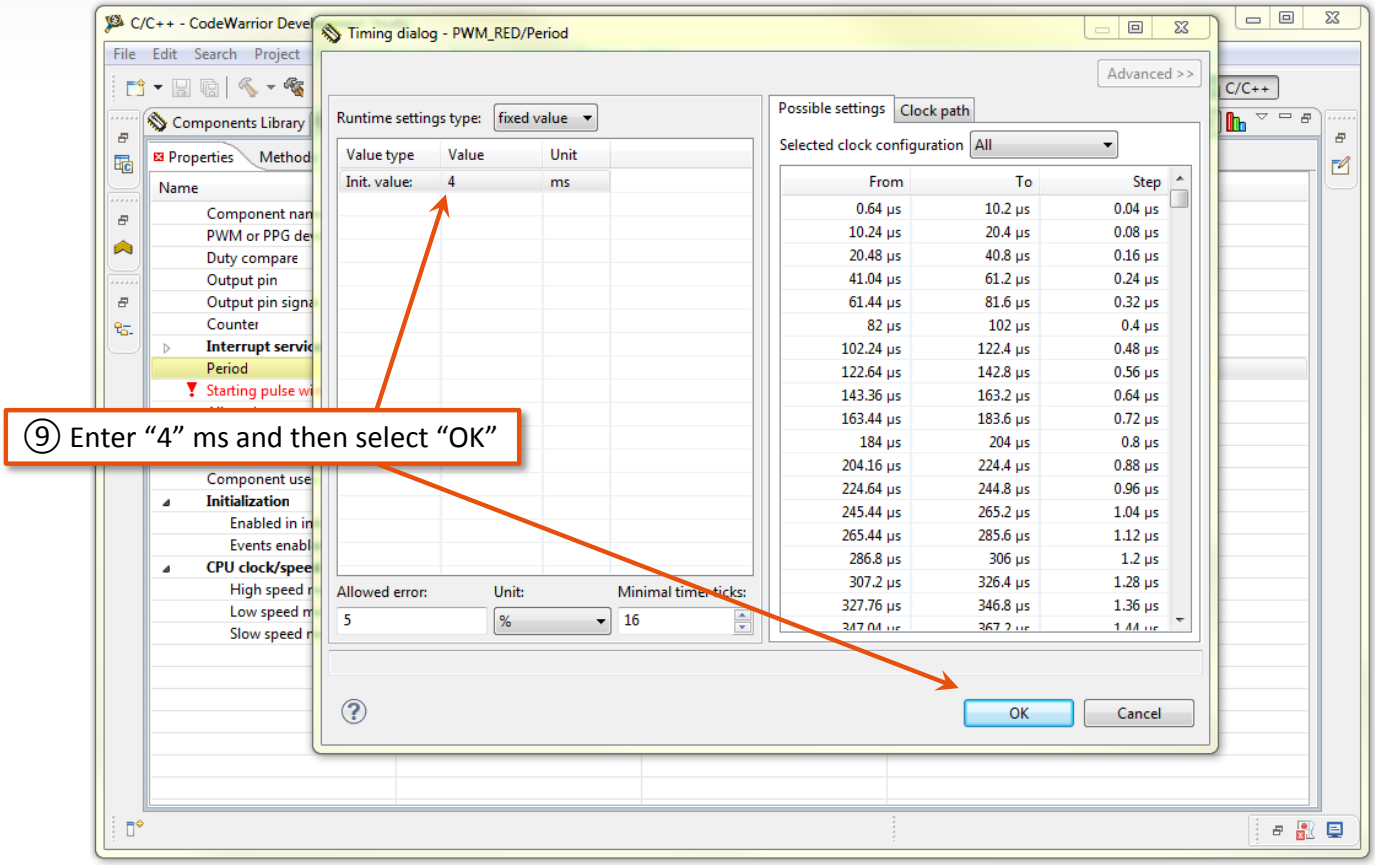
Change PWM Component Properties



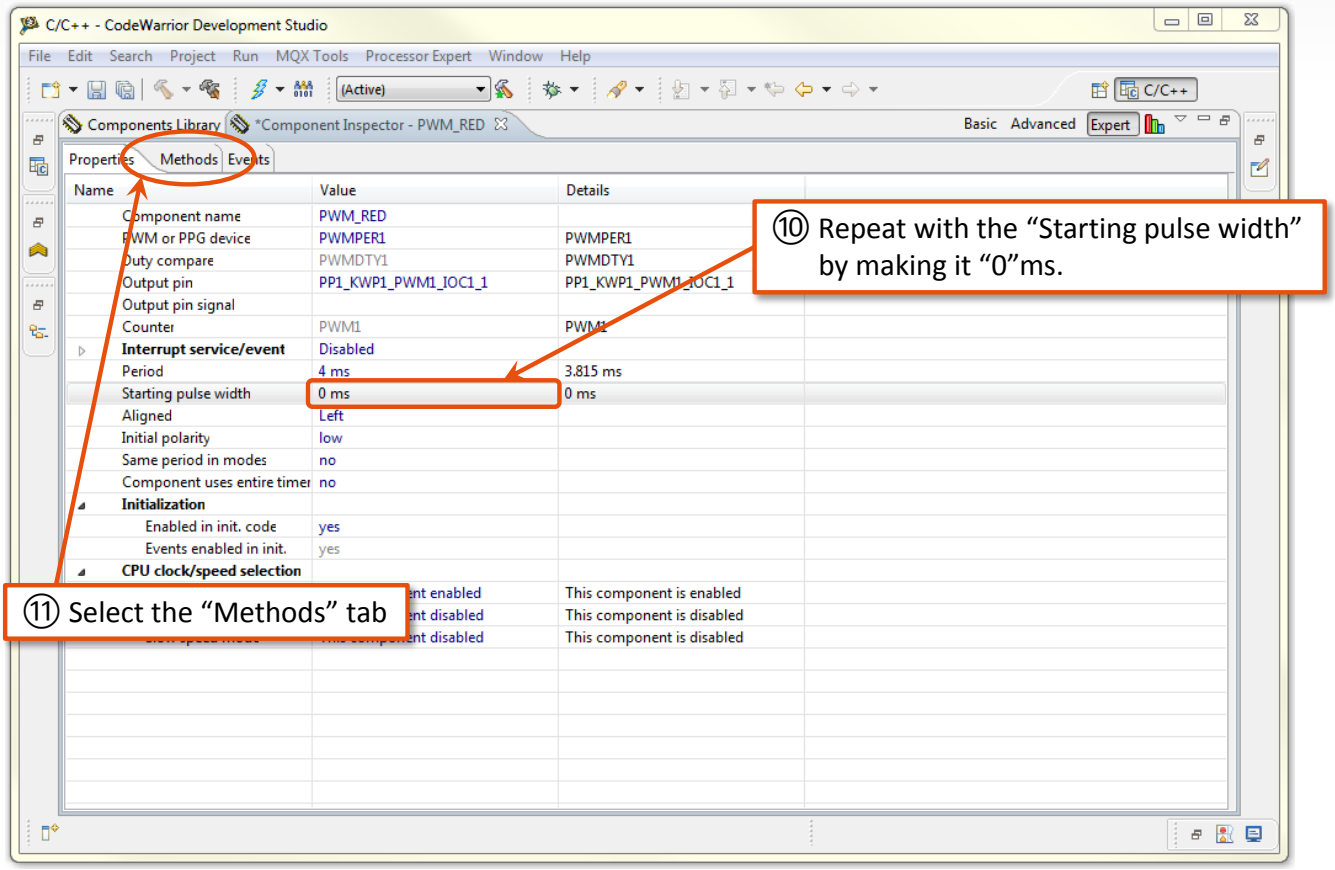
Change PWM Component Properties



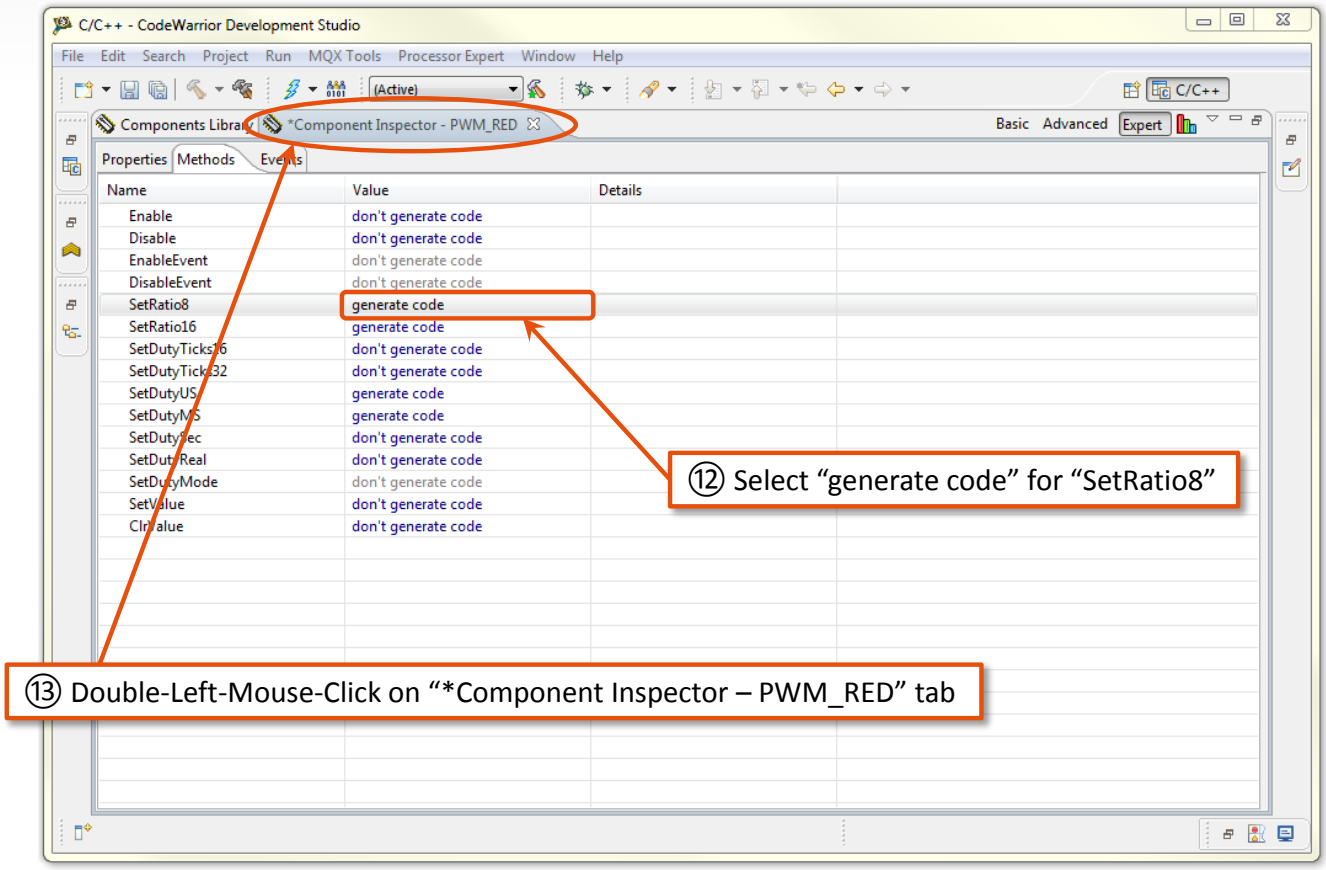
Change PWM Component Properties



Change PWM Component Properties



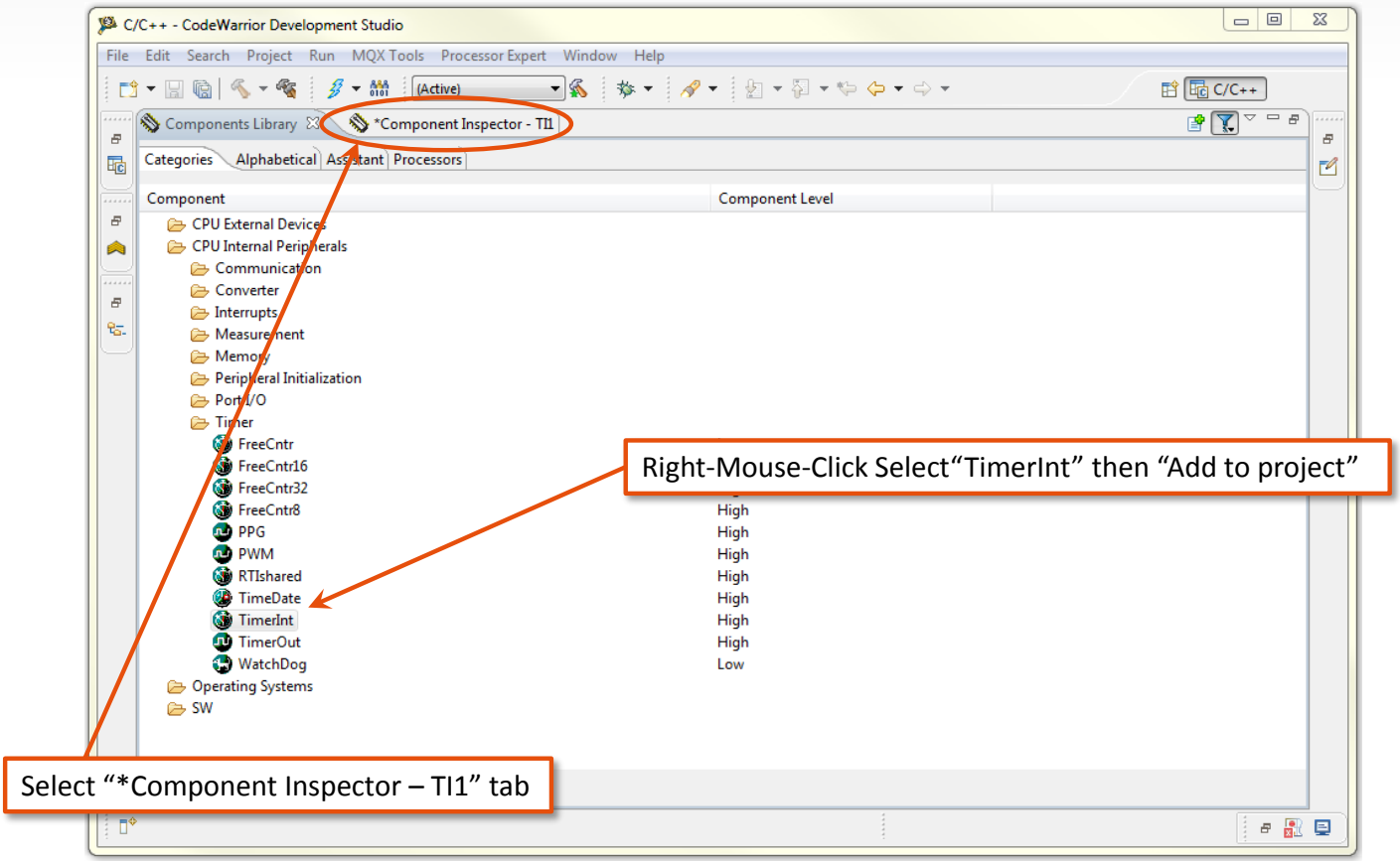
Change PWM Component Properties



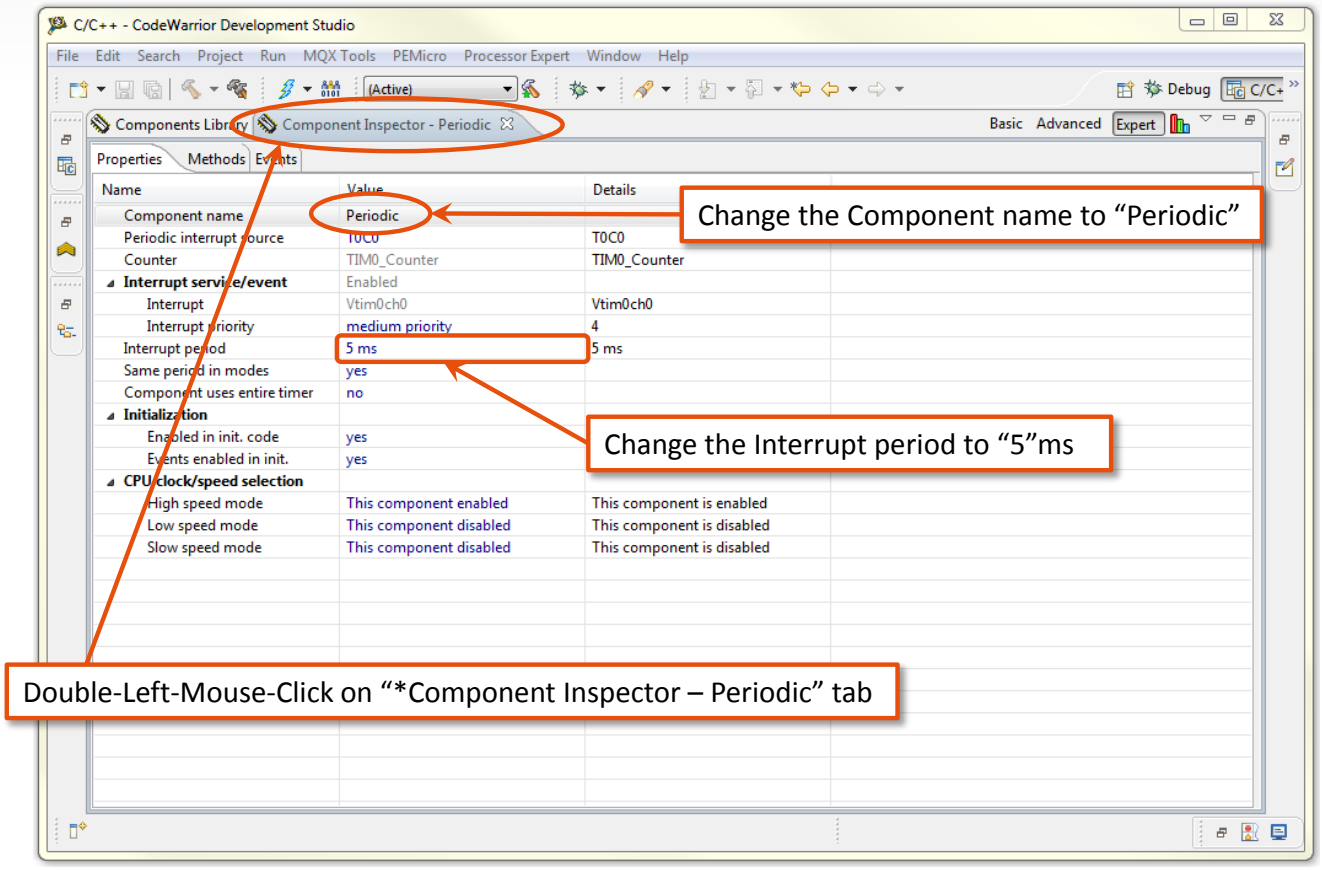
Create a PWM Component for Each LED Colour

- Repeat the previous steps ① through ⑬ two more times creating separate identical PWM channels for:
  - "PWM_GREEN" on "PWMPER5"
    - on Output pin "PP5_XIRQ_KWP5_PWM5"
  - "PWM_BLUE" on "PWMPER3"
    - on Output pin "PP3_IRQ_KWP3_PWM3"

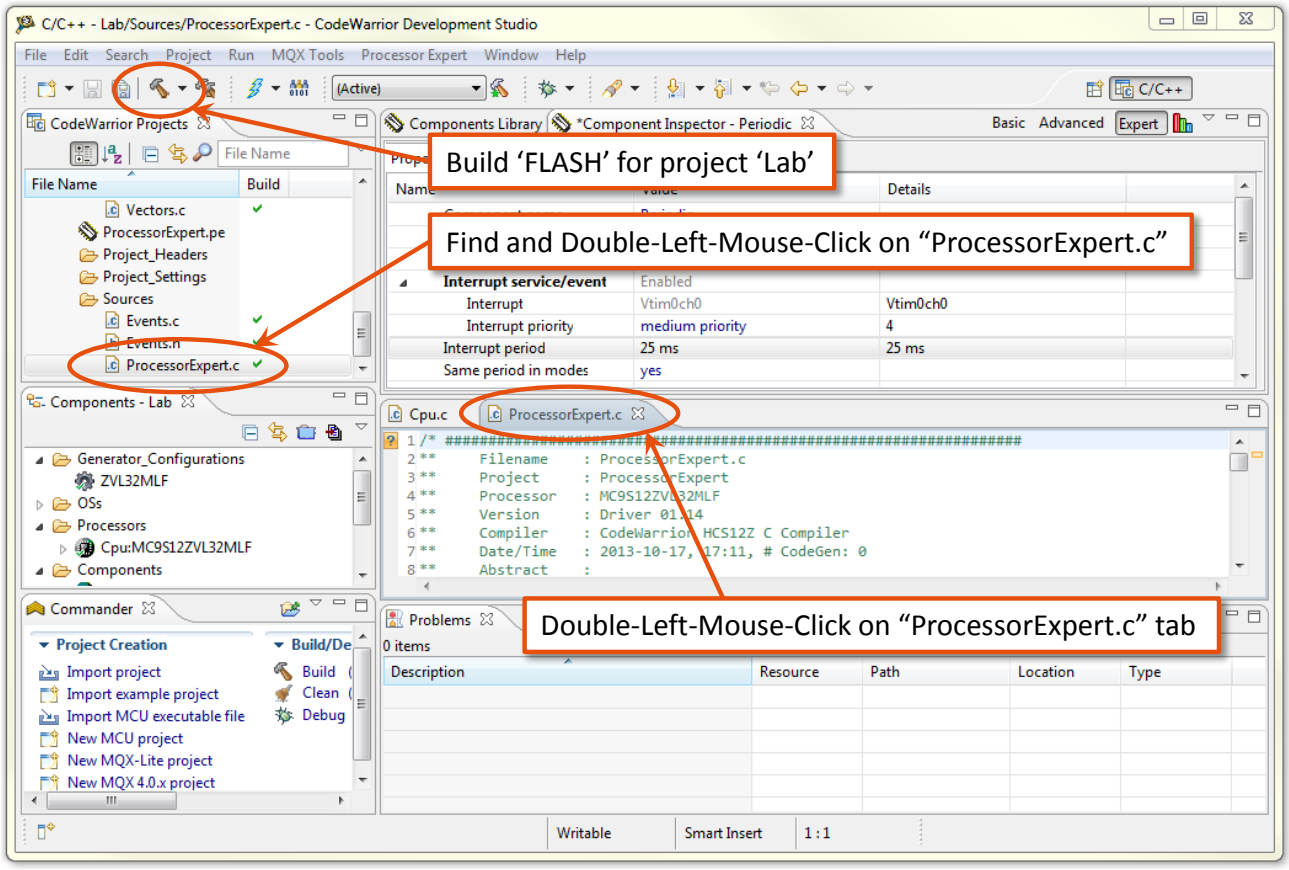
Add a Periodic Timer Component to the Project



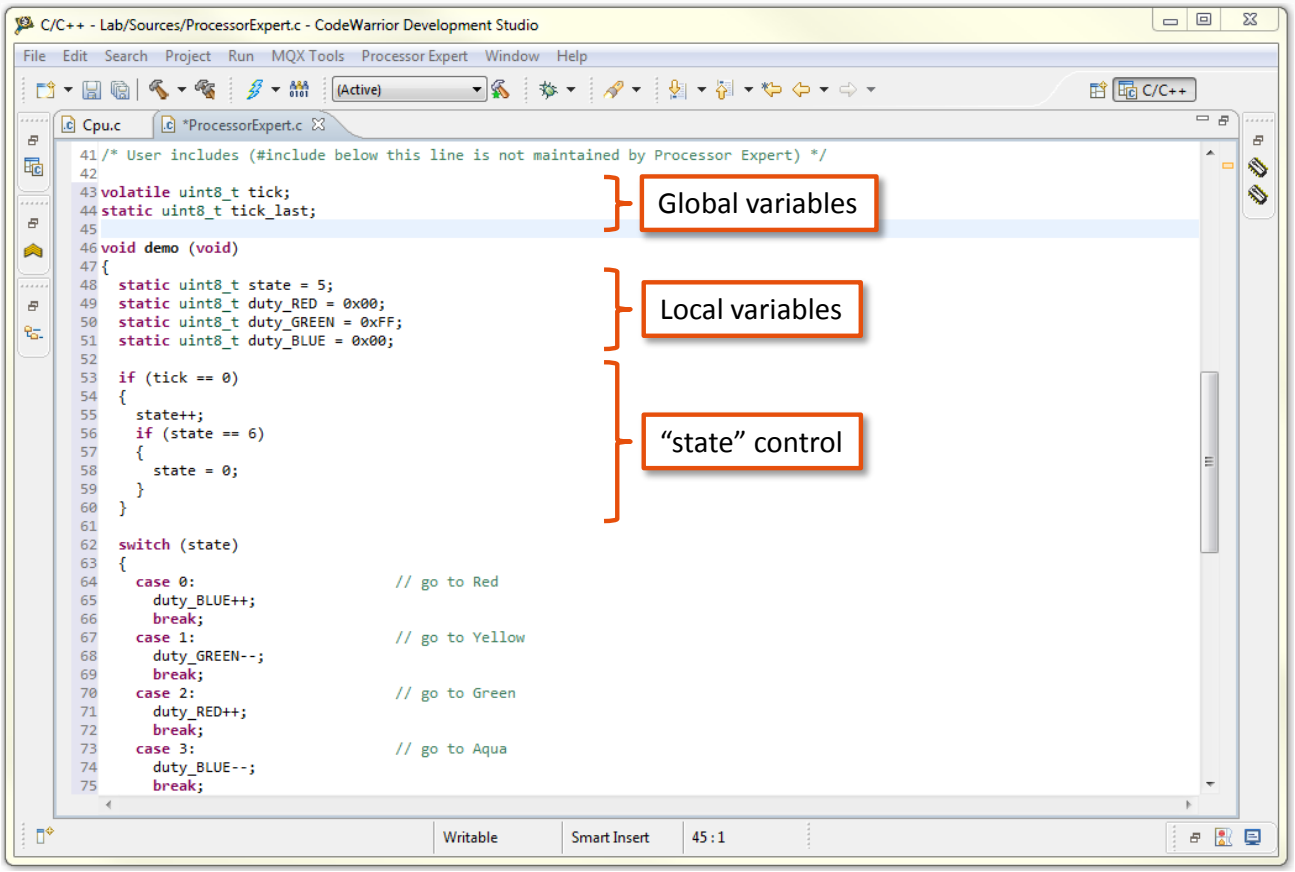
Change Periodic Timer Component Properties



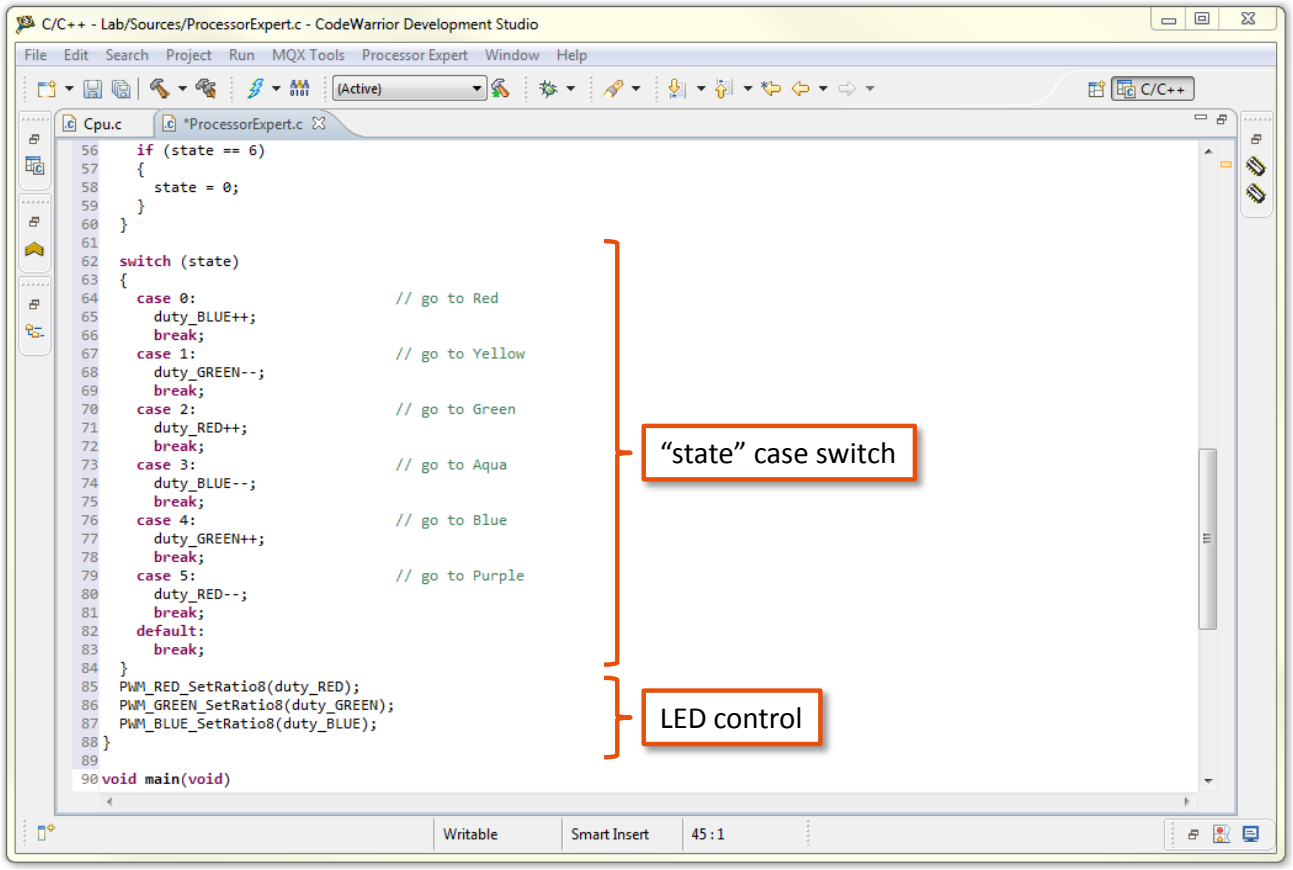
Build the Processor Expert Components



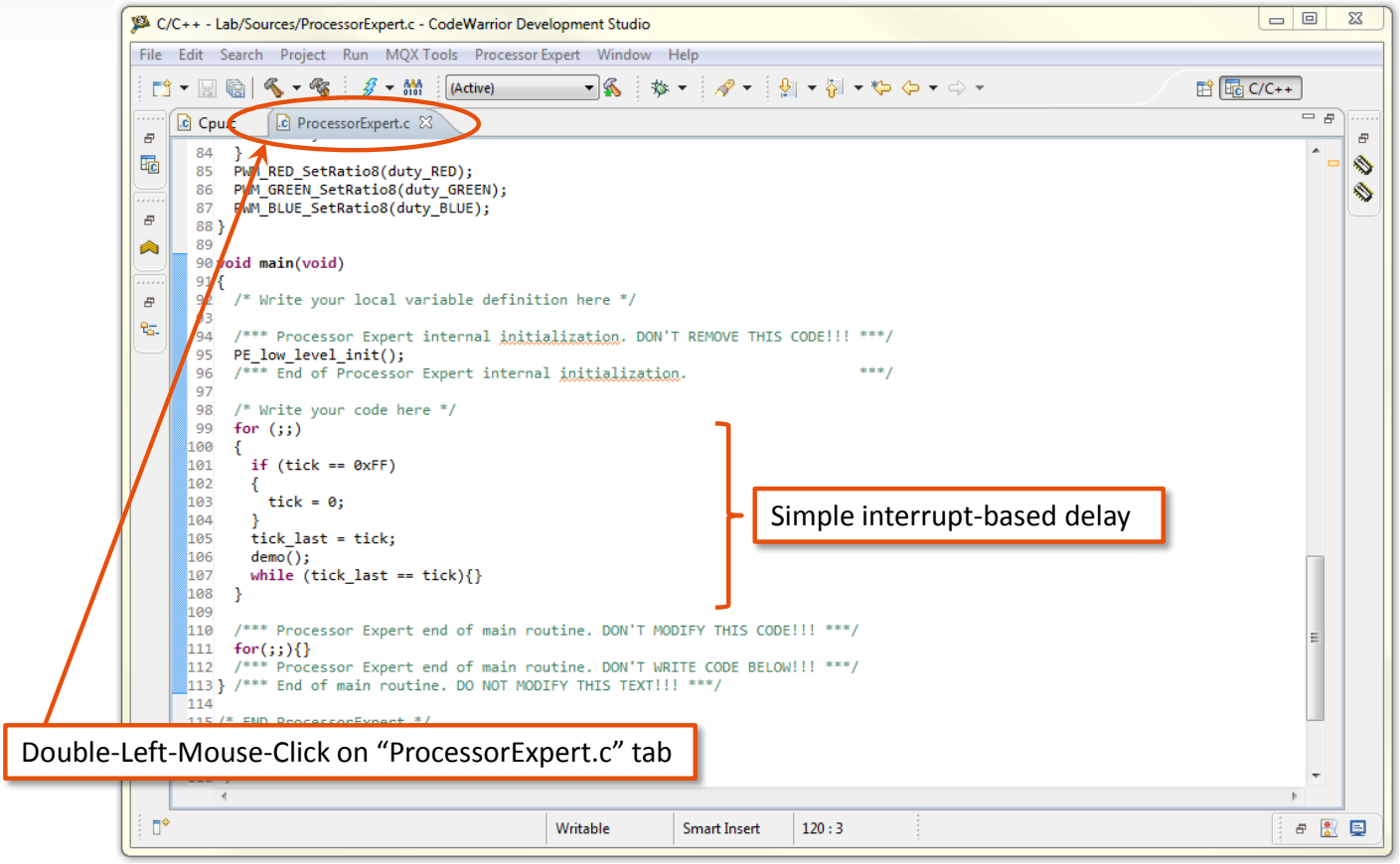
Add Code to ProcessorExpert.c



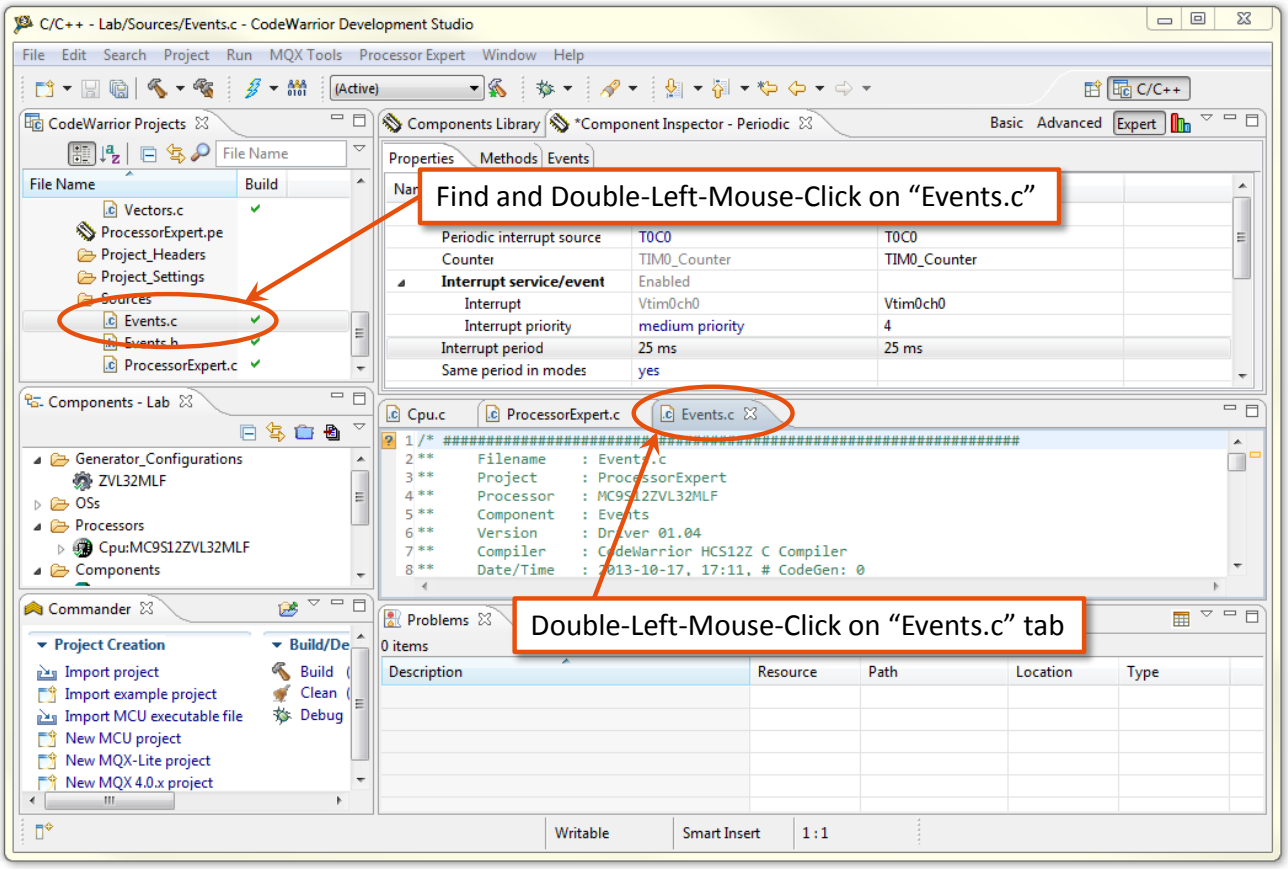
Add Code to ProcessorExpert.c



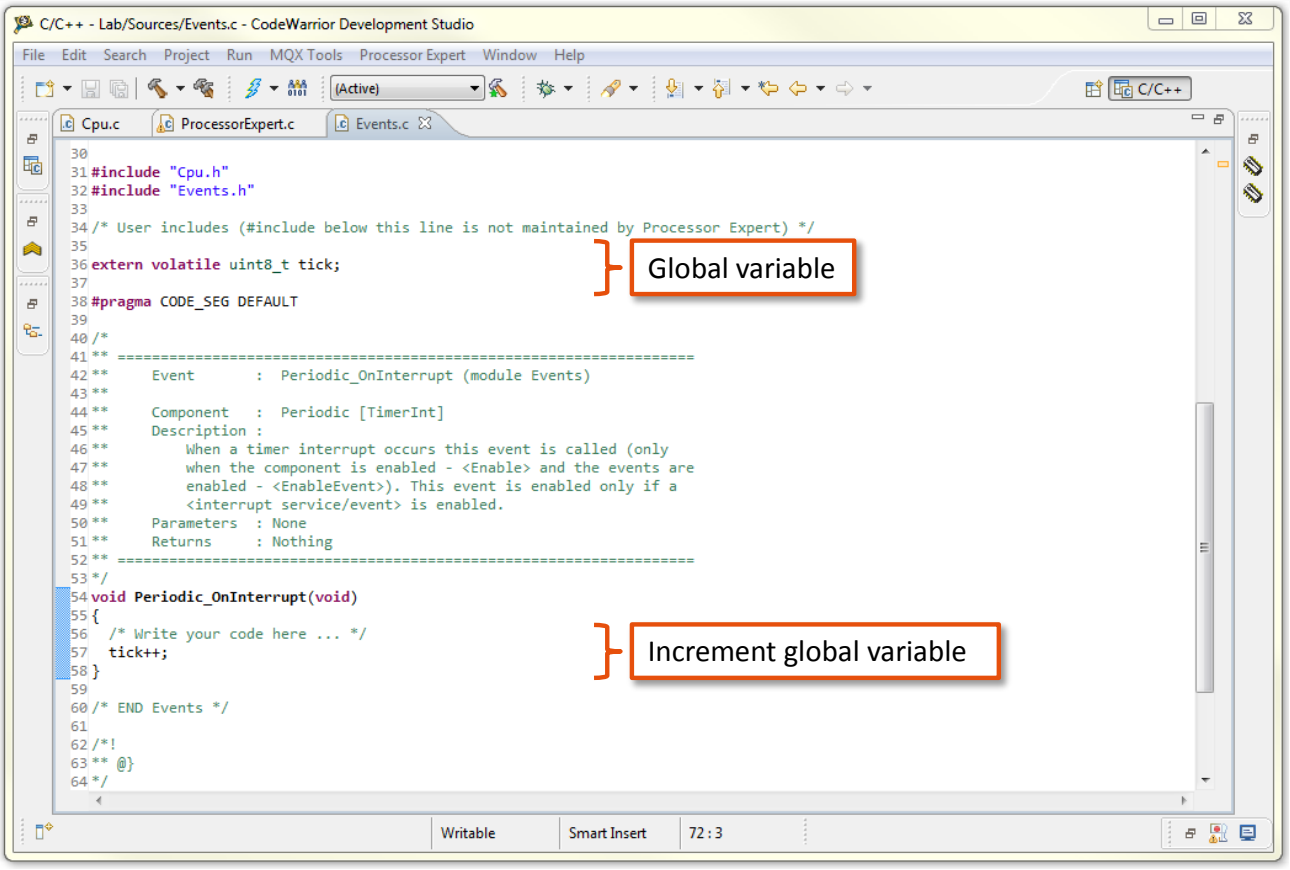
Add Code to ProcessorExpert.c



Add Code to Events.c

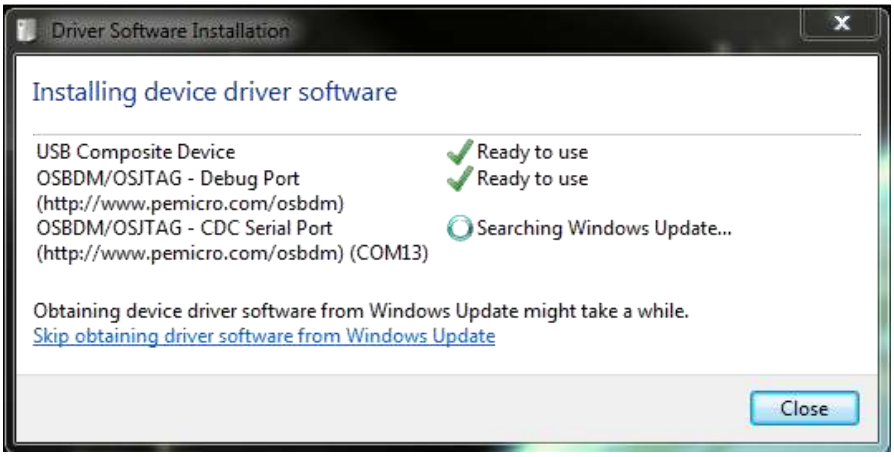


Add Code to Events.c



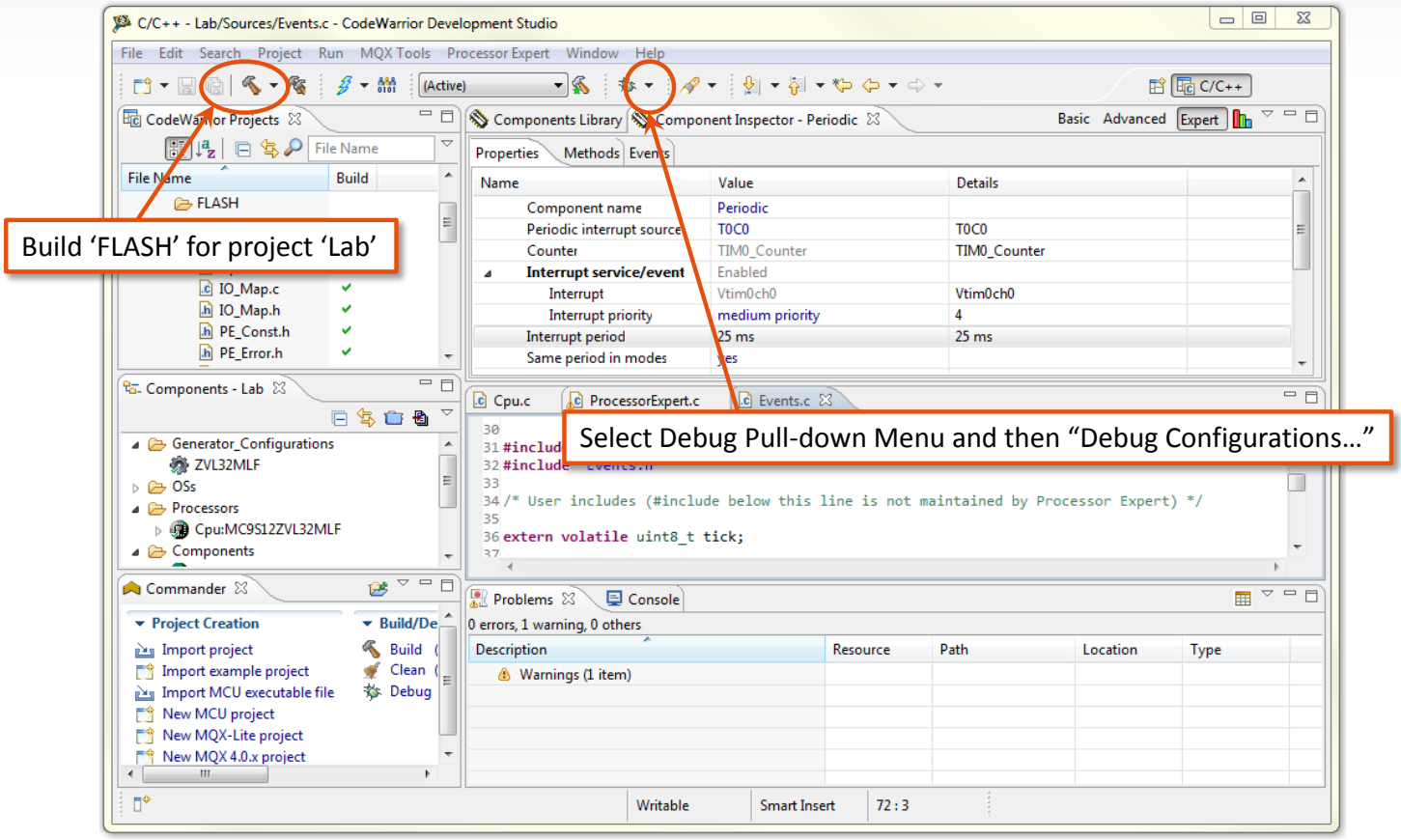
Prepare the Hardware

- Connect USB cable to the TRK-S12ZVL Evaluation Board

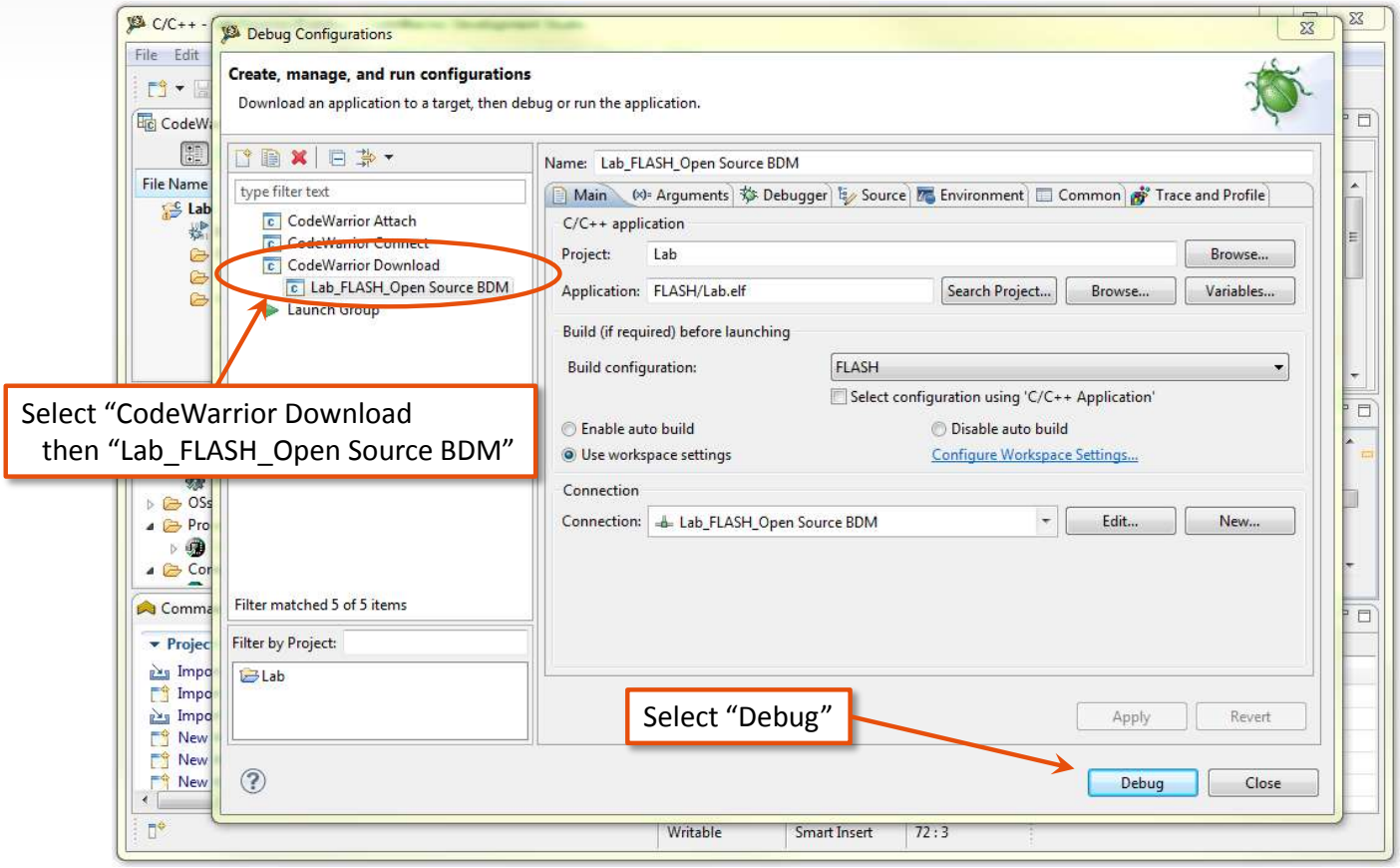


- Connect 12V Power Supply

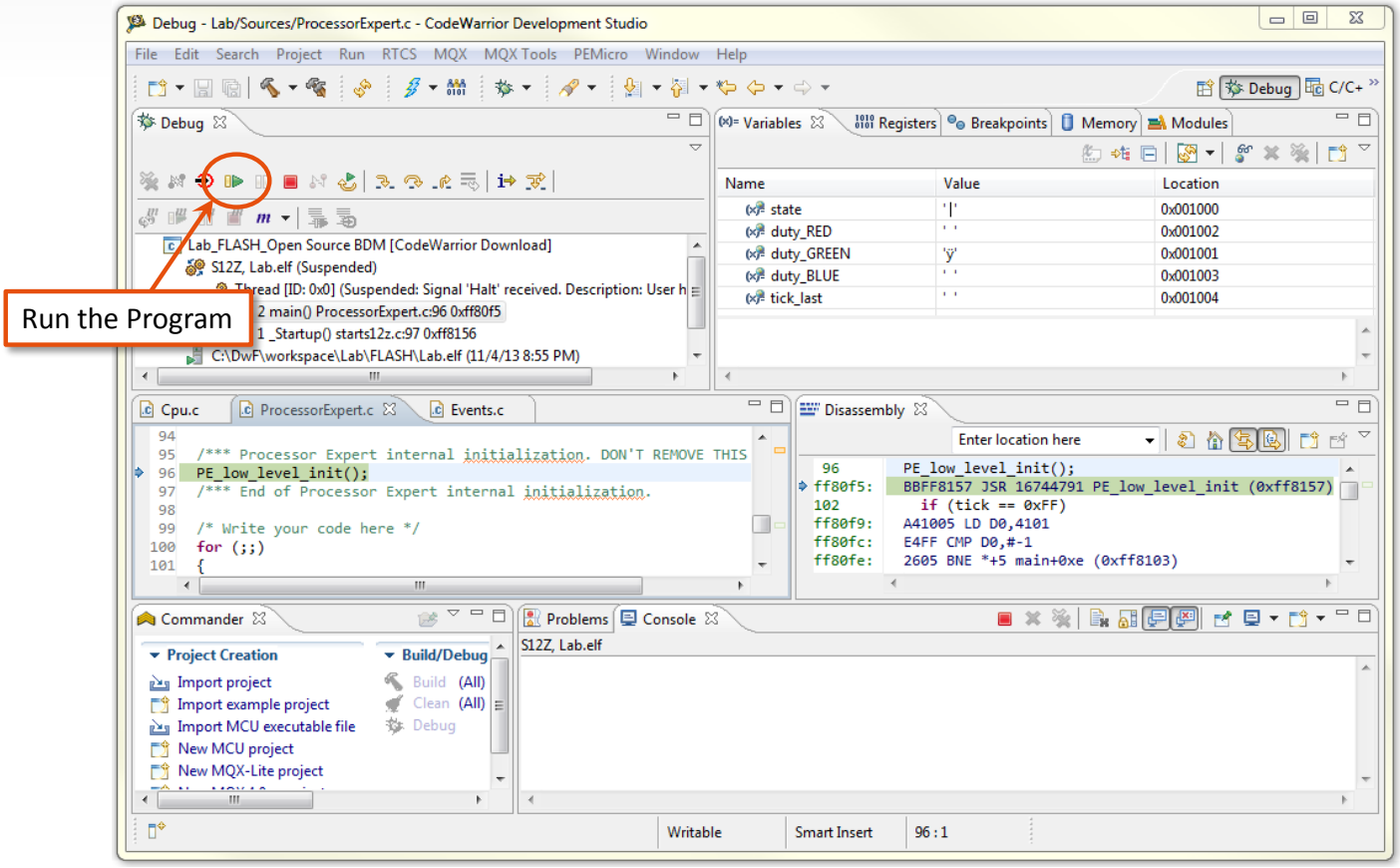
Build and Prepare to Debug



Select the Debug Configuration



Run the Program



Agenda

- Automotive Body Electronics
- MagniV Solutions and Roadmap
- Lab 1 ————————
  - Getting Started with CodeWarrior 10.4

- S12Z Enhanced CPU Core
- S12ZVM for BLDC Motor Control
- S12ZVL for General Purpose LIN
- S12ZVC for General Purpose CAN
- Lab 2 ————————
  - Developing a Project for the S12ZVL

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