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TPS61175QPWPRQ1

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TPS61175-Q1 3-A High Voltage Boost Converter with Soft-start and Programmable Switching Frequency

1 Features

- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: -40°C to 125°C Junction Operating Temperature Range
- 2.9-V to 18-V Input Voltage Range
- 3A, 40V Internal Switch
- High Efficiency Power Conversion: Up to 93%
- Frequency Set by External Resistor: 200-kHz to 2.2-MHz
- Synchronous External Switching Frequency
- User Defined Soft Start into Full Load
- Skip-Switching Cycle for Output Regulation at Light Load
- 14-pin HTSSOP Package with PowerPAD™

2 Applications

- 5V to 12V, 24V power conversion
- Supports SEPIC, Flyback topology
- ADSL Modems
- TV Tuner

3 Description

The TPS61175-Q1 is a monolithic switching regulator with integrated 3-A, 40-V power switch. It can be configured in several standard switching-regulator topologies, including boost, SEPIC and flyback. The device has a wide input voltage range to support application with input voltage from multi-cell batteries or regulated 5-V, 12-V power rails.

The TPS61175-Q1 regulates the output voltage with current mode PWM (pulse width modulation) control. The switching frequency of PWM is either set by an external resistor or an external clock signal. The user can program the switching frequency from 200-kHz to 2.2-MHz.

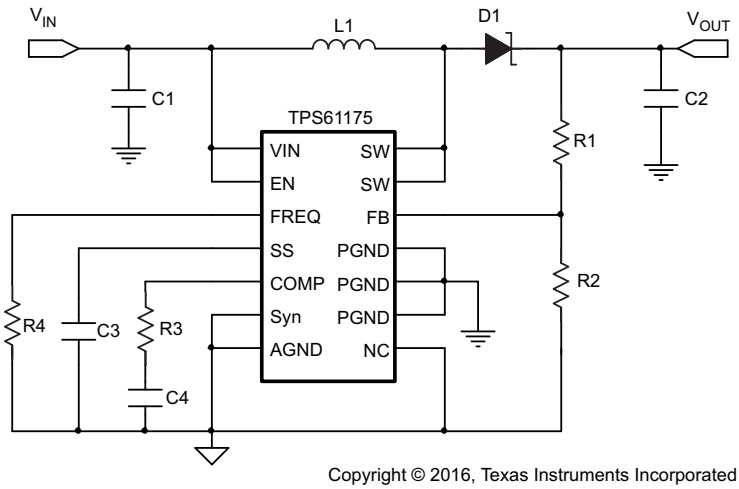
The device features a programmable soft-start function to limit inrush current during start-up, and has built-in other protection features, such as pulse-by-pulse over current limit and thermal shutdown. The TPS61175-Q1 is available in 14-pin HTSSOP package with PowerPAD.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61175-Q1	HTSSOP (14)	5.00mm x 4.40mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



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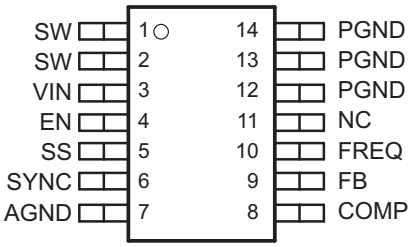
5 Revision History

Changes from Original (December 2014) to Revision A	Page
• Revised for clarity the second paragraph of *Minimum ON Time and Pulse Skipping* section.	11

6 Pin Configuration and Functions

TSSOP 14-PIN
(TOP VIEW)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VIN	3	I	The input supply pin for the IC. Connect VIN to a supply voltage between 2.9 V and 18 V. It is acceptable for the voltage on the pin to be different from the boost power stage input for applications requiring voltage beyond VIN range.
SW	1,2	I	This is the switching node of the IC. Connect SW to the switched side of the indu1ctor.
FB	9	I	Feedback pin for positive voltage regulation. Connect to the center tap of a resistor divider to program the output voltage.
EN	4	I	Enable pin. When the voltage of this pin falls below the enable threshold for more than 10 ms, the IC turns off.
COMP	8	O	Output of the internal transconductance error amplifier. An external RC network is connected to this pin to compensate the regulator.
SS	5	O	Soft start programming pin. A capacitor between the SS pin and GND pin programs soft start timing. See application section for information on how to size the SS capacitor.
FREQ	10	O	Switch frequency program pin. An external resistor is connected to this pin to set switch frequency. See application section for information on how to size the FREQ resistor.
AGND	7	I	Signal ground of the IC
PGND	12,13,14	I	Power ground of the IC. It is connected to the source of the PWM switch.
SYNC	6	I	Switch frequency synchronous pin. Customers can use an external signal to set the IC switch frequency between 200-kHz and 2.2-MHz. If not used, this pin should be tied to AGND as short as possbile to avoid noise coupling.
NC	11	I	Reserved pin. Must connect this pin to ground.
Thermal Pad			The thermal pad should be soldered to the analog ground. If possible, use thermal via to connect to top and internal ground plane layers for ideal power dissipation.

7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

	VALUE		UNIT
	MIN	MAX	
Supply Voltages on pin VIN (2)	–0.3	20	V
Voltages on pins EN(2)	–0.3	20	V
Voltage on pin FB, FREQ and COMP(2)	–0.3	3	V
Voltage on pin SYNC, SS(2)	–0.3	7	V
Voltage on pin SW(2)	–0.3	40	V
Continuous Power Dissipation	See the *Thermal Information* Table		
Operating Junction Temperature Range	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011 — All pins except 1, 7, 8, and 14	±500	
		Charged-device model (CDM), per AEC Q100-011 — Pins 1, 7, 8, and 14	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2.9		18	V
V_O	Output voltage range	V_{IN}		38	V
L	Inductor(1)	4.7		47	µH
f_{SW}	Switching frequency	200		2200	kHz
C_I	Input Capacitor	4.7			µF
C_O	Output Capacitor	4.7			µF
V_{SYN}	External Switching Frequency Logic			5	V
T_A	Operating ambient temperature	–40		125	°C
T_J	Operating junction temperature	–40		125	°C

(1) The inductance value depends on the switching frequency and end application. While larger values may be used, values between 4.7-µH and 47-µH have been successfully tested in various applications. Refer to the Inductor Selection for detail.

7.4 Thermal Information

THERMAL METRIC(1)		TPS61175-Q1 PWP 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	45.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	30.1	
ψ_{JT}	Junction-to-top characterization parameter	1.5	
ψ_{JB}	Junction-to-board characterization parameter	29.9	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

FSW = 1.2 MHz (R_{freq} = 80 kΩ), V_{IN} = 3.6V, T_A = T_J = –40°C to 125°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{IN}	Input voltage range		2.9		18	V
I_Q	Operating quiescent current into Vin	Device PWM switching without load			3.5	mA
I_{SD}	Shutdown current	EN = GND			1.5	µA
V_{UVLO}	Under-voltage lockout threshold			2.5	2.7	V
V_{hys}	Under-voltage lockout hysteresis			130		mV
ENABLE AND REFERENCE CONTROL						
$V_{(ENh)}$	EN logic high voltage	V_{IN} = 2.9 V to 18 V	1.2			V
$V_{(ENl)}$	EN logic low voltage	V_{IN} = 2.9 V to 18 V			0.4	V
$V_{(SYNh)}$	SYN logic high voltage		1.2			V
$V_{(SYNl)}$	SYN logic low voltage				0.4	V
$R_{(EN)}$	EN pull down resistor		400	800	1600	kΩ
VOLTAGE AND CURRENT CONTROL						
V_{REF}	Voltage feedback regulation voltage		1.204	1.229	1.254	V
I_{FB}	Voltage feedback input bias current				200	nA
I_{sink}	Comp pin sink current	V_{FB} = V_{REF} + 200 mV, V_{COMP} = 1 V		50		µA
I_{source}	Comp pin source current	V_{FB} = V_{REF} –200 mV, V_{COMP} = 1 V		130		µA
V_{CCLP}	Comp pin Clamp Voltage	High Clamp, V_{FB} = 1 V Low Clamp, V_{FB} = 1.5 V		3 0.75		V
$V_{(CTH)}$	Comp pin threshold	Duty cycle = 0%		0.95		V
G_{ea}	Error amplifier transconductance		240	340	440	µmho
R_{ea}	Error amplifier output resistance			10		MΩ
f_{ea}	Error amplifier crossover frequency			500		KHz
FREQUENCY						
f_S	Oscillator frequency	R_{freq} = 480 kΩ	0.16	0.21	0.26	MHz
		R_{freq} = 80 kΩ	1.0	1.2	1.4	
		R_{freq} = 40 kΩ	1.76	2.2	2.64	
D_{max}	Maximum duty cycle	V_{FB} = 1.0 V, Rfreq = 80 kΩ	89%	93%		
$V_{(FREQ)}$	FREQ pin voltage			1.229		V

Electrical Characteristics (continued)

FSW = 1.2 MHz (R_{freq} = 80 kΩ), V_{IN} = 3.6V, T_A = T_J = –40°C to 125°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SWITCH						
$R_{DS(ON)}$	N-channel MOSFET on-resistance	V_{IN} = V_{GS} = 3.6 V V_{IN} = V_{GS} = 3.0 V		0.13 0.13	0.25 0.3	Ω
I_{LN_NFET}	N-channel leakage current	V_{DS} = 40 V, T_A = 25°C			1	µA
OC, OVP AND SS						
I_{LIM}	N-Channel MOSFET current limit	D = D_{max}	3	3.8	5	A
I_{SS}	Soft start bias current	V_{SS} = 0 V		6		µA
THERMAL SHUTDOWN						
$T_{shutdown}$	Thermal shutdown threshold			160		°C
$T_{hysteresis}$	Thermal shutdown threshold hysteresis			15		°C

7.6 Timing Requirements

			MIN	TYP	MAX	UNIT
ENABLE AND REFERENCE CONTROL						
t_{off}	Shutdown delay, SS discharge	EN high to low	10			ms
FREQUENCY						
t_{min_on}	Minimum on pulse width	R_{freq} = 80 kΩ		60		ns

7.7 Typical Characteristics

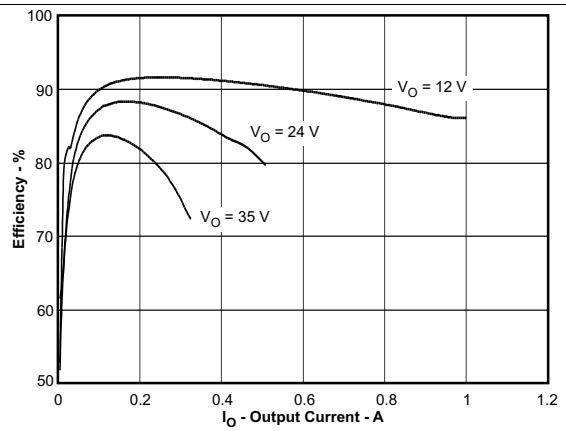


Figure 1. Efficiency vs Output Current

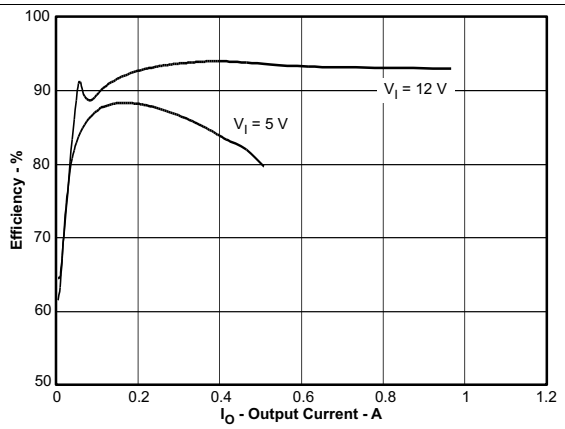


Figure 2. Efficiency vs Output Current

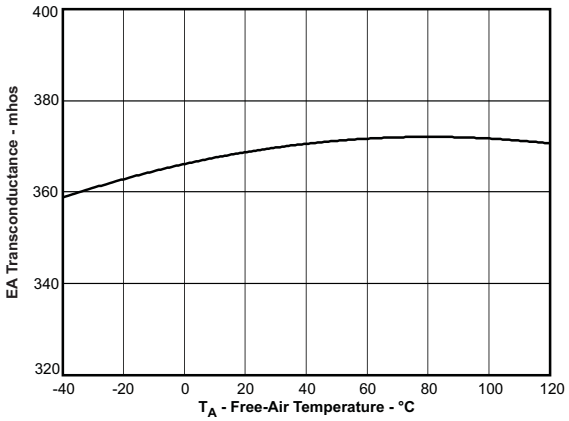


Figure 3. Error Amplifier Transconductance vs Free-Air Temperature

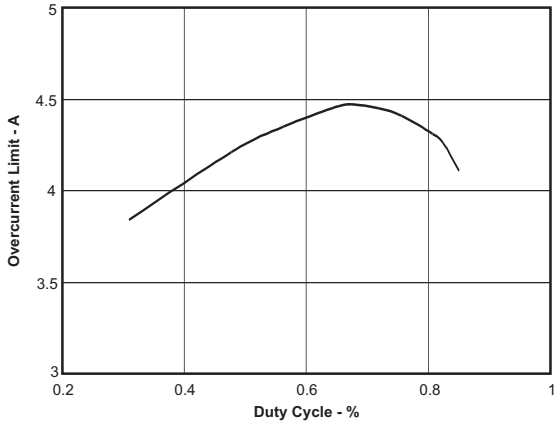


Figure 4. Overcurrent Limit vs Duty Cycle

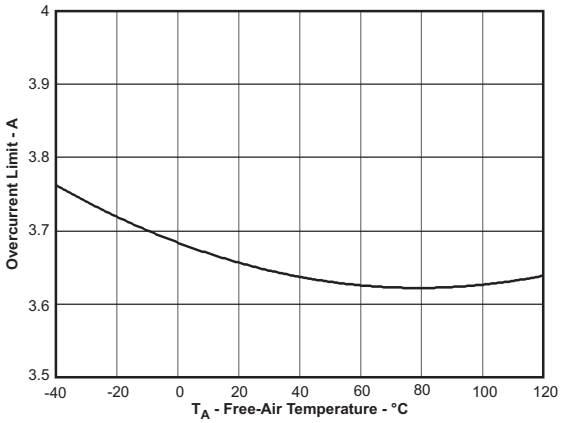


Figure 5. Overcurrent Limit vs Free-Air Temperature

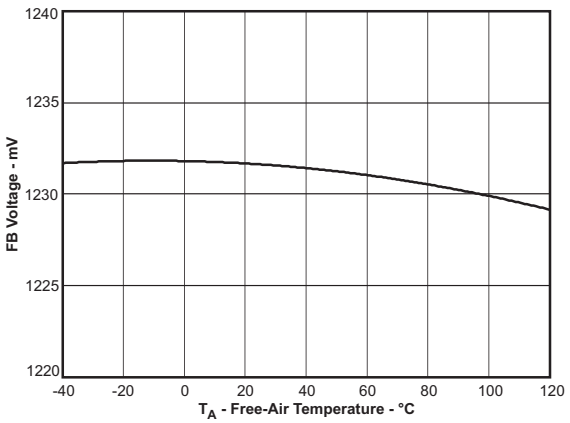


Figure 6. FB Voltages Free-Air Temperature

8 Detailed Description

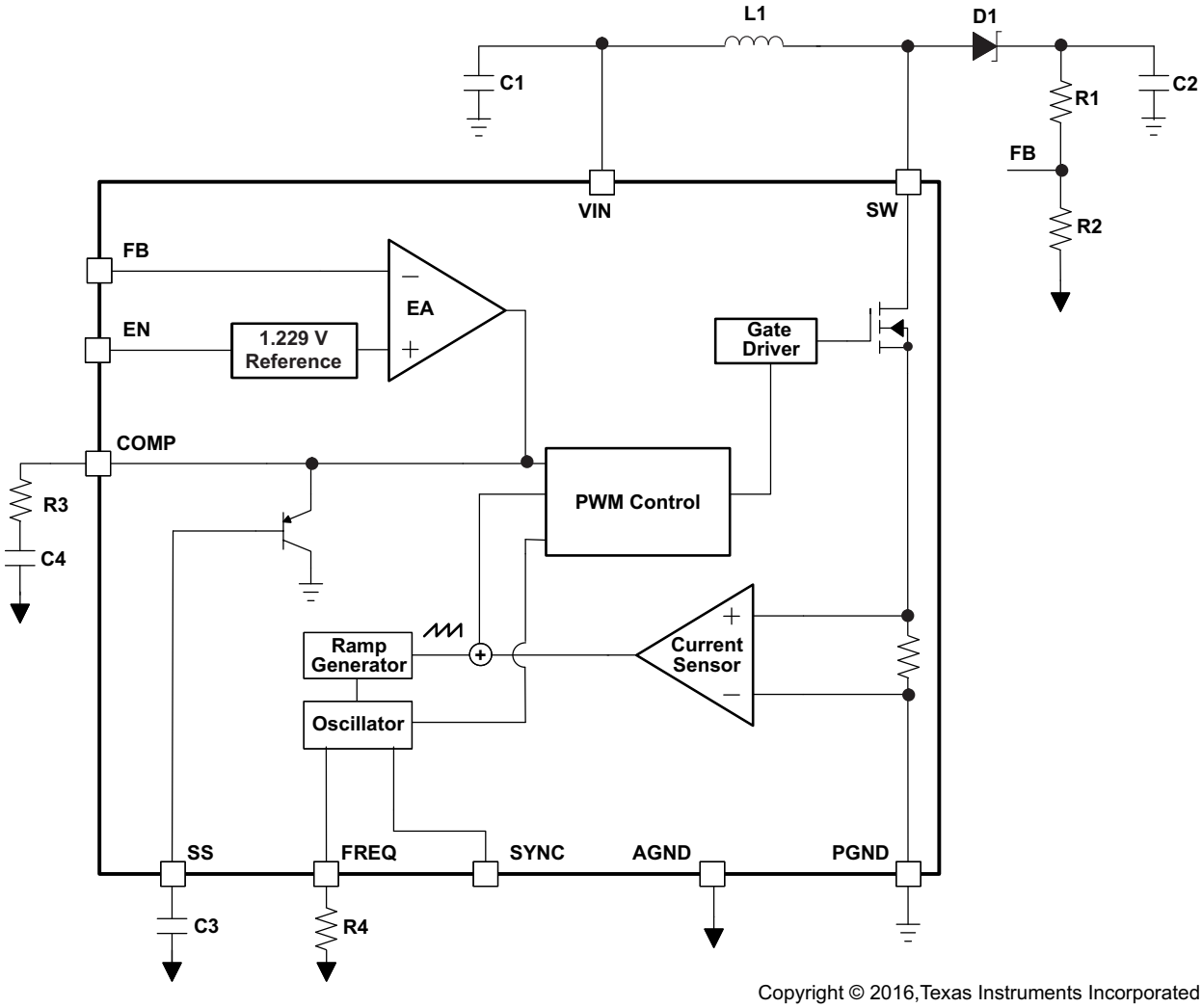
8.1 Overview

The TPS61175-Q1 integrates a 40-V low side switch FET for up to 38-V output. The device regulates the output with current mode PWM (pulse width modulation) control. The PWM control circuitry turns on the switch at the beginning of each switching cycle. The input voltage is applied across the inductor and stores the energy as inductor current ramps up. During this portion of the switching cycle, the load current is provided by the output capacitor. When the inductor current rises to the threshold set by the error amplifier output, the power switch turns off and the external Schottky diode is forward biased. The inductor transfers stored energy to replenish the output capacitor and supply the load current. This operation repeats each every switching cycle. As shown in the block diagram, the duty cycle of the converter is determined by the PWM control comparator which compares the error amplifier output and the current signal. The switching frequency is programmed by the external resistor or synchronized to an external clock signal.

A ramp signal from the oscillator is added to the current ramp to provide slope compensation. Slope compensation is necessary to avoid subharmonic oscillation that is intrinsic to the current mode control at duty cycle higher than 50%. If the inductor value is lower than 4.7µH, the slope compensation may not be adequate.

The feedback loop regulates the FB pin to a reference voltage through a transconductance error amplifier. The output of the error amplifier is connected to the COMP pin. An external RC compensation network is connected to the COMP pin to optimize the feedback loop for stability and transient response.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Switching Frequency

The switch frequency is set by a resistor (R4) connected to the FREQ pin of the TPS61175-Q1. Do not leave this pin open. A resistor must always be connected for proper operation. See Table 1 and Figure 7 for resistor values and corresponding frequencies.

Table 1. Switching Frequency vs External Resistor

R4 (kΩ)	f_{SW} (kHz)
443	240
256	400
176	600
80	1200
51	2000

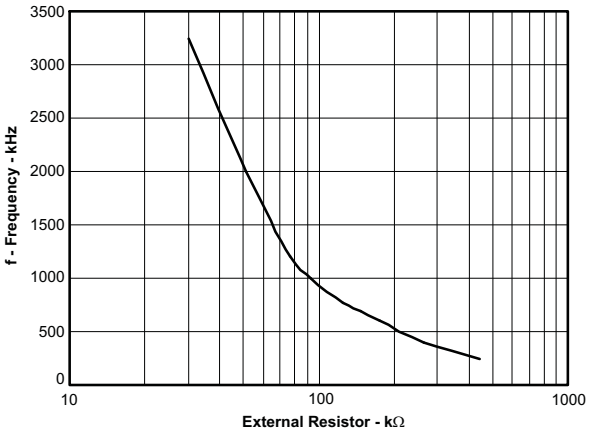


Figure 7. Switching Frequency vs External Resistor

Alternatively, the TPS61175-Q1 switching frequency will synchronize to an external clock signal that is applied to the SYNC pin. The logic level of the external clock is shown in the specification table. The duty cycle of the clock is recommended in the range of 10% to 90%. The resistor also must be connected to the FREQ pin when IC is switching by the external clock. The external clock frequency must be within ±20% of the corresponding frequency set by the resistor. For example, if the corresponding frequency as set by a resistor on the FREQ pin is 1.2-MHz, the external clock signal should be in the range of 0.96-MHz to 1.44-MHz.

If the external clock signal is higher than the frequency per the resistor on the FREQ pin, the maximum duty cycle specification (D_{MAX}) should be lowered by 2%. For instance, if the resistor set value is 2.5MHz, and the external clock is 3MHz, D_{MAX} is 87% instead of 89%.

8.3.2 Soft Start

The TPS61175-Q1 has a built-in soft start circuit which significantly reduces the start-up current spike and output voltage overshoot. When the IC is enabled, an internal bias current (6-μA typically) charges a capacitor (C3) on the SS pin. The voltage at the capacitor clamps the output of the internal error amplifier that determines the duty cycle of PWM control, thereby the input inrush current is eliminated. Once the capacitor reaches 1.8-V, the soft start cycle is completed and the soft start voltage no longer clamps the error amplifier output. Refer to Figure 7 for the soft start waveform. See Table 2 for C3 and corresponding soft start time. A 47-nF capacitor eliminates the output overshoot and reduces the peak inductor current for most applications.

Table 2. Soft Start Time vs C3

V_{IN} (V)	V_{OUT} (V)	Load (A)	C_{OUT} (µF)	f_{SW} (MHz)	C3 (nF)	t_{SS}(ms)	Overshot (mV)
5	24	0.4	10	1.2	47	4	none
					10	0.8	210
12	35	0.6	10	2	100	6.5	none
					10	0.4	300

When the EN is pulled low for 10-ms, the IC enters shutdown and the SS capacitor discharges through a 5kΩ resistor for the next soft start.

8.3.3 Overcurrent Protection

The TPS61175-Q1 has a cycle-by-cycle overcurrent limit protection that turns off the power switch once the inductor current reaches the overcurrent limit threshold. The PWM circuitry resets itself at the beginning of the next switch cycle. During an overcurrent event, the output voltage begins to droop as a function of the load on the output. When the FB voltage drops lower than 0.9-V, the switching frequency is automatically reduced to 1/4 of the set value. The switching frequency does not reset until the overcurrent condition is removed. This feature is disabled during soft start.

8.3.4 Enable and Thermal Shutdown

The TPS61175-Q1 enters shutdown when the EN voltage is less than 0.4-V for more than 10-ms. In shutdown, the input supply current for the device is less than 1.5-µA (max). The EN pin has an internal 800-kΩ pull down resistor to disable the device when it is floating.

An internal thermal shutdown turns off the device when the typical junction temperature of 160°C is exceeded. The IC restarts when the junction temperature drops by 15°C.

8.3.5 Under Voltage Lockout (UVLO)

An under voltage lockout circuit prevents mis-operation of the device at input voltages below 2.5-V (typical). When the input voltage is below the under voltage threshold, the device remains off and the internal switch FET is turned off. The under voltage lockout threshold is set below minimum operating voltage of 2.9V to avoid any transient VIN dip triggering the UVLO and causing the device to reset. For the input voltages between UVLO threshold and 2.9V, the device attempts to operate, but the specifications are not ensured.

8.4 Device Functional Modes

8.4.1 Minimum ON Time and Pulse Skipping

Once the PWM switch is turned on, the TPS61175-Q1 has minimum ON pulse width of 60-ns. This sets the limit of the minimum duty cycle of the PWM switch, and it is independent of the set switching frequency. When operating conditions result in the TPS61175-Q1 having a minimum ON pulse width less than 60-ns, the IC enters pulse-skipping mode. In this mode, the device keeps the power switch off for several switching cycles to keep the output voltage from rising above the regulated voltage. This operation typically occurs in light load condition when the PWM operates in discontinuous mode. Pulse skipping increases the output voltage ripple, see Figure 15.

When setting switching frequency higher than 1.2 MHz, TI recommends using an external synchronous clock as switching frequency to ensure pulse-skipping function works at light load. When using the internal switching frequency above 1.2 MHz, the pulse-skipping operation may not function. When the pulse-skipping function does not work at light load, the TPS61175-Q1 will always run in PWM mode with minimum ON pulse width. To keep the output voltage in regulation, a minimum load is required. The minimum load is related to the input voltage, output voltage, switching frequency, external inductor value and the maximum value of the minimum ON pulse width. Use Equation 1 and Equation 2 to calculate the required minimum load at the worst case. The maximum t_{min_ON} could be estimated to 80 ns. C_{SW} is the total parasite capacitance at the switching node SW pin. It could be estimated to 100 pF.

$$I_{(min\_load)} = \frac{1}{2} \times \frac{\left(V_{IN} \times t_{min\_ON} + (V_{OUT} + V_D - V_{IN}) \times \sqrt{L \times C_{SW}}\right)^2 \times f_{SW}}{L \times (V_{OUT} + V_D - V_{IN})} \quad \text{When } V_{OUT} + V_D - V_{IN} < V_{IN} \tag{1}$$

Device Functional Modes (continued)

$$I_{(min\_load)} = \frac{1}{2} \times \frac{\left(V_{IN} \times t_{min\_ON} + V_{IN} \times \sqrt{L \times C_{SW}}\right)^2 \times f_{SW}}{L \times \left(V_{OUT} + V_D - V_{IN}\right)} \quad \text{When } V_{OUT} + V_D - V_{IN} > V_{IN} \tag{2}$$

9 Application and Implementation

9.1 Application Information

The following section provides a step-by-step design approach for configuring the TPS61175-Q1 as a voltage regulating boost converter, as shown in Figure 8. When configured as SEPIC or flyback converter, a different design approach is required.

9.2 Typical Application

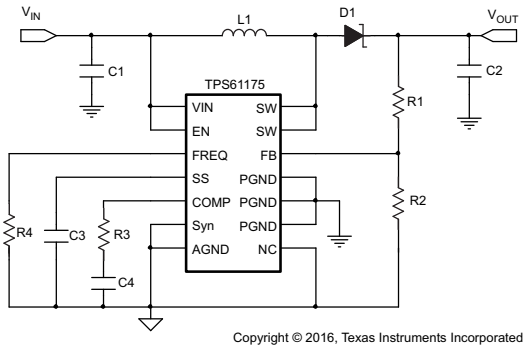


Figure 8. Boost Converter Configuration

9.2.1 Design Requirements

Table 3. Design Parameters

PARAMETERS	VALUES
Input voltage	5 V
Output voltage	24 V
Operating frequency	1.2 MHz

9.2.2 Detailed Design Procedure

9.2.2.1 Determining the Duty Cycle

The TPS61175-Q1 has a maximum worst case duty cycle of 89% and a minimum on time of 60 ns. These two constraints place limitations on the operating frequency that can be used for a given input to output conversion ratio. The duty cycle at which the converter operates is dependent on the mode in which the converter is running. If the converter is running in discontinuous conduction mode (DCM), where the inductor current ramps to zero at the end of each cycle, the duty cycle varies with changes to the load much more than it does when running in continuous conduction mode (CCM). In continuous conduction mode, where the inductor maintains a dc current, the duty cycle is related primarily to the input and output voltages as computed below:

$$D = \frac{V_{OUT} + V_D - V_{IN}}{V_{OUT} + V_D} \tag{3}$$

In discontinuous mode the duty cycle is a function of the load, input and output voltages, inductance and switching frequency as computed below:

$$D = \frac{\sqrt{2 \times (V_{OUT} + V_D) \times I_{OUT} \times L \times f_{SW}}}{V_{IN}} \tag{4}$$

All converters using a diode as the freewheeling or catch component have a load current level at which they transition from discontinuous conduction to continuous conduction. This is the point where the inductor current just falls to zero. At higher load currents, the inductor current does not fall to zero but remains flowing in a positive direction and assumes a trapezoidal wave shape as opposed to a triangular wave shape. This load boundary between discontinuous conduction and continuous conduction can be found for a set of converter parameters as follows.

$$I_{OUT(crit)} = \frac{(V_{OUT} + V_D - V_{IN}) \times V_{IN}^2}{2 \times (V_{OUT} + V_D)^2 \times f_{SW} \times L} \quad (5)$$

For loads higher than the result of the equation above, the duty cycle is given by Equation 3 and for loads less than the results of Equation 4, the duty cycle is given in Equation 5. For Equation 3 through Equation 5, the variable definitions are as follows.

- V_{OUT} is the output voltage of the converter in V
- V_D is the forward conduction voltage drop across the rectifier or catch diode in V
- V_{IN} is the input voltage to the converter in V
- I_{OUT} is the output current of the converter in A
- L is the inductor value in H
- f_{SW} is the switching frequency in Hz

Unless otherwise stated, the design equations that follow assume that the converter is running in continuous mode.

9.2.2.2 Selecting the Inductor

The selection of the inductor affects steady state operation as well as transient behavior and loop stability. These factors make it the most important component in power regulator design. There are three important inductor specifications, inductor value, DC resistance and saturation current. Considering inductor value alone is not enough.

Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can fall to some percentage of its 0-A value depending on how the inductor vendor defines saturation current. For CCM operation, the rule of thumb is to choose the inductor so that its inductor ripple current (ΔI_L) is no more than a certain percentage (RPL% = 20–40%) of its average DC value ($I_{IN(AVG)} = I_{L(AVG)}$)

$$\Delta I_L = \frac{V_{IN} \times D}{L \times f_{SW}} = \frac{(V_{OUT} + V_D - V_{IN}) \times (1 - D)}{L \times f_{SW}} = \frac{1}{\left[L \times f_{SW} \times \left(\frac{1}{V_{OUT} + V_D - V_{IN}} + \frac{1}{V_{IN}}\right)\right]}$$

$$\leq RPL\% \times \frac{P_{OUT}}{V_{IN} \times \eta_{est}} \quad (6)$$

Rearranging and solving for L gives

$$L \geq \frac{\eta_{est} \times V_{IN}}{\left[f_{SW} \left(\frac{1}{V_{OUT} + V_D - V_{IN}} + \frac{1}{V_{IN}}\right)\right] \times RPL\% \, P_{OUT}} \quad (7)$$

Choosing the inductor ripple current to closer to 20% of the average inductor current results in a larger inductance value, maximizes the converter's potential output current and minimizes EMI. Choosing the inductor ripple current closer to 40% of $I_{L(AVG)}$ results in a smaller inductance value, and a physically smaller inductor, improves transient response but results in potentially higher EMI and lower efficiency if the DCR of the smaller packaged inductor is significantly higher. Using an inductor with a smaller inductance value than computed above may result in the converter operating in DCM. This reduces the boost converter's maximum output current, causes larger input voltage and output ripple and typically reduces efficiency. Table 4 lists the recommended inductor for the TPS61175-Q1.

Table 4. Recommended Inductors for TPS61175-Q1

PART NUMBER	L (µH)	DCR MAX (mΩ)	SATURATION CURRENT (A)	SIZE (L × W × H mm)	VENDOR
D104C2	10	44	3.6	10.4x10.4x4.8	TOKO
VLF10040	15	42	3.1	10.0x9.7x4.0	TDK
CDRH105RNP	22	61	2.9	10.5x10.3x5.1	Sumida
MSS1038	15	50	3.8	10.0x10.2x3.8	Coilcraft

The device has built-in slope compensation to avoid subharmonic oscillation associated with current mode control. If the inductor value is lower than 4.7µH, the slope compensation may not be adequate, and the loop can be unstable. Applications requiring inductors above 47µH have not been evaluated. Therefore, the user is responsible for verifying operation if they select an inductor that is outside the 4.7µH–47µH recommended range.

9.2.2.3 Computing the Maximum Output Current

The over-current limit for the integrated power FET limits the maximum input current and thus the maximum input power for a given input voltage. Maximum output power is less than maximum input power due to power conversion losses. Therefore, the current limit setting, input voltage, output voltage and efficiency can all change the maximum current output ($I_{OUT(MAX)}$). The current limit clamps the peak inductor current, therefore the ripple has to be subtracted to derive maximum DC current.

$$I_{OUT(max)} = \frac{V_{IN(MIN)} \times I_{IN(AVG)} \times \eta_{est}}{V_{OUT}} = \frac{V_{IN(NIM)} \times I_{LIM} \times \eta_{est}}{V_{OUT} \times (1 + RPL\%/2)} \quad (8)$$

where

- I_{LIM} = over current limit
- η_{est}= efficiency estimate based on similar applications or computed above

For instance, when V_{IN} = 12 V is boosted to V_{OUT} = 24 V, the inductor is 10 uH, the Schottky forward voltage is 0.4-V and the switching frequency is 1.2-MHz; then the maximum output current is 1.2-A in typical condition, assuming 90% efficiency and a %RPL = 20%.

9.2.2.4 Setting Output Voltage

To set the output voltage in either DCM or CCM, select the values of R1 and R2 according to the following equation.

$$Vout = 1.229\ V \times \left(\frac{R1}{R2} + 1\right)$$
$$R1 = R2 \times \left(\frac{Vout}{1.229V} - 1\right) \quad (9)$$

Considering the leakage current through the resistor divider and noise decoupling into FB pin, an optimum value for R2 is around 10k. The output voltage tolerance depends on the V_{FB} accuracy and the tolerance of R1 and R2.

9.2.2.5 Setting the Switching Frequency

Choose the appropriate resistor from the resistance versus frequency table Table 1 or graph Figure 7. A resistor must be placed from the FREQ pin to ground, even if an external oscillation is applied for synchronization.

Increasing switching frequency reduces the value of external capacitors and inductors, but also reduces the power conversion efficiency. The user should set the frequency for the minimum tolerable efficiency.

9.2.2.6 Setting the Soft Start Time

Choose the appropriate capacitor from the soft start table Table 2. Increasing the soft start time reduces the overshoot during start-up.

9.2.2.7 Selecting the Schottky Diode

The high switching frequency of the TPS61175-Q1 demands a high-speed rectification for optimum efficiency. Ensure that the diode's average and peak current rating exceed the average output current and peak inductor current. In addition, the diode's reverse breakdown voltage must exceed the switch FET rating voltage of 40V. So, the VISHAY SS3P6L-E3/86A is recommended for TPS61175-Q1. The power dissipation of the diode's package must be larger than $I_{OUT(max)} \times V_D$

9.2.2.8 Selecting the Input and Output Capacitors

The output capacitor is mainly selected to meet the requirements for the output ripple and load transient. Then the loop is compensated for the output capacitor selected. The output ripple voltage is related to the capacitor's capacitance and its equivalent series resistance (ESR). Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by

$$C_{out} = \frac{(V_{OUT} - V_{IN})I_{out}}{V_{OUT} \times Fs \times V_{ripple}} \quad (10)$$

where, Vripple= peak to peak output ripple. The additional output ripple component caused by ESR is calculated using:

$$V_{ripple\_ESR} = I \times R_{ESR}$$

Due to its low ESR, Vripple_ESR can be neglected for ceramic capacitors, but must be considered if tantalum or electrolytic capacitors are used.

The minimum ceramic output capacitance needed to meet a load transient requirement can be estimated by Equation 11.

$$C_{OUT} = \frac{\Delta I_{TRAN}}{2 \times \pi \times f_{LOOP\text{-}BW} \times \Delta V_{TRAN}} \quad (11)$$

Where

- ΔI_{TRAN} is the transient load current step
- ΔV_{TRAN} is the allowed voltage dip for the load current step
- $f_{LOOP\text{-}BW}$ is the control loop bandwidth (that is, the frequency where the control loop gain crosses zero).

Care must be taken when evaluating a ceramic capacitor's derating under dc bias, aging and AC signal. For example, larger form factor capacitors (in 1206 size) have their self resonant frequencies in the range of the switching frequency. So the effective capacitance is significantly lower. The DC bias can also significantly reduce capacitance. Ceramic capacitors can loss as much as 50% of its capacitance at its rated voltage. Therefore, one must add margin on the voltage rating to ensure adequate capacitance at the required output voltage.

For a typical boost converter implementation, at least 4.7µF of ceramic input and output capacitance is recommended. Additional input and output capacitance may be required to meet ripple and/or transient requirements.

The popular vendors for high value ceramic capacitors are:

TDK (http://www.component.tdk.com/components.php)
Murata (http://www.murata.com/cap/index.html)

9.2.2.9 Compensating the Small Signal Control Loop

All continuous mode boost converters have a right half plane zero (f_{RHPZ}) due to the inductor being removed from the output during charging. In a traditional voltage mode controlled boost converter, the inductor and output capacitor form a small signal double pole. For a negative feedback system to be stable, the fed back signal must have a gain less than 1 before having 180 degrees of phase shift. With its double pole and RHPZ all providing phase shift, voltage mode boost converters are a challenge to compensate. In a converter with current mode control, there are essentially two loops, an inner current feedback loop created by the inductor current information sensed across R_{SENSE} (40 mΩ) and the output voltage feedback loop. The inner current loop allows the switch, inductor and modulator to be lumped together into a small signal variable current source controlled by the error amplifier, as shown in Figure 9.

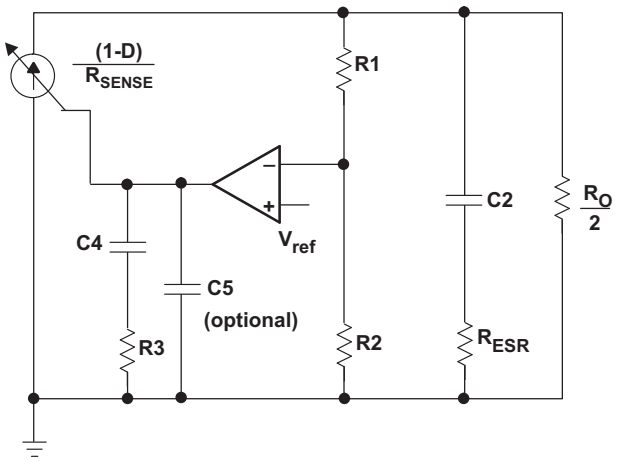


Figure 9. Small Signal Model of a Current Mode Boost in CCM

The new power stage, including the slope compensation, small signal model becomes:

$$G_{PS}(s) = \frac{R_{OUT} \times (1-D)}{2 \times R_{SENSE}} \times \frac{\left(1 + \frac{s}{2 \times \pi \times f_{ESR}}\right)\left(1 - \frac{s}{2 \times \pi \times f_{RHPZ}}\right)}{1 + \frac{s}{2 \times \pi \times f_P}} \times He(s) \quad (12)$$

Where

$$f_P = \frac{2}{2\pi \times R_O \times C2} \quad (13)$$

$$f_{ESR} \approx \frac{1}{2\pi \times R_{ESR} \times C2} \quad (14)$$

$$f_{RHPZ} = \frac{R_O}{2\pi \times L} \times \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \quad (15)$$

And

$$He(s) = \frac{1}{1 + \frac{s \times \left[\left(1 + \frac{Se}{Sn}\right) \times (1-D) - 0.5\right]}{f_{SW}} + \frac{s^2}{(\pi \times f_{SW})^2}} \quad (16)$$

He(s) models the inductor current sampling effect as well as the slope compensation effect on the small signal response.

NOTE

If Se slope dominates Sn, that is, when the inductance is oversized in order to give ripple current much smaller than the recommended 0.2 – 0.4 times the average input current, then the converter behaves more like a voltage mode converter, and the above model no longer holds.

The slope compensation in TPS61175-Q1 is shown as follow

$$Sn = \frac{V_{OUT} + V_D - V_{IN}}{L} \times R_{SENSE} \quad (17)$$

$$Se = \frac{0.32\ V / R4}{16 \times (1 - D) \times 6pF} + \frac{0.5\ \mu A}{6\ pF}$$

Where R4 is the frequency setting resistor (18)

Figure 10 shows a bode plot of a typical CCM boost converter power stage

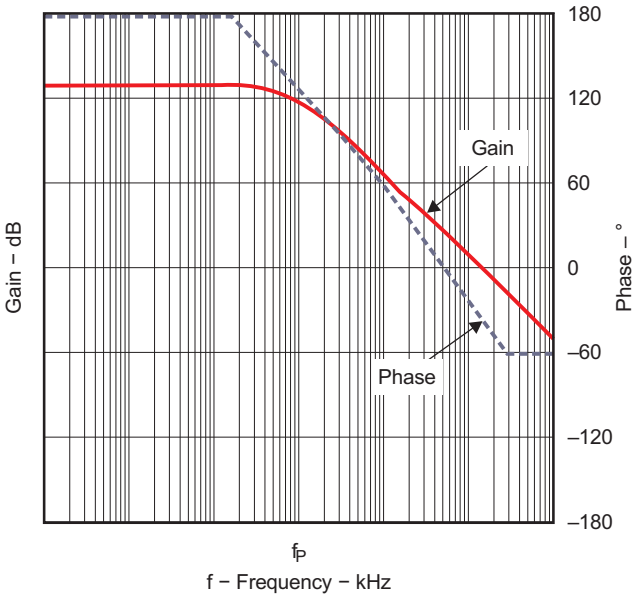


Figure 10. Bode Plot of Power Stage Gain and Phase

The TPS61175-Q1 COMP pin is the output of the internal trans-conductance amplifier. Equation 19 shows the equation for feedback resistor network and the error amplifier.

$$H_{EA} = G_{EA} \times R_{EA} \times \frac{R2}{R2 + R1} \times \frac{1 + \frac{s}{2 \times \pi \times f_Z}}{\left(1 + \frac{s}{2 \times \pi \times f_{P1}}\right) \times \left(1 + \frac{s}{2 \times \pi \times f_{P2}}\right)} \quad (19)$$

where G_{EA} and R_{EA} are the amplifier's trans-conductance and output resistance located in the *Electrical Characteristics* table.

$$f_{P1} = \frac{1}{2\pi \times R_{EA} \times C4} \quad (20)$$

$$f_{P2} = \frac{1}{2\pi \times R3 \times C5} \text{ (optional)}$$

C5 is optional and can be modeled as 10 pF stray capacitance. (21)

and

$$f_Z = \frac{1}{2\pi \times R3 \times C4} \quad (22)$$

Figure 11 shows a typical bode plot for transfer function H(s).

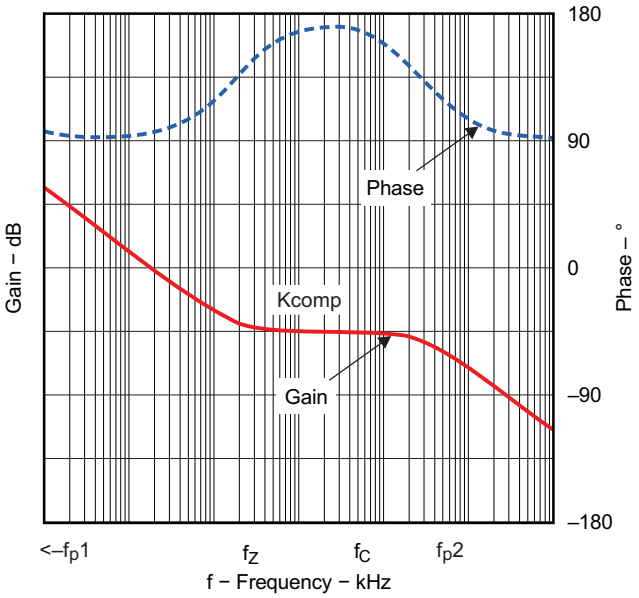


Figure 11. Bode Plot of Feedback Resistors and Compensated Amplifier Gain and Phase

The next step is to choose the loop crossover frequency, f_C. The higher in frequency that the loop gain stays above zero before crossing over, the faster the loop response will be and therefore the lower the output voltage will droop during a step load. It is generally accepted that the loop gain cross over no higher than the lower of either 1/5 of the switching frequency, f_{SW}, or 1/3 of the RHPZ frequency, f_{RHPZ}. To approximate a single pole roll-off up to f_{P2}, select R3 so that the compensation gain, K_{COMP}, at f_C on Figure 11 is the reciprocal of the gain, K_{PW}, read at frequency f_C from the Figure 10 bode plot or more simply

$$K_{COMP}(f_C) = 20 \times \log(G_{EA} \times R3 \times R2/(R2+R1)) = 1/K_{PW}(f_C)$$

This makes the total loop gain, $T(s) = G_{PS}(s) \times H_{EA}(s)$, zero at the f_C. Then, select C4 so that $f_Z \cong f_C/10$ and optional $f_{P2} > f_C \times 10$. Following this method should lead to a loop with a phase margin near 45 degrees. Lowering R3 while keeping $f_Z \cong f_C/10$ increases the phase margin and therefore increases the time it takes for the output voltage to settle following a step load.

In the TPS61175-Q1, if the FB pin voltage changes suddenly due to a load step on the output voltage, the error amplifier increases its transconductance for 8-ms in an effort to speed up the IC's transient response and reduce output voltage droop due to the load step. For example, if the FB voltage decreases 10-mV due to load change, the error amplifier increases its source current through COMP by 5 times; if FB voltage increases 11-mV, the sink current through COMP is increased to 3.5 times normal value. This feature often results in saw tooth ringing on the output voltage, shown as Figure 13. Designing the loop for greater than 45 degrees of phase margin and greater than 10db gain margin minimizes the amplitude of this ringing. This feature is disabled during soft start.

9.2.3 Application Curves

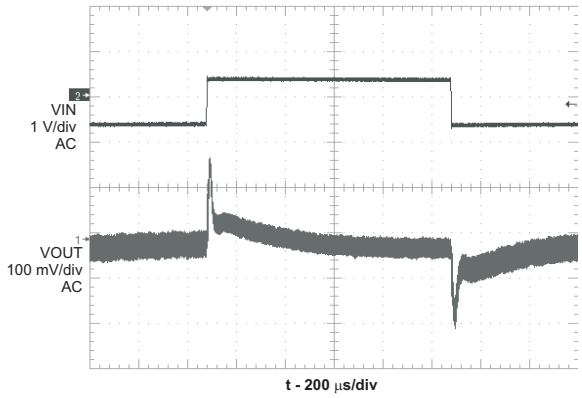


Figure 12. Line Transient Response

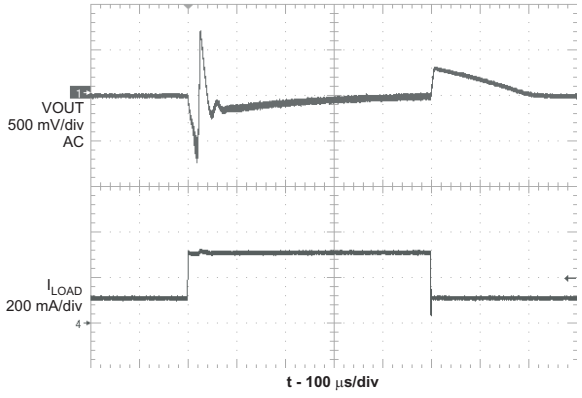


Figure 13. Load Transient Response

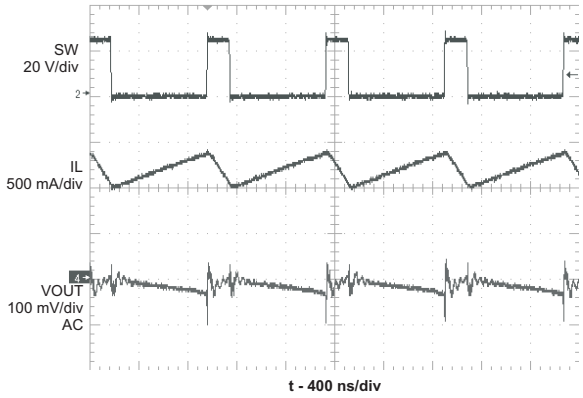


Figure 14. PWM Operation

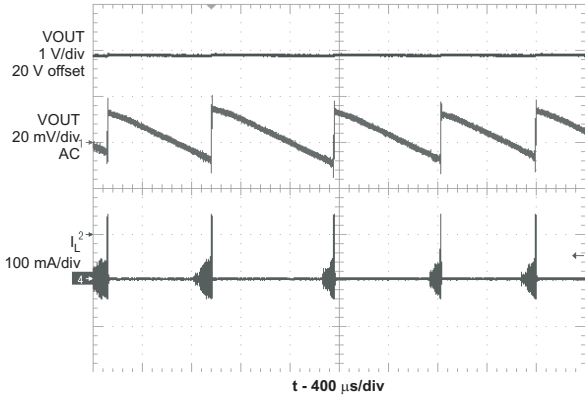


Figure 15. Pulse Skipping

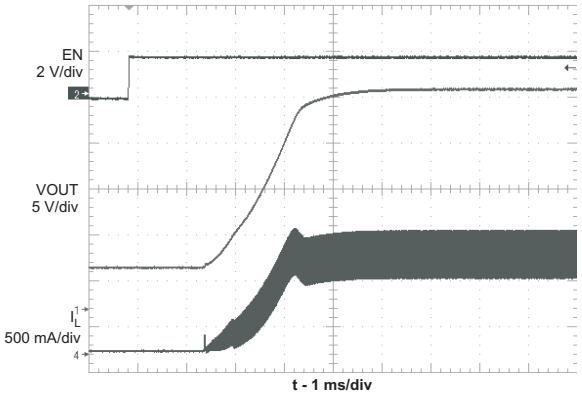


Figure 16. Soft Startup

10 Power Supply Recommendations

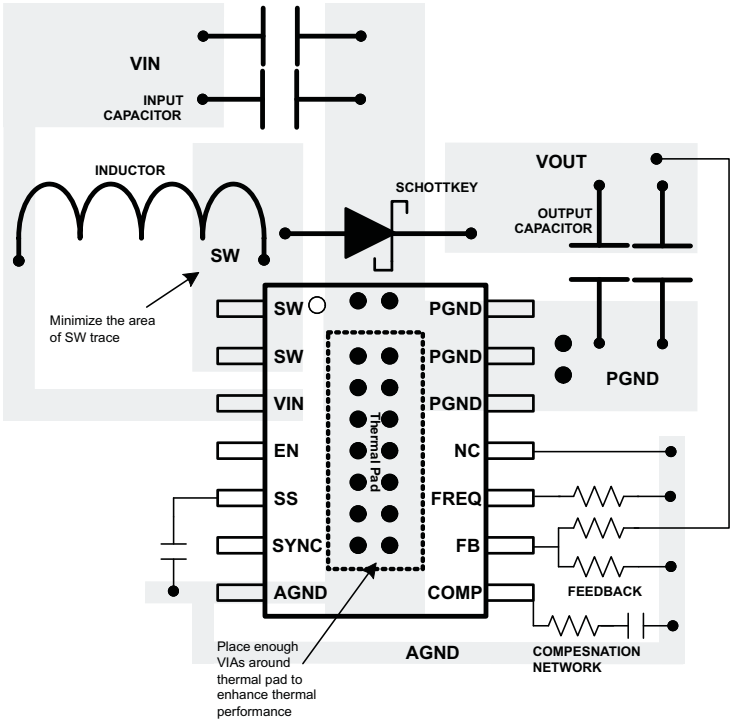
The device is designed to operate from an input voltage supply range between 2.9 V and 18 V. The input power supply's output current needs to be rated according to the supply voltage, output voltage and output current of the TPS61175-Q1.

11 Layout

11.1 Layout Guidelines

- As for all switching power supplies, especially those running at high switching frequency and high currents, layout is an important design step. If layout is not carefully done, the regulator could suffer from instability as well as noise problems. To maximize efficiency, switch rise and fall times are fast. To prevent radiation of high frequency noise (this is, EMI), proper layout of the high frequency switching path is essential.
- Minimize the length and area of all traces connected to the SW pin and always use a ground plane under the switching regulator to minimize interplane coupling.
- The high current path including the switch, Schottky diode, and output capacitor, contains nanosecond rise and fall times and should be kept as short as possible.
- The input capacitor needs not only to be close to the VIN pin, but also to the GND pin in order to reduce the input supply ripple.

11.2 Layout Example



11.3 Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation of the TPS61175-Q1. Calculate the maximum allowable dissipation, P_D(max), and keep the actual dissipation less than or equal to P_D(max). The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{125°C - T_A}{R_{\theta JA}} \quad (23)$$

where, T_A is the maximum ambient temperature for the application. $R_{\theta JA}$ is the thermal resistance junction-to-ambient given in the *Thermal Information* table.

The TPS61175-Q1 comes in a thermally enhanced TSSOP package. This package includes a thermal pad that improves the thermal capabilities of the package. The RθJA of the TSSOP package greatly depends on the PCB layout and thermal pad connection. The thermal pad must be soldered to the analog ground on the PCB. Using thermal vias underneath the thermal pad.

12 Device and Documentation Support

12.1 Trademarks

PowerPAD is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

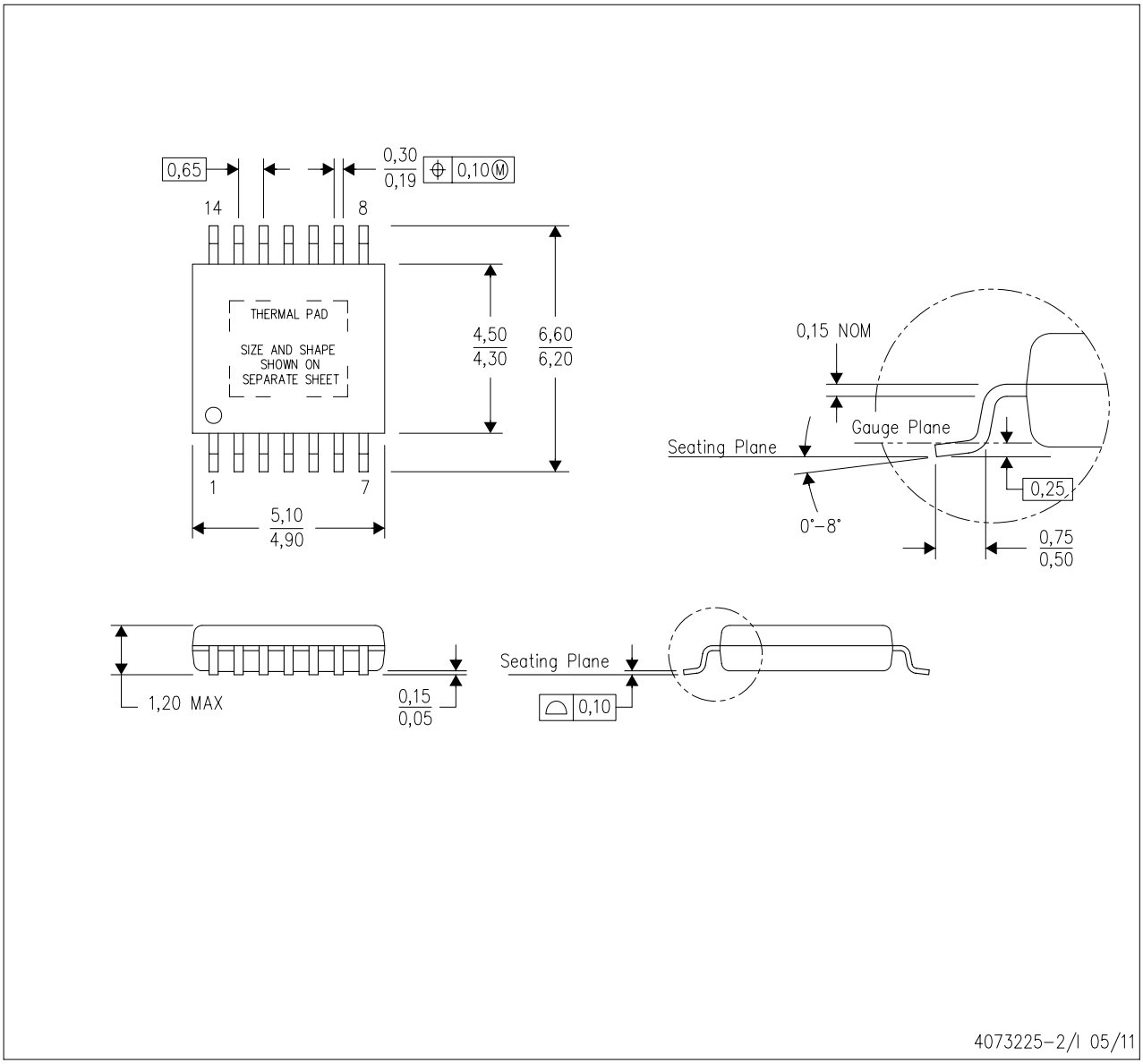
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

MECHANICAL DATA

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

THERMAL PAD MECHANICAL DATA

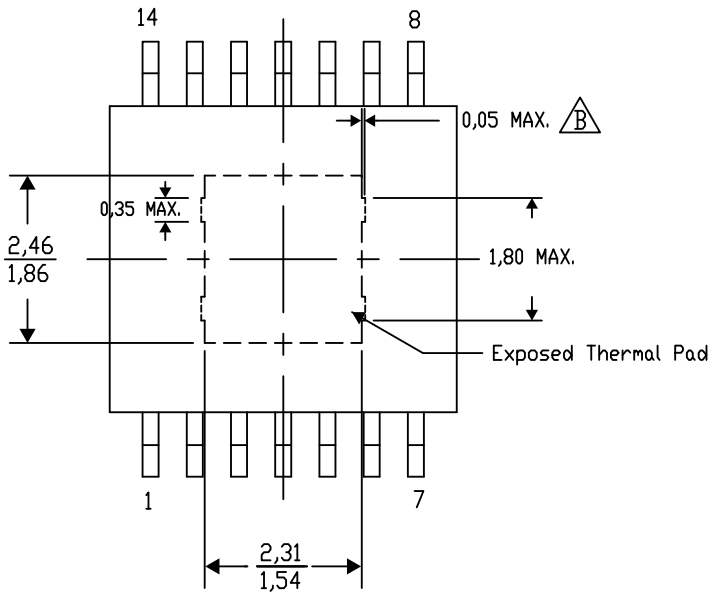
PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

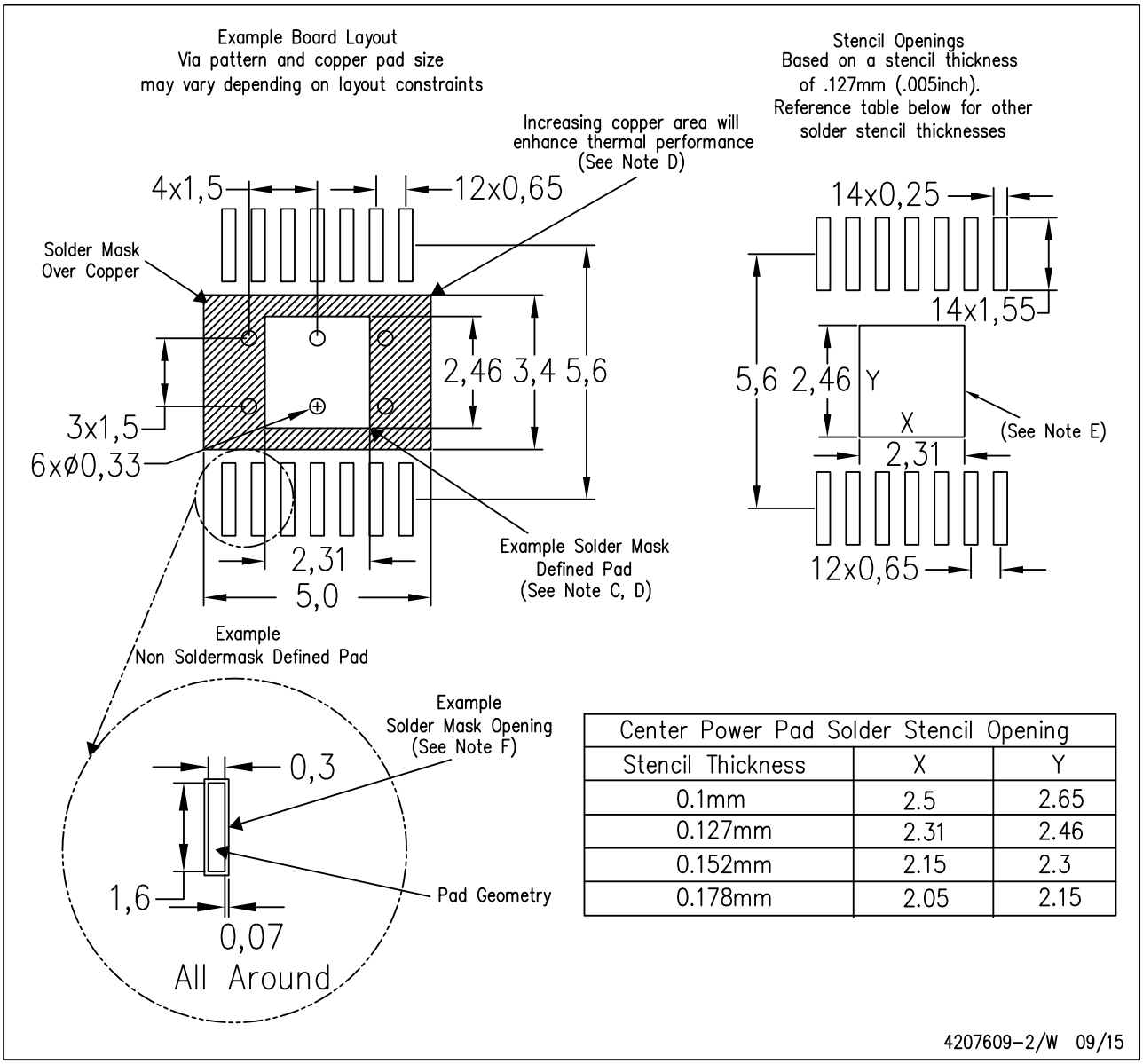
4206332–44/AJ 10/14

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61175QPWPRQ1	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	61175Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS61175-Q1 :

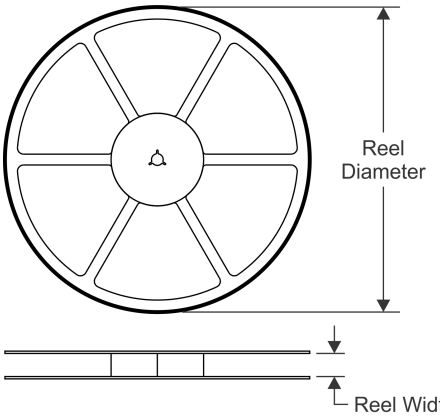
- Catalog: TPS61175

NOTE: Qualified Version Definitions:

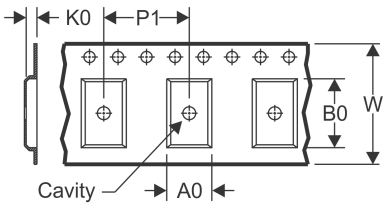
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

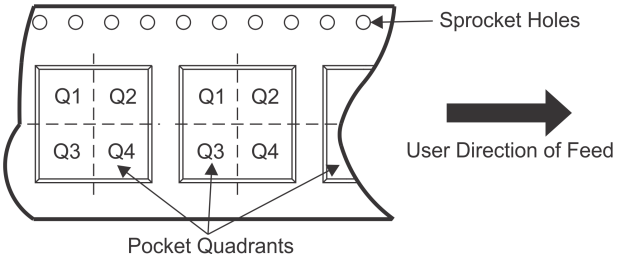


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

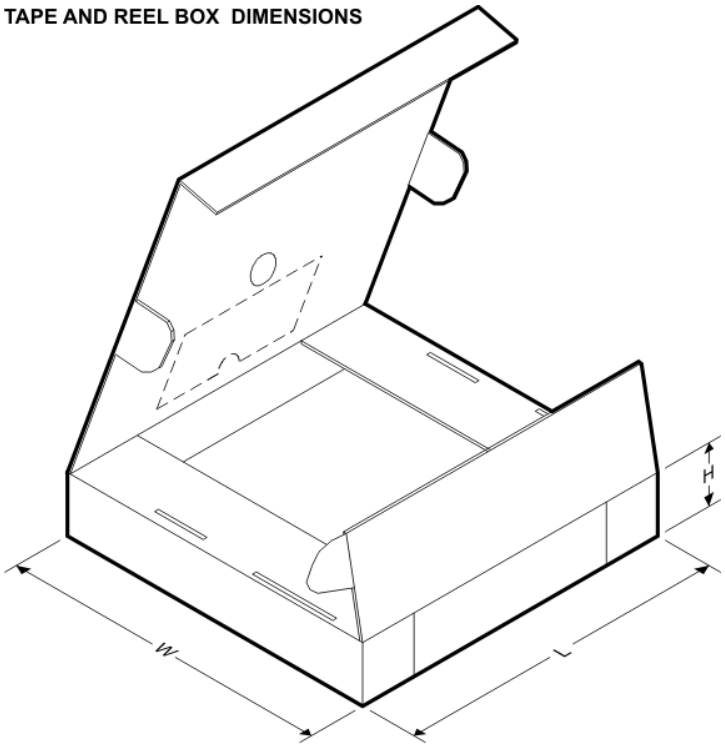


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61175QPWPRQ1	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61175QPWPRQ1	HTSSOP	PWP	14	2000	367.0	367.0	38.0

IMPORTANT NOTICE

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