December 2014

FAN6602R
Highly Integrated Green-Mode PWM Controller

Features

- Low Startup Current: 8 µA
- Low Standby Power: Under 0.1 W
- Low Operating Current in Green Mode: 600 µA
- PWM Frequency Continuously Decreasing with Cycle Skipping and Burst Mode at Light Loads
- Fixed PWM Frequency (65 kHz) with Frequency Hopping
- Full Range Frequency Hopping
- Peak-Current Mode Operation with Cycle-by-Cycle Current Limiting
- Constant Output Power Limit (Full AC Input Range)
- V_{DD} Over-Voltage Protection (OVP)
- Feedback Open-Loop Protection: 60 ms Delay
- Internal OTP Sensor with Hysteresis
- Gate Output Maximum Voltage Clamp: 13.5 V
- Gate Driving Capability: 400 mA
- Soft-Start Time: 6 ms
- Soft Driving for EMI Improvement

Applications

General-purpose switched-mode power supplies and flyback power converters, including:

- Power Adapters
- Open-Frame SMPS
- SMPS with Surge-Current Output, such as for Printers, Scanners, Motor Drivers

Description

A highly integrated PWM controller, FAN6602R provides several features to enhance the performance of flyback converters. To minimize standby power consumption, a proprietary Green Mode provides off-time modulation to continuously decrease the switching frequency under light-load conditions. Under zero-load conditions, the power supply enters Burst Mode, which completely shuts off PWM output. Output restarts just before the supply voltage drops below the Under-Voltage Lockout (UVLO) lower limit. Green Mode enables power supplies to meet international power conservation requirements.

The FAN6602R is designed for SMPS and integrates a frequency-hopping function that helps to reduce EMI emission of a power supply with minimum line filters. To compensate the power limit variation over universal input range, a current limit (V_{LIMIT}) adaptively keeps the power limit substantially constant. The gate output is clamped at 13.5 V to protect the external MOSFET from over-voltage damage.

Other protection functions include V_{DD} Over-Voltage Protection (OVP), and Over-Temperature Protection (OTP). For OTP, an external NTC thermistor can be applied to sense the ambient temperature. Protection types are shown in Table 1.

Table 1. Protection Type

Part Number	OVP	OLP	OTP / OTP2
FAN6602R	AR	AR	AR

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN6602RM6X	-40 to +105°C	6-Lead, SOT23, JEDEC MO-178 Variation AB, 1.6 mm Wide	Tape & Reel

Typical Application

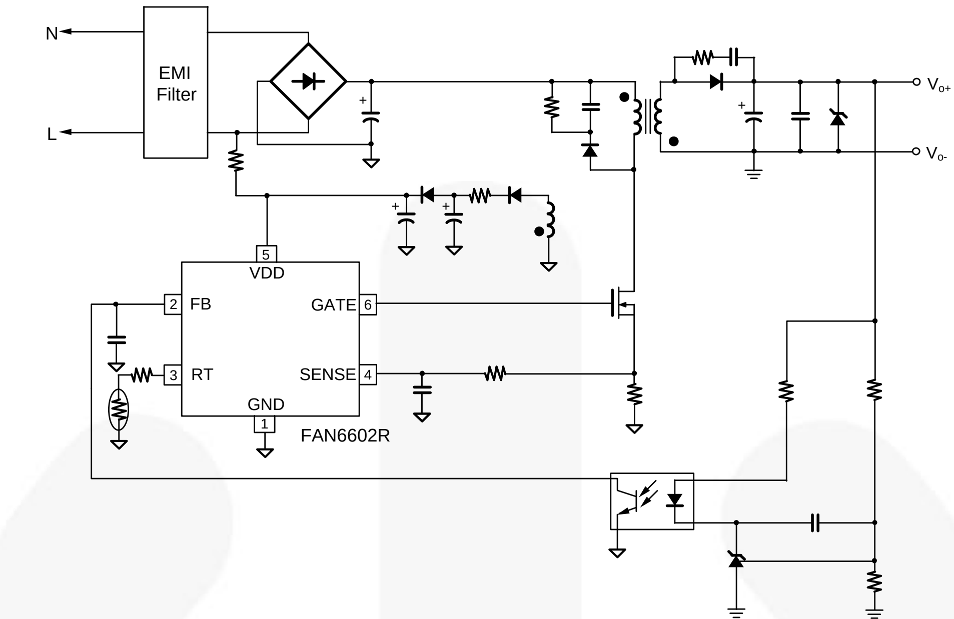

Figure 1. Typical Application

Block Diagram

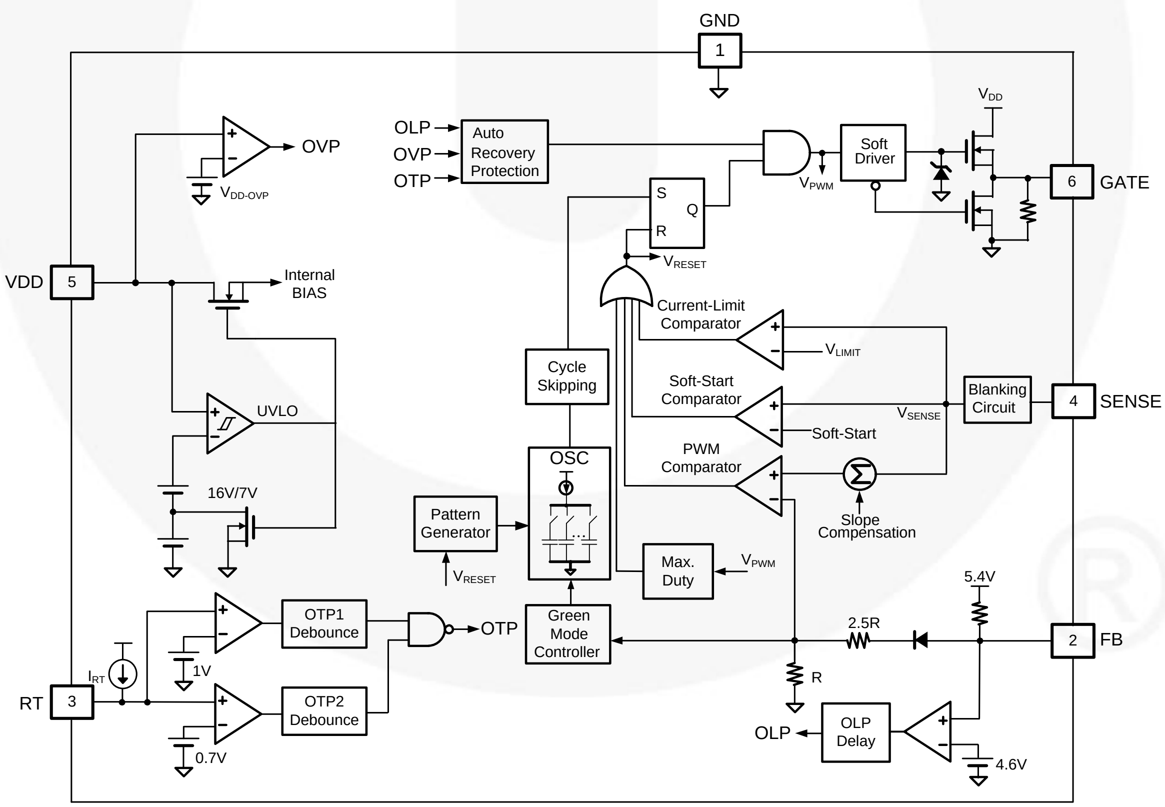

Figure 2. Block Diagram

Marking Information

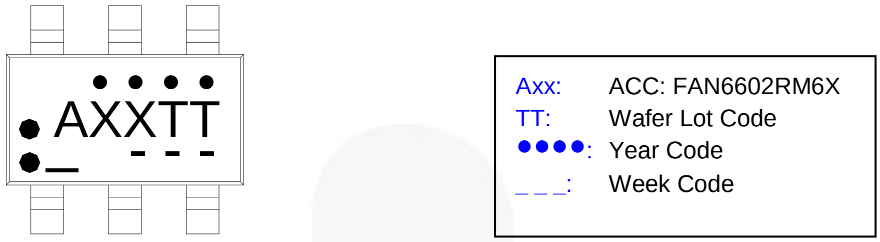

Figure 3. Top Mark

Pin Configuration

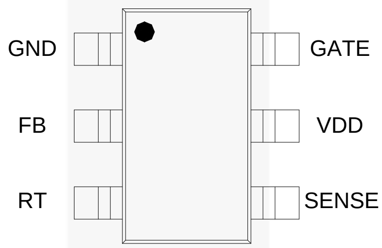

Figure 4. Pin Configuration

Pin Definitions

Pin #	Name	Function	Description
1	GND	Ground	Ground.
2	FB	Feedback	The FB pin provides the output voltage regulation signal. It provides feedback to the internal PWM comparator, so the PWM comparator can control the duty cycle. This pin also provides over-current protection. If V_{FB} is higher than the trigger level and persists at that level, the controller stops and restarts.
3	RT	Temperature Detection	An external NTC thermistor is connected from this pin to the GND pin. The impedance of the NTC decreases at high temperatures. If the voltage of the RT pin drops below the threshold, PWM output is disabled.
4	SENSE	Current Sense	This pin senses the voltage across a resistor. When the voltage reaches the internal threshold, PWM output is disabled and this activates over-current protection. This pin also provides current amplitude information for Current Mode control.
5	VDD	Power Supply	Power supply.
6	GATE	Driver Output	The totem-pole output driver for driving the power MOSFET.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. All voltage values, except differential voltages, are given with respect to GND pin.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply Voltage		30	V
V_L	Input Voltage to FB, SENSE, and RT Pins	-0.3	7.0	V
P_D	Power Dissipation at T_A<50°C		400	mW
$R\Theta_{JA}$	Thermal Resistance (Junction-to-Ambient)		244	°C/W
T_J	Operating Junction Temperature	-40	+150	°C
T_{STG}	Storage Temperature Range	-55	+150	°C
T_L	Lead Temperature, Wave Soldering, 10 Seconds		+260	°C

ESD Capability

Symbol	Parameter	Value	Unit
ESD	Human Body Model, EIA/JESD22-A114	6.0	kV
	Charge Device Model, JESD22-C101	2.0	kV

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
T_A	Operating Ambient Temperature	-40	+105	°C
V_{DD}	Supply Voltage		25	V
V_L	Input Voltage to FB, SENSE, and RT Pins	-0.3	6.0	V
T_J	Operating Junction Temperature	-40	+125	°C

Electrical Characteristics

V_{DD} = 7.5 ~ 20 V and T_A = -40 ~ 105°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD} Section						
$V_{DD\text{-}OP}$	Continuously Operating Voltage				20	V
$V_{DD\text{-}ON}$	Turn-On Threshold Voltage		15	16	17	V
$V_{DD\text{-}OFF}$	Turn-Off Threshold Voltage		6.5	7.0	7.5	V
$I_{DD\text{-}ST}$	Startup Current	$V_{DD\text{-}ON}$ – 0.16 V		8	15	µA
$I_{DD\text{-}OP1}$	Operating Supply Current in PWM Operation	V_{DD} = 20 V, V_{FB} = 3 V, Gate Open			2	mA
$I_{DD\text{-}OP2}$	Operating Supply Current when V_{FB} < $V_{FB\text{-}ZDC}$	V_{DD} = 15 V, V_{FB} < $V_{FB\text{-}ZDC}$			600	µA
$V_{DD\text{-}OVP}$	V_{DD} Over-Voltage Protection	T_A = 25°C	21.0	22.5	24.0	V
$t_{D\text{-}VDDOVP}$	V_{DD} OVP Debounce Time			50	70	µs
Feedback Input Section						
A_V	Input-Voltage to Current-Sense Attenuation		1/4.0	1/3.5	1/3.0	V/V
Z_{FB}	Input Impedance	T_A = 25°C		17		kΩ
$V_{FB\text{-}OPEN}$	FB Pin Open Voltage		5.2	5.4	5.6	V
$V_{FB\text{-}OLP}$	Threshold Voltage for Open-Loop Protection	T_A = 25°C	4.3	4.6	5.0	V
$t_{D\text{-}OLP}$	Open-Loop Protection Delay	V_{FB} > $V_{FB\text{-}OLP}$, t_{ON} > 2.5 µs,	54	60	66	ms
$t_{D\text{-}SCP}$	Secondary Short-Circuit Protection Delay	V_{FB} > $V_{FB\text{-}OLP}$, t_{ON} < 2.5 µs,	6	7	8	ms
$t_{ON\text{-}SCP}$	Short-Circuit Protection On-Time Detection	V_{FB} > $V_{FB\text{-}OLP}$,		2.9		µs
Current Sense Section						
t_{PD}	Delay to Output			100	250	ns
t_{LEB}	Leading-Edge Blanking Time		180	245	310	ns
V_{STHFL}	Flat Threshold Voltage for Current Limit	Duty > 55%	0.57	0.60	0.63	V
V_{STHVA}	Valley Threshold Voltage for Current Limit	Duty = 0%	0.36	0.39	0.42	V
$t_{SOFT\text{-}START}$	Period During Startup Time	Startup Time	4.00	6.00	9.00	ms

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Electrical Characteristics (Continued)

V_{DD} = 7.5 ~ 20 V and T_A = -40 ~ 105°C, unless otherwise noted.

Symbol	Parameter		Condition	Min.	Typ.	Max.	Unit
Oscillator Section							
f_{OSC}	Normal PWM Frequency	Center Frequency	$V_{FB} > V_{FB-N}$, $T_A = 25°C$	60	65	68	kHz
		Hopping Range	$V_{FB} \geq V_{FB-N}$, $T_A = 25°C$		±4.2		
			$V_{FB} = V_{FB-G}$(1), $T_A = 25°C$		±2.9		
t_{hop-1}	Hopping Period 1(1)		$V_{FB} \geq V_{FB-N}$		4.4		ms
f_{OSC-G}	Green Mode Minimum Frequency			18	22	26	kHz
V_{FB-N}	FB Threshold Voltage for Frequency Reduction		$T_A = 25°C$	2.35	2.50	2.65	V
V_{FB-G}	FB Voltage at f_{OSC-G}		$T_A = 25°C$	2.05	2.20	2.30	V
$V_{FB-SKIP}$	FB Threshold Voltage for Cycle Skipping Period Divide(1)		$(V_{FB-N} + V_{FB-G}) / 2$		2.35		V
t_{SKIP-N}	Cycle Skipping Period(1)		$V_{FB-SKIP} < V_{FB} < V_{FB-N}$		256		ms
t_{SKIP-G}	Cycle Skipping Period(1)		$V_{FB-G} < V_{FB} < V_{FB-SKIP}$		128		ms
V_{FB-ZDC}	FB Threshold Voltage for Zero-Duty			1.4	1.6	1.8	V
$V_{FB-ZDCR} - V_{FB-ZDC}$	ZDC Hysteresis				0.15		V
f_{DV}	Frequency Variation vs. V_{DD} Deviation		V_{DD} = 7.5 V to 21 V		0.5	2.0	%
f_{DT}	Frequency Variation vs. Temperature Deviation(1)					5.0	%

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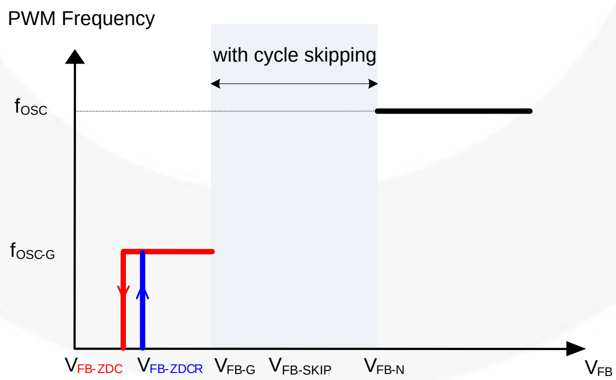

Figure 5. PWM Frequency

Electrical Characteristics (Continued)

V_{DD} = 7.5 ~ 20 V and T_A = -40 ~ 105°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
PWM Output Section						
DCY_{MAX}	Maximum Duty Cycle		68	75	85	%
V_{OL}	Output Voltage Low	V_{DD} = 15 V, I_O = 50 mA			1.5	V
V_{OH}	Output Voltage High	V_{DD} = 8 V, I_O = 50 mA	6			V
t_R	Rising Time (with Soft Driving)	Gate = 1 nF		150	200	ns
t_F	Falling Time	Gate = 1 nF		35	80	ns
V_{CLAMP}	Gate Output Clamping Voltage	V_{DD} = 20 V	12.0	13.5	15.0	V
$I_{O\text{-}SOURCE}$	Gate Source Driving Capability[1]	V_{DD} = 15 V		400		mA
$I_{O\text{-}SINK}$	Gate Sink Driving Capability[1]	V_{DD} = 15 V		400		mA
Over-Temperature Protection (OTP) Section						
R_{RT}	Maximum External Resistance of RT Pin to Trigger Protection	T_A = 25°C	9	10	11	kΩ
V_{OTP}	Threshold Voltage for Over-Temperature Protection		0.94	1.03	1.09	V
I_{RT}	Output Current of RT Pin	T_A = 25°C	92	100	108	µA
t_{DOTP}	Over-Temperature Debounce Time	V_{FB} = $V_{FB\text{-}N}$	13.5	17.0	20.5	ms
V_{OTP2}	Second Threshold Voltage for Over-Temperature Protection		0.65	0.72	0.78	V
t_{DOTP2}	Second Over-Temperature Debounce Time		50	125	200	µs
T_{OTP}	Protection Junction Temperature[1,2]			+135		°C
$T_{Restart}$	Restart Junction Temperature [1,3]			T_{OTP}-25		°C

Notes:
1. Guarantee by design.
2. When activated, the output is disabled.
3. The threshold temperature for enabling the output again and resetting the after OTP has been activated.

Typical Performance Characteristics

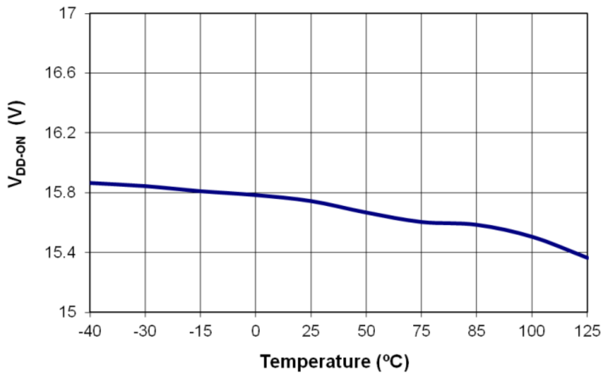

Figure 6. Turn-On Threshold Voltage (V_{DD-ON}) vs. Temperature

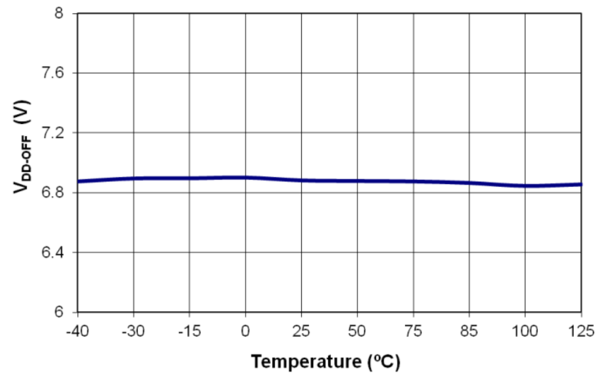

Figure 7. Turn-Off Threshold Voltage (V_{DD-OFF}) vs. Temperature

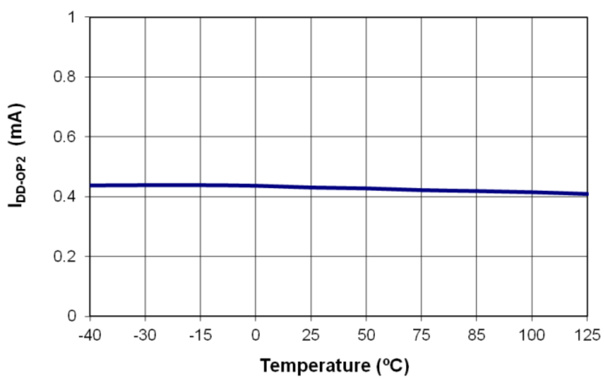

Figure 8. Operating Current (I_{DD-OP2}) vs. Temperature

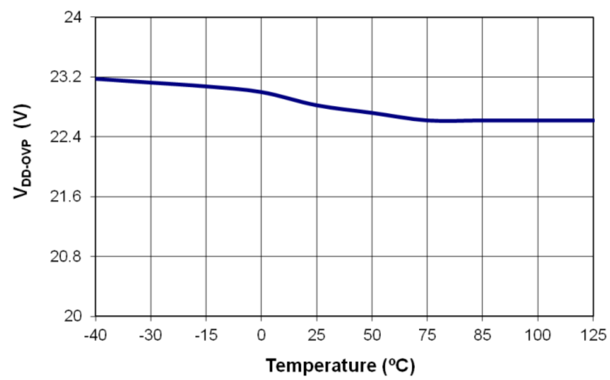

Figure 9. V_{DD} Over-Voltage Protection (V_{DD-OVP}) vs. Temperature

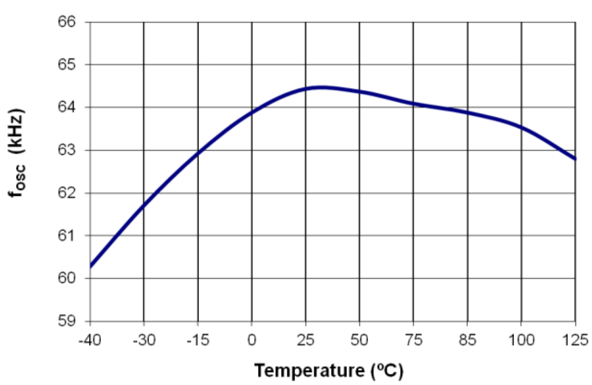

Figure 10. Center Frequency (f_{OSC}) vs. Temperature

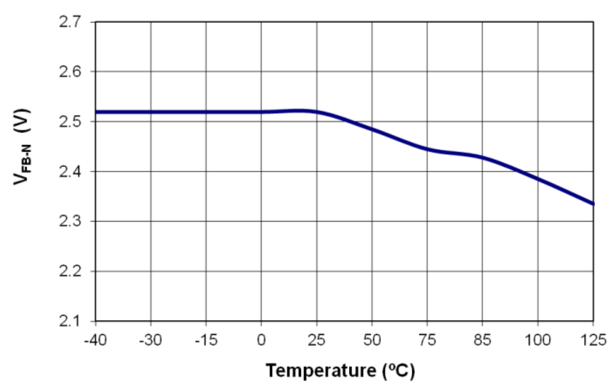

Figure 11. FB Threshold Voltage for Frequency Reduction (V_{FB-N}) vs. Temperature

Typical Performance Characteristics (Continued)

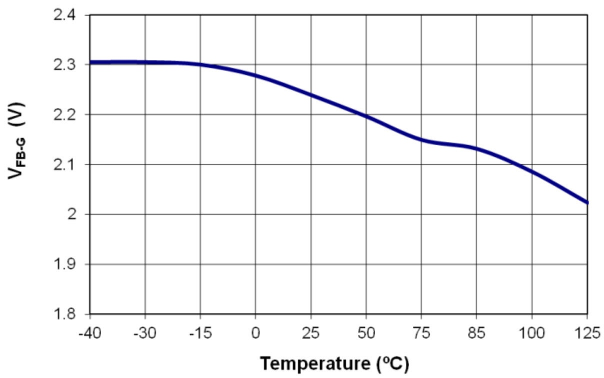

Figure 12. FB Voltage at f_{OSC-G} (V_{FB-G}) vs. Temperature

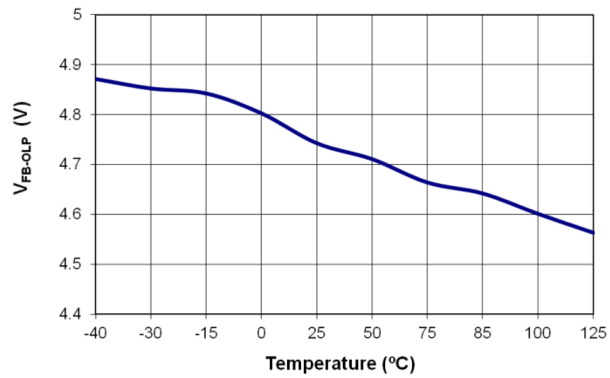

Figure 13. Threshold Voltage for Open-Loop Protection (V_{FB-OLP}) vs. Temperature

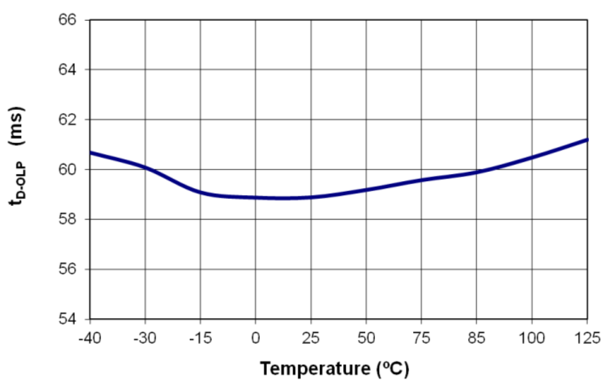

Figure 14. Open-Loop Protection Delay (t_{D-OLP}) vs. Temperature

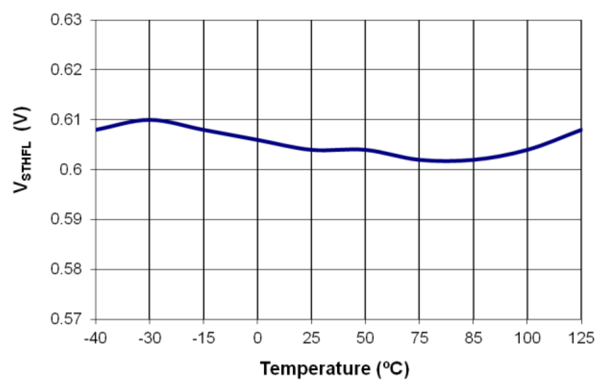

Figure 15. Flat Threshold Voltage for Current Limit (V_{STHFL}) vs. Temperature

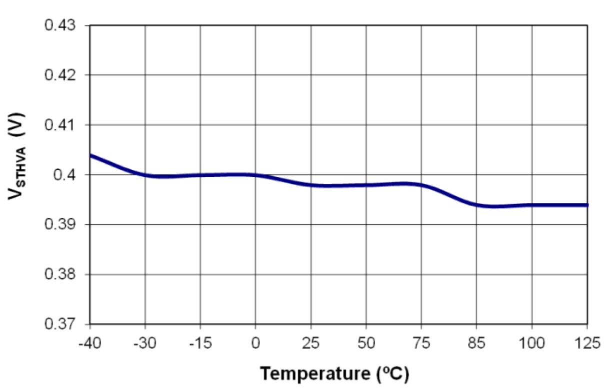

Figure 16. Valley Threshold Voltage for Current Limit (V_{STHVA}) vs. Temperature

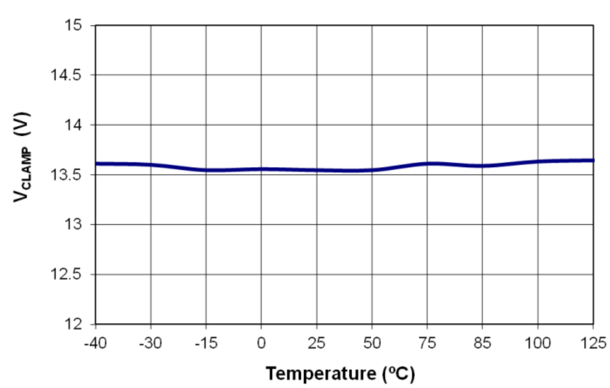

Figure 17. Gate Output Clamping Voltage (V_{CLAMP}) vs. Temperature

Typical Performance Characteristics (Continued)

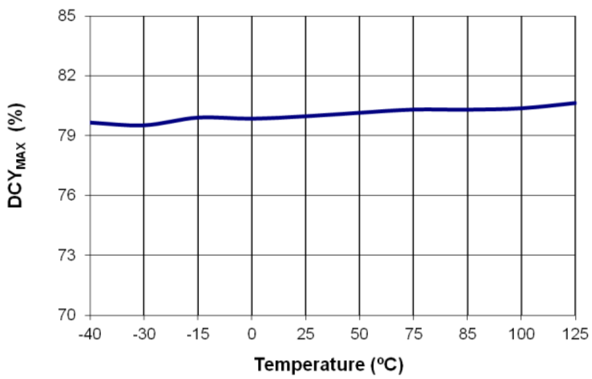

Figure 18. Maximum Duty Cycle (DCY_{MAX}) vs. Temperature

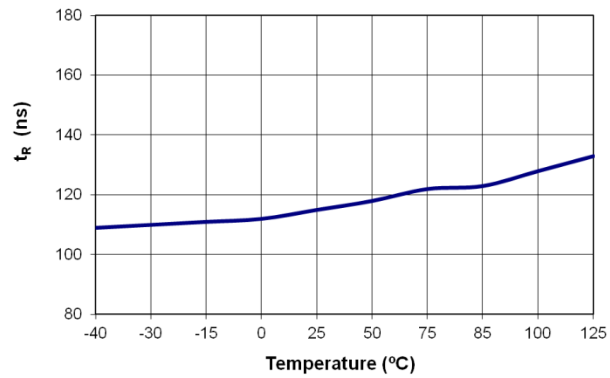

Figure 19. Rising Time (t_R) vs. Temperature

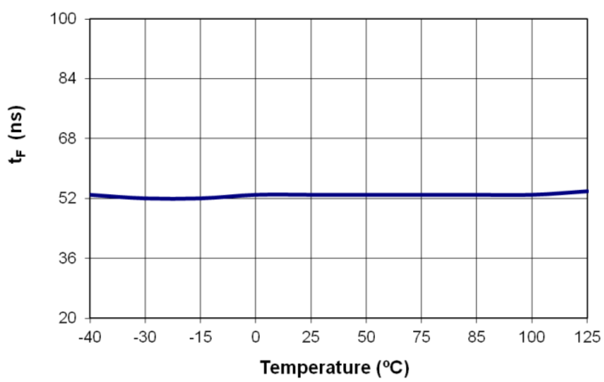

Figure 20. Falling Time (t_F) vs. Temperature

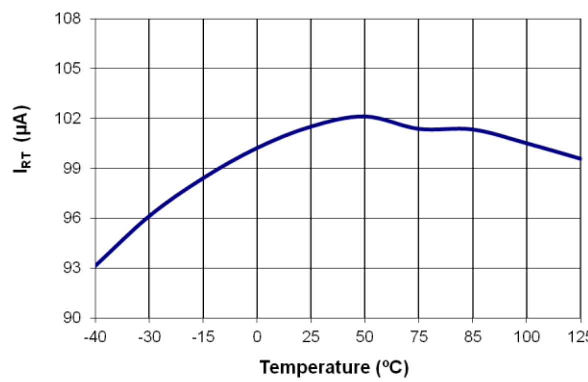

Figure 21. Output Current of RT Pin (I_{RT}) vs. Temperature

Operation Description

Startup Operation

Figure 22 shows a typical startup circuit and transformer auxiliary winding for a typical application. Before switching operation begins, FAN6602R consumes only startup current (typically 8 µA) and the current supplied through the startup resistor charges the V_{DD} capacitor (C_{DD}). When V_{DD} reaches turn-on voltage of 16 V (V_{DD-ON}), switching begins and the current consumed increases to 2 mA. The hold-up capacitor continues to supply VDD before the energy can be delivered from the auxiliary winding of the main transformer. The large hysteresis of V_{DD} (7 V) provides more holdup time, which allows using a small capacitor for V_{DD}. The startup resistor is typically connected to AC line.

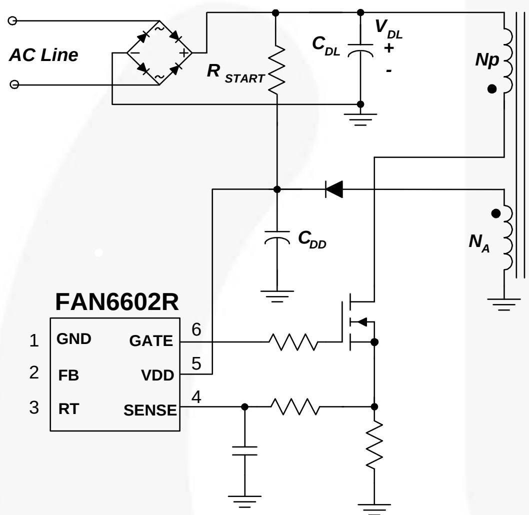

Figure 22. Startup Circuit

Green-Mode Operation

The FAN6602R uses feedback voltage (V_{FB}) as an indicator of the output load and modulates the PWM frequency, as shown in Figure 23, such that the switching frequency decreases as load decreases. In heavy-load conditions, the switching frequency is 65 kHz. Once V_{FB} decreases below V_{FB-N} (2.5 V), the PWM frequency starts to linearly decrease with cycle skipping from 65 kHz to 22 kHz to reduce the switching losses. As V_{FB} decreases below V_{FB-G} (2.2 V), the switching frequency is fixed at 22 kHz and FAN6602R enters "deep" Green Mode, where the operating current decreases to 600 µA (typical), further reducing the standby power consumption. As V_{FB} decreases below V_{FB-ZDC} (1.6 V), FAN6602R enters Burst-Mode operation. When V_{FB} drops below V_{FB-ZDC}, switching stops and the output voltage starts to drop, which causes the feedback voltage to rise. Once V_{FB} rises above $V_{FB-ZDCR}$, switching resumes. Burst Mode alternately enables and disables switching, thereby reducing switching loss in Standby Mode.

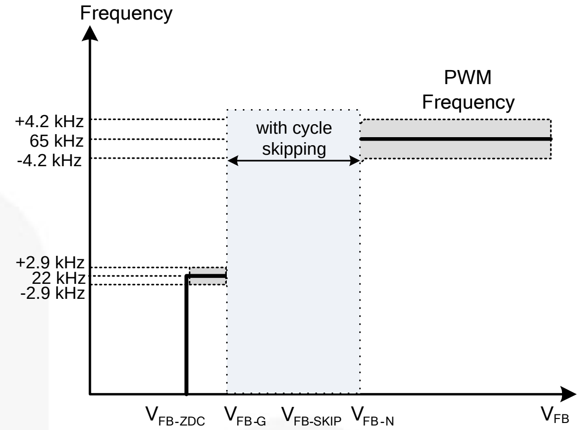

Figure 23. PWM Frequency

Frequency Hopping

EMI reduction is accomplished by frequency hopping, which spreads the energy over a wider frequency range than the bandwidth measured by the Electromagnetic Interference (EMI) test equipment. An internal frequency-hopping circuit changes the switching frequency between 60.8 kHz and 69.2 kHz with a period of 4.4 ms.

Leading-Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs on the sense resistor. To avoid premature termination of the switching pulse, a leading-edge blanking time (t_{LEB}) is built in. During this blanking period, the current-limit comparator is disabled and cannot switch off the gate driver.

Gate Output / Soft Driving

The BiCMOS output stage is a fast totem-pole gate driver. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. The output driver is clamped by an internal 13.5 V Zener diode to protect power MOSFET transistors against undesirable gate over voltage. A soft-driving circuit is implemented to minimize EMI.

Soft-Start

For many applications, it is necessary to minimize the inrush current at startup. The built-in 6 ms soft-start circuit significantly reduces the startup current spike and output voltage overshoot.

Slope Compensation

The sensed voltage across the current-sense resistor is used for peak-current-mode control and pulse-by-pulse current limiting. Built-in slope compensation improves stability and prevents sub-harmonic oscillation. FAN6602R inserts a synchronized positive-going ramp at every switching cycle as slope compensation.

Protections

Self-protective functions include V_{DD} Over-Voltage Protection (OVP), Open-Loop / Overload Protection (OLP), Over-Current Protection (OCP), Short-Circuit Protection (SCP) and Over-Temperature Protection (OTP). All the self-protective functions are Auto-Restart (AR) Mode protections

Auto-Restart (AR) Mode Protection

Once a fault condition is detected, switching is terminated and the MOSFET remains off. This causes V_{DD} to fall because no more power is delivered from auxiliary winding. When V_{DD} falls to $V_{DD\text{-}OFF}$ (7 V), the protection is reset and the operating current reduces to startup current, which causes V_{DD} to rise. FAN6602R resumes normal operation when V_{DD} reaches $V_{DD\text{-}ON}$ (16 V). In this manner, the auto-restart can alternately enable and disable the switching of the MOSFET until the fault condition is eliminated.

Over-Current Protection (OCP)

FAN6602R over-current protection is a pulse-by-pulse bias current limit threshold (V_{STHVA} and V_{STHFL}) that turns off the MOSFET once the sensing voltage of MOSFET drain current reaches the threshold. The current limit compensates the power-limit variation over the universal input range and adaptively keeps the power limit substantially constant.

Open-Loop / Overload Protection (OLP)

When the upper branch of the voltage divider for the shunt regulator is broken, no current flows through the photo-coupler transistor, which pulls up the feedback voltage to 5.4 V.

When feedback voltage is above 4.6 V for longer than 60 ms, OLP is triggered. This protection is also triggered when the SMPS output drops below the nominal value for longer than 60 ms due to the overload condition.

If the secondary output-short situation occurs when the feedback voltage is above 4.6 V, protection time is 7 ms for shorter debounce time.

V_{DD} Over-Voltage Protection (OVP)

V_{DD} over-voltage protection prevents IC damage caused by over-voltage on the V_{DD} pin. Once the V_{DD} voltage is over the over-voltage protection voltage ($V_{DD\text{-}OVP}$), and lasts for $t_{D\text{-}VDDOVP}$, the PWM pulses are disabled. A debounce time (typically 50 µs) prevents false triggering by switching noise.

Over-Temperature Protection (OTP)

The OTP circuit is composed of current source and voltage comparators. Typically, an NTC thermistor is connected between the RT and GND pins. If the voltage of this pin drops below a threshold of 1.03 V, PWM output is disabled after t_{DOTP} debounce time. If this pin voltage drops below 0.72 V, it triggers the protection immediately after t_{DOTP2} debounce time.

Typical Application Circuit (Netbook Adapter by Flyback)

Application	Fairchild Devices	Input Voltage Range	Output
Netbook Adapter	FAN6602R	90~265 V_{AC}	19 V / 2.1 A (40 W)

Features

- High efficiency (>85.3% at full-load condition) meeting EPS regulation with enough margin
- Low standby (pin<0.1 W at no-load condition)
- Soft-start time: 5 ms

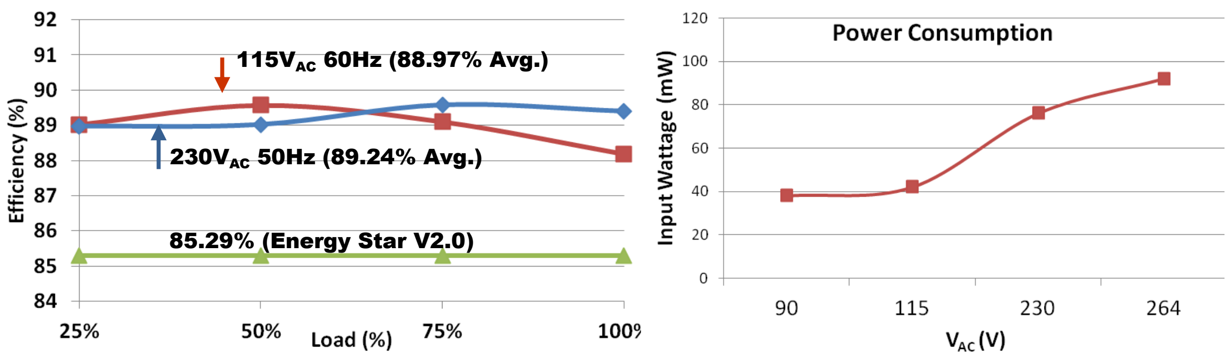

Figure 30. Measured Efficiency and Power Saving

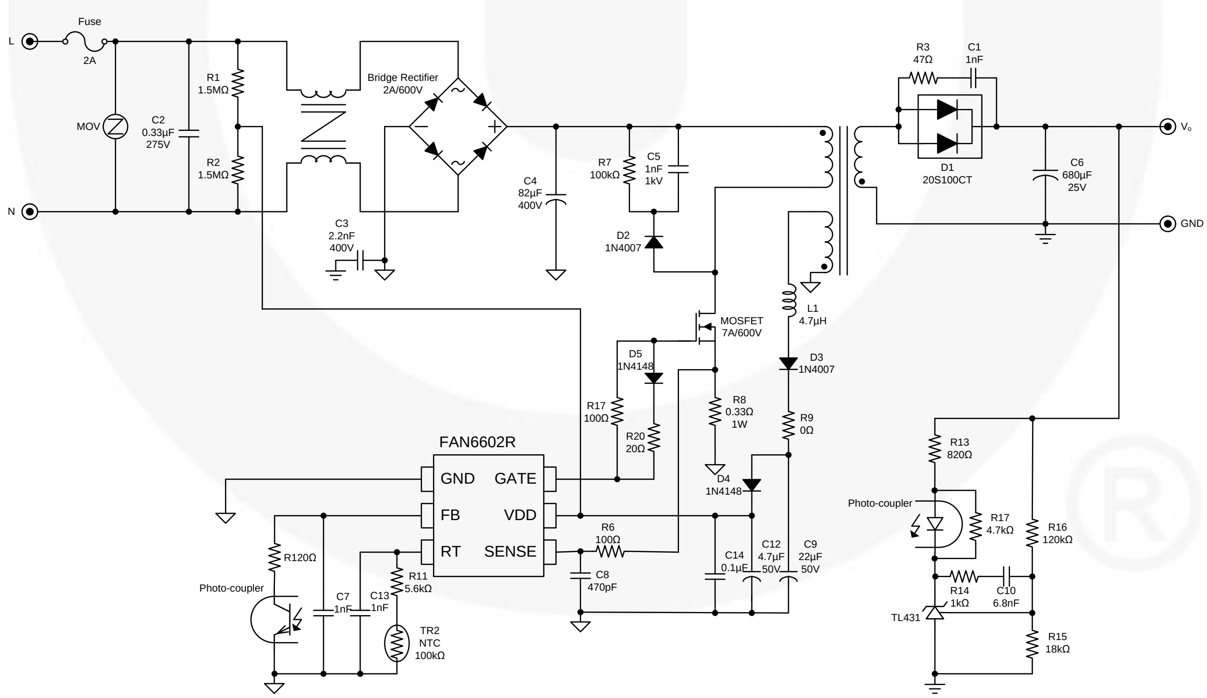

Figure 24. Schematic of Typical Application Circuit

Transformer Specification

- Core: RM 8
- Bobbin: RM 8

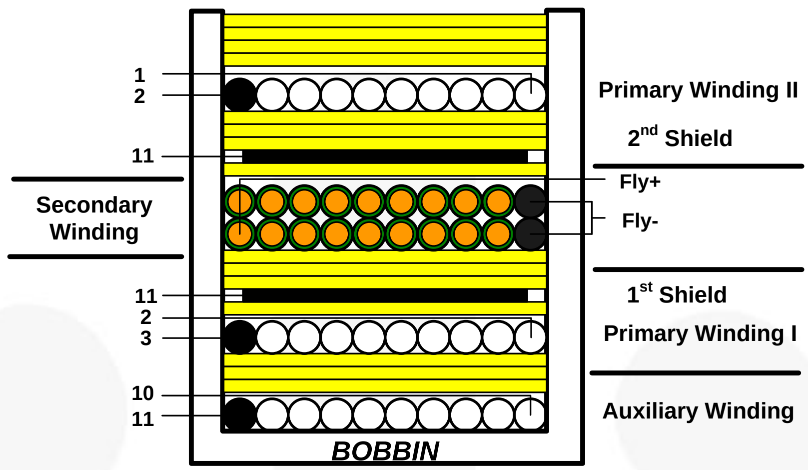

Figure 25. Transformer

NO	Terminal		Wire	Ts	Insulation
	S	F			Ts
N1	11	10	0.25 • 1	9	3
N2	3	2	0.25 • 1	33	1
	11		COPPER SHIELD	1.2	3.0
N3	Fly-	Fly+	0.5 • 2	12	1
	11		COPPER SHIELD	1.2	3.0
N4	2	1	0.25 • 1	33	4
			CORE ROUNDING TAPE		3

	Pin	Specification	Remark
Primary-Side Inductance	3—1	920 µH ±5%	100 kHz, 1 V
Primary-Side Effective Leakage	3—1	15 µH Maximum	Short One of the Secondary Windings

Physical Dimensions

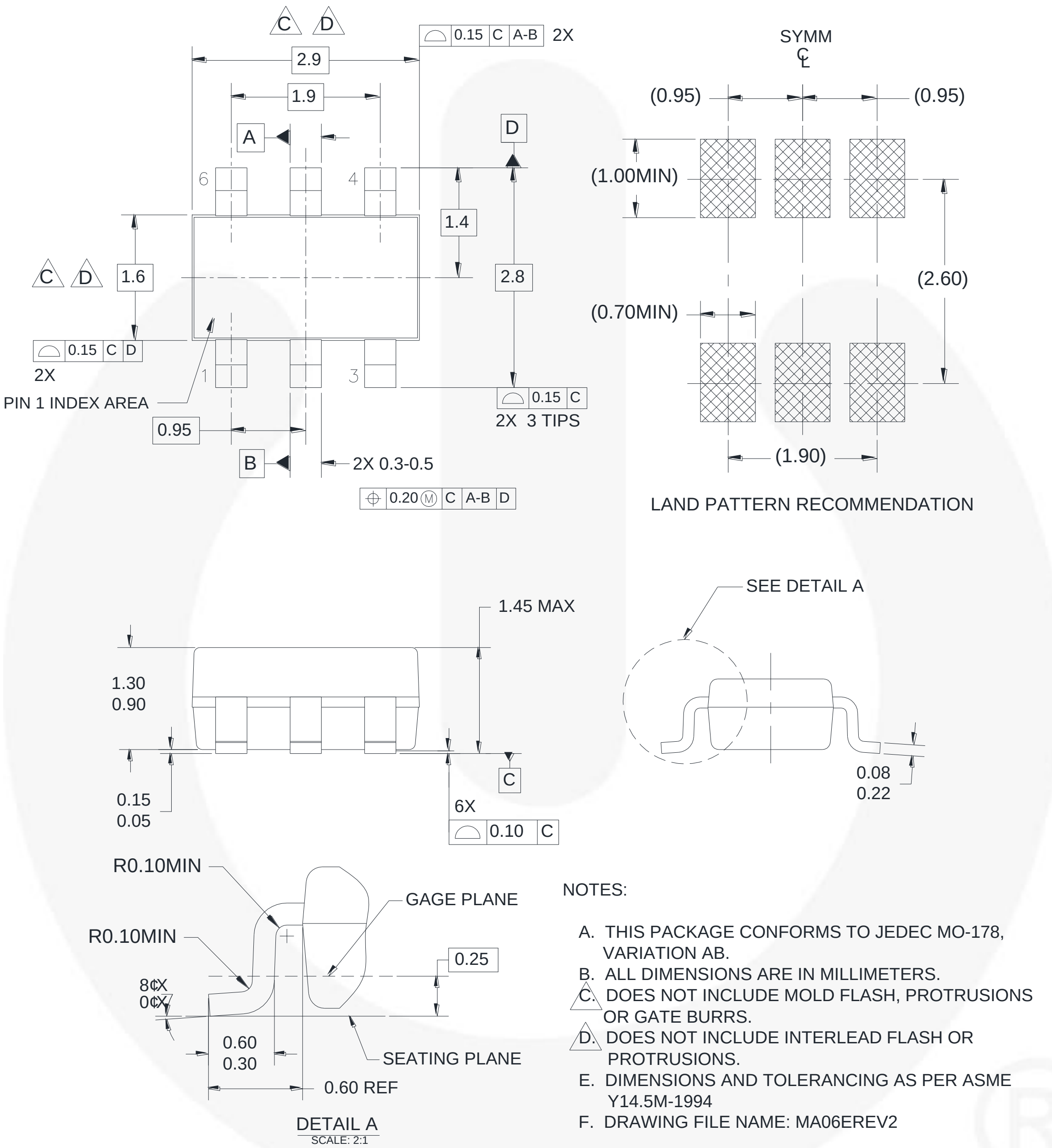

Figure 26. 6-Lead, SOT23, JEDEC MO-178 Variation AB, 1.6 mm Wide

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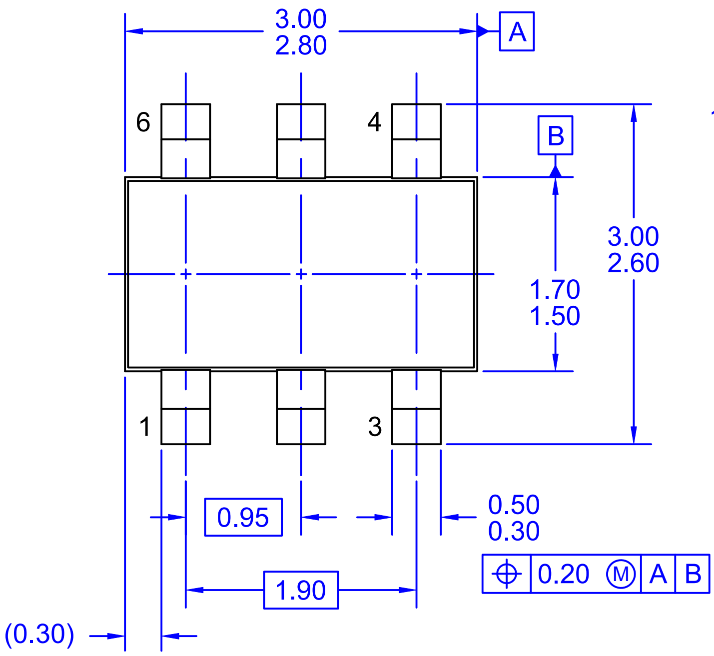
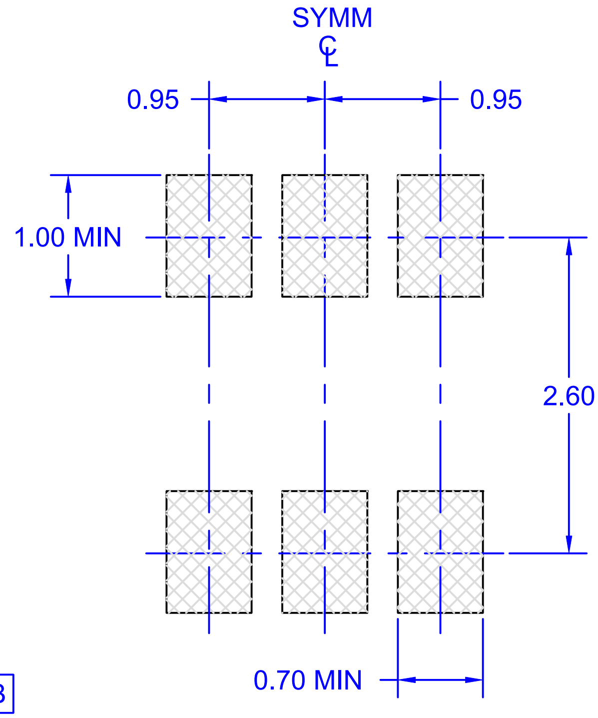
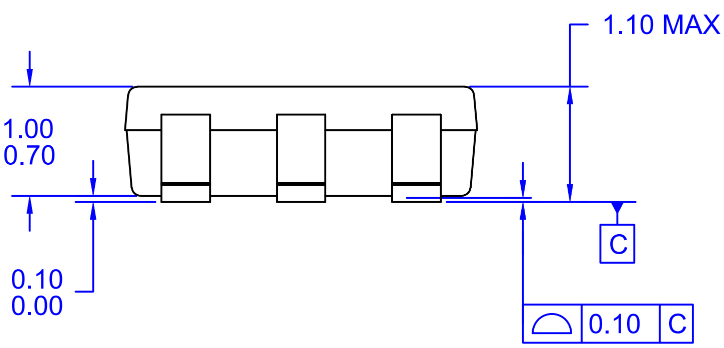
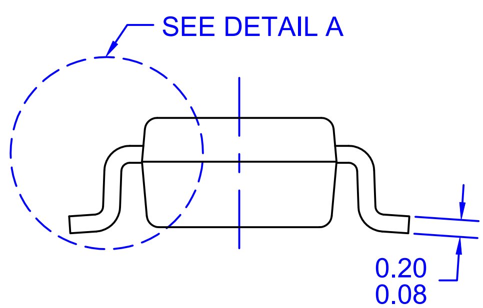
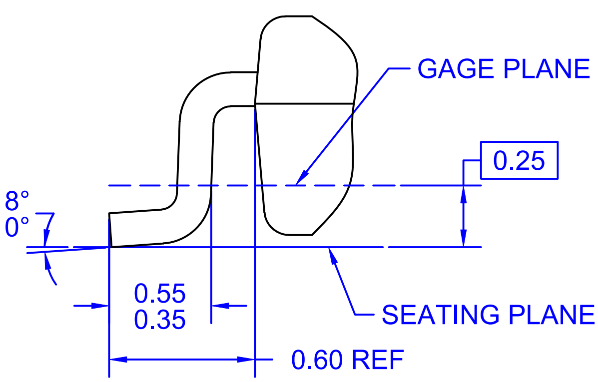




LAND PATTERN RECOMMENDATION







DETAIL A
SCALE: 50X

NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC MO-193. VAR. AA, ISSUE C, DATED JANUARY 2000.

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 2009.

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