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EPC9046

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Development Board
EPC9046
Quick Start Guide

Half Bridge with Gate Drive
for EPC2029

DESCRIPTION

This development board is in a half bridge topology with onboard gate drives, featuring the EPC2029 eGaN® field effect transistor (FET). The purpose of this development board is to simplify the evaluation process of these eGaN FETs by including all the critical components on a single board that can be easily connected into any existing converter.

The development board is 2" x 2" and contains two eGaN FETs in a half bridge configuration using the Texas Instruments LM5113 gate driver, supply and bypass capacitors. The board contains all critical components and layout for optimal switching performance and has additional area to add buck output filter components on the board. There are also various probe points to facilitate simple waveform measurement and efficiency calculation. A complete block diagram of the circuit is given in Figure 1.

For more information on the EPC2029 eGaN FET, please refer to the datasheets available from EPC at **www.epc-co.com**. The datasheet should be read in conjunction with this quick start guide.

Table 1: Performance Summary ($T_A = 25°C$)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{DD}	Gate Drive Input Supply Range		7	12	V
V_{IN}	Bus Input Voltage Range			64	V
V_{OUT}	Switch Node Output Voltage			80*	V
I_{OUT}	Switch Node Output Current			22*	A
V_{PWM}	PWM Logic Input Voltage Threshold	Input 'High' Input 'Low'	3.5 0	6 1.5	V V
	Minimum 'High' State Input Pulse Width	V_{PWM} rise and fall time < 10ns	50		ns
	Minimum 'Low' State Input Pulse Width	V_{PWM} rise and fall time < 10ns	100#		ns

*Assumes inductive load, maximum current depends on die temperature – actual maximum current with be subject to switching frequency, bus voltage and thermal cooling.
\# Limited by time needed to 'refresh' high side bootstrap supply voltage.

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EFFICIENT POWER CONVERSION

QUICK START PROCEDURE

The development boards are easy to set up to evaluate the performance of the eGaN FET. The board allows the on-board placement of buck output components. Refer to Figure 2 for proper connect and measurement setup and follow the procedure below:

1. With power off, connect the input power supply bus to +V_{IN} (J5, J6) and ground / return to –V_{IN} (J7, J8).

2. With power off, connect the switch node of the half bridge OUT (J3, J4) to your circuit as required.

3. With power off, connect the gate drive input to +V_{DD} (J1, Pin-1) and ground return to –V_{DD} (J1, Pin-2).

4. With power off, connect the input PWM control signal to PWM (J2, Pin-1) and ground return to any of the remaining J2 pins.

5. Turn on the gate drive supply – make sure the supply is between 7 V and 12 V range.

6. Turn on the bus voltage to the required value (do not exceed the absolute maximum voltage of 80 V on V_{OUT}

7. Turn on the controller / PWM input source and probe switching node to see switching operation.

8. Once operational, adjust the bus voltage and load PWM control within the operating range and observe the output switching behavior, efficiency and other parameters.

9. For shutdown, please follow steps in reverse.

NOTE. When measuring the high frequency content switch node (OUT), care must be taken to avoid long ground leads. Measure the switch node (OUT) by placing the oscilloscope probe tip through the large via on the switch node (designed for this purpose) and grounding the probe directly across the GND terminals provided. See Figure 3 for proper scope probe technique.
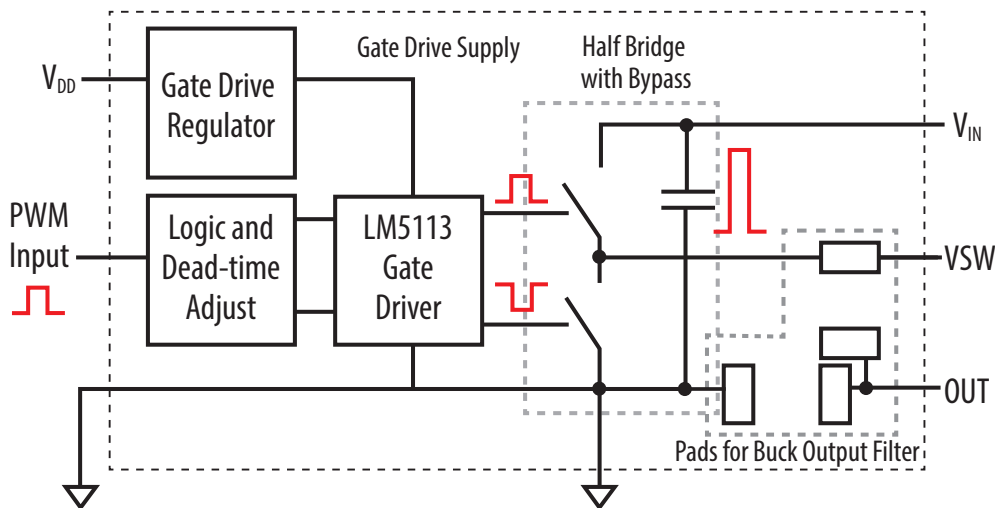

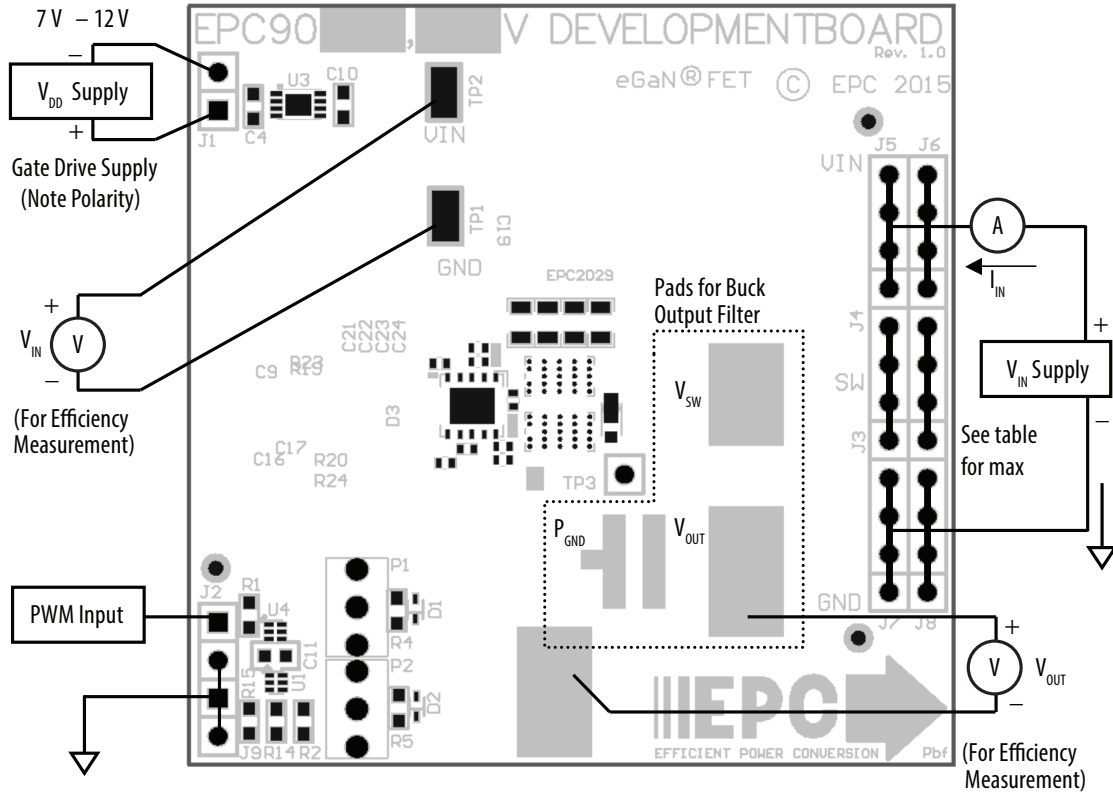Figure 1: Block Diagram of Development Board

QUICK START PROCEDURE

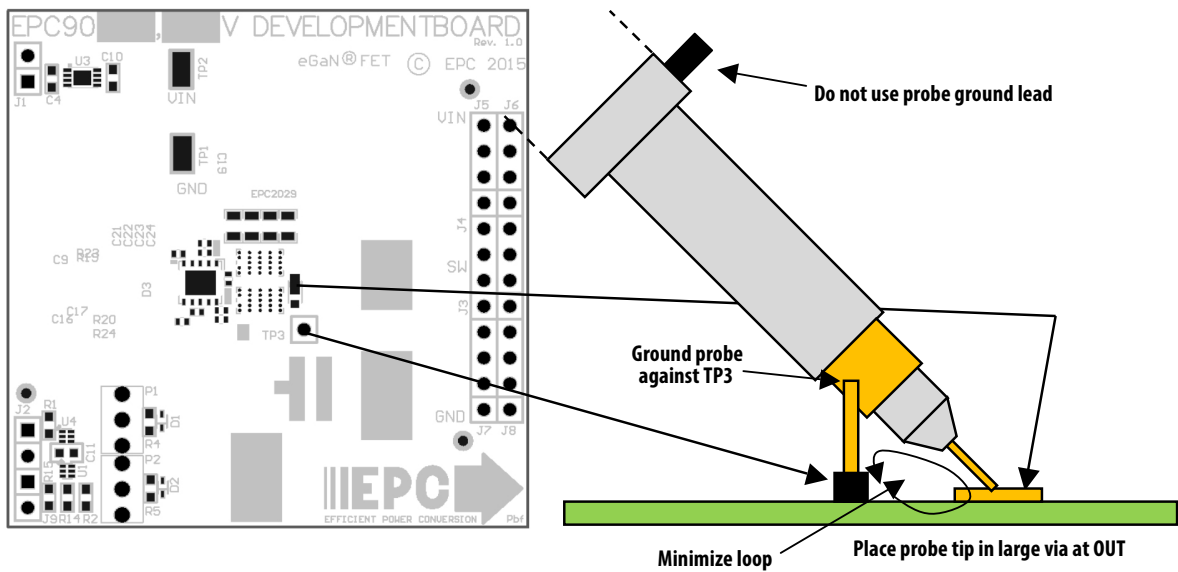Figure 2: Proper Connection and Measurement Setup
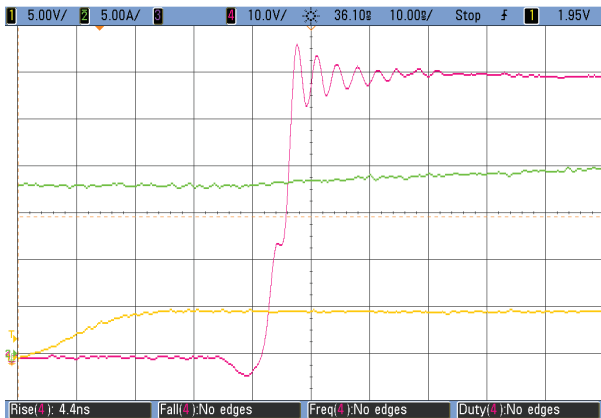

Figure 3: Proper Measurement of Switch Node – OUT

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Datasheet of EPC9046 - BOARD DEV FOR EPC2029 80V EGAN
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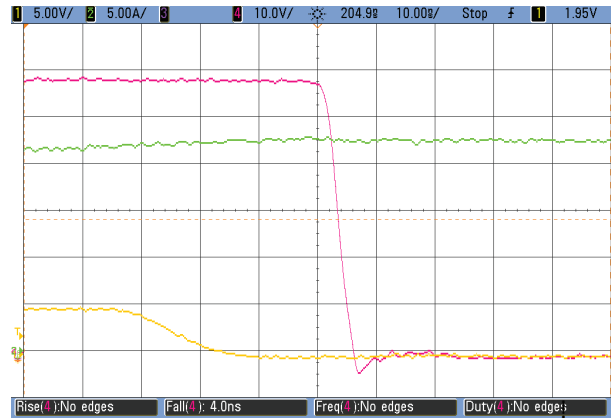| QUICK START GUIDE | EPC9046 |

THERMAL PERFORMANCE

Figure 4 (a) – Rising Edge

Figure 4 (b) – Falling Edge

Typical Waveforms for V_{IN} = 60 V to 5V/20 A (300 kHz) Buck converter CH1: (V_{PWM}) Input logic signal – CH2: (I_{OUT}) Output inductor current – CH4: (V_{OUT}) Switch node voltage

The EPC9046 development board showcases the EPC2029 eGaN FET. These development boards are intended for bench evaluation with low ambient temperature and convection cooling. The addition of heat-sinking and forced air cooling can significantly increase the current rating of these devices, but care must be taken to not exceed the absolute maximum die temperature of 150°C.

NOTE. The EPC9046 development board does not have any current or thermal protection on board.

Table 2: Bill of Materials

| Item	Qty	Reference	Part Description	Manufacturer / Part #
1	3	C4, C10, C11,	Capacitor, 1 µF, 10%, 25 V, X5R	Murata, GRM188R61E105KA12D
2	2	C16, C17	Capacitor, 100 pF, 5%, 50 V, NP0	Kemet, C0402C101K5GACTU
3	1	C9	Capacitor, 0.1 µF, 10%, 25 V, X5R	TDK, C1005X5R1E104K
4	1	C19	Capacitor, 1 µF, 10%, 25 V, X5R	C1005X5R1E105K
5	4	C21, C22, C23, C24	Capacitor, 1 µF, 10%, 100 V, X7R	TDK, CGA4J3X7S2A105K125AE
6	2	D1, D2	Schottky Diode, 30 V	Diodes Inc., SDM03U40-7
7	3	J1, J2, J9	Connector	FCI, 68001-236HLF
8	1	J3, J4, J5, J6, J7, J8	Connector	FCI, 68602-224HLF
9	2	Q1, Q2	eGaN® FET	EPC2029
10	1	R1	Resistor, 10.0 K, 5%, 1/10 W	Panasonic, ERJ-3GEY0R00V
11	2	R2, R15	Resistor, 0 Ohm, 1/8 W	Stackpole, RMCF0603ZT0R00
12	1	R4	Resistor, 47 Ohm, 1%, 1/10 W	Stackpole, RMFC0603FT47R0
13	1	R5	Resistor, 75 Ohm, 1%, 1.10 W	Stackpole, RMCF0603FT75R0
14	4	R19, R20, R23, R24	Resistor, 0 Ohm, 1/16 W	Stackpole, RMCF0402ZT0R00
15	2	TP1, TP2	Test Point	Keystone Elect, 5015
16	1	TP3	Connector	1/40th of Tyco, 4-103185-0
17	1	U1	I.C., Logic	Fairchild, NC7SZ00L6X
18	1	U2	I.C., Gate Driver	National, LM5113
19	1	U3	I.C., Regulator	Microchip, MCP1703T-5002E/MC
20	1	U4	I.C., Logic	Fairchild, NC7SZ08L6X
21	0	R14	Optional Resistor	
22	0	D3	Optional Diode	
23	0	P1, P2	Optional Potentiometer	
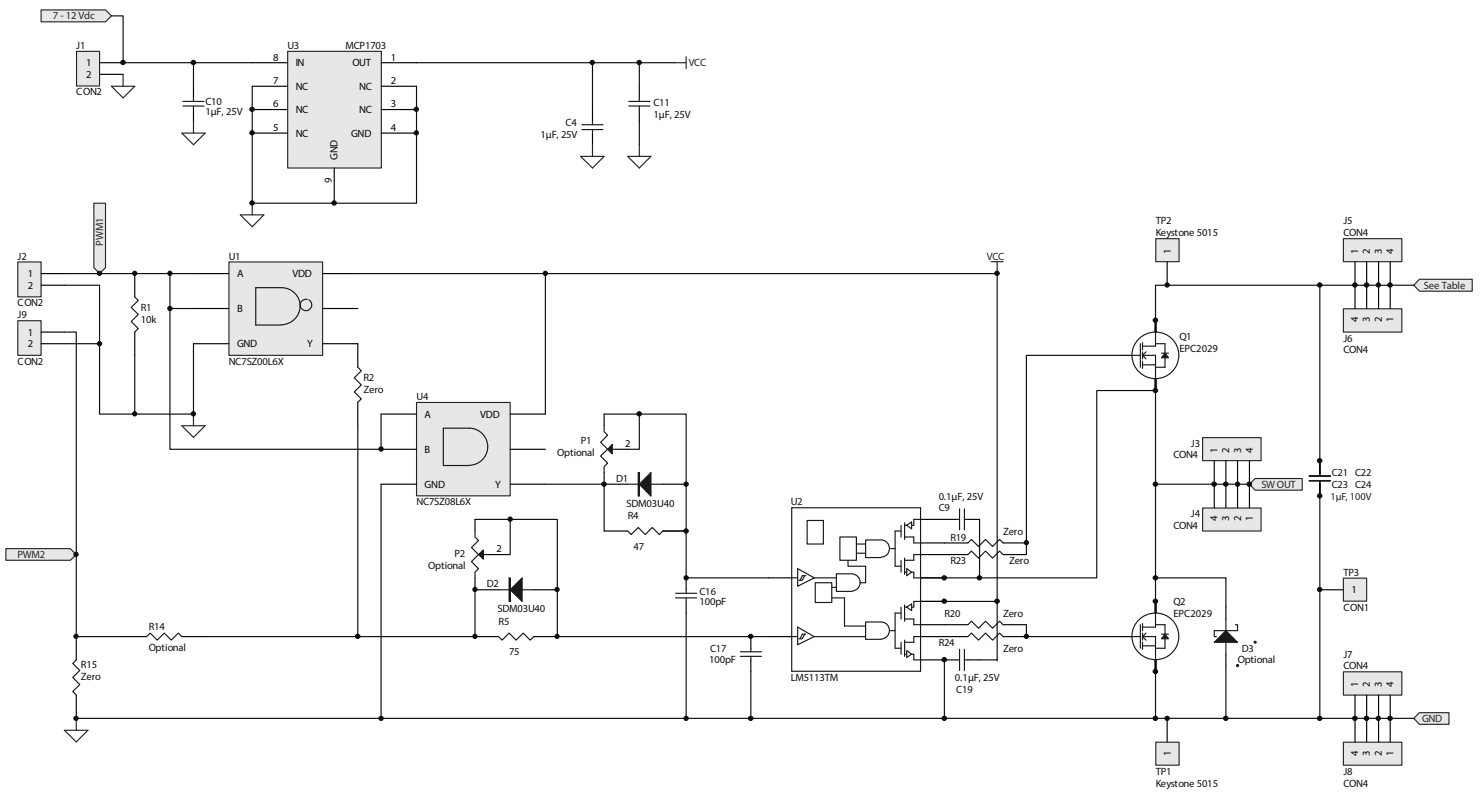
Figure 5: Development Board Schematic