



FDMS5361L_F085

N-Channel PowerTrench[®] MOSFET

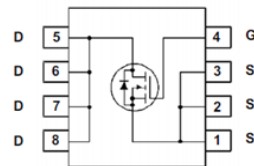
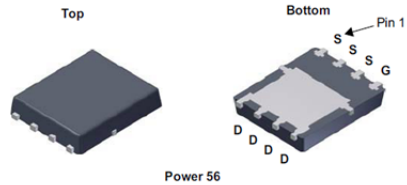
60 V, 35 A, 15 mΩ

Features

- Typ $r_{DS(on)}$ = 11.7 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 16.5\text{ A}$
- Typ $Q_{g(tot)}$ = 37 nC at $V_{GS} = 10\text{ V}$, $I_D = 16.5\text{ A}$
- UIS Capability
- RoHS Compliant
- Qualified to AEC Q101

Applications

- Automotive Engine Control
- Powertrain Management
- Solenoid and Motor Drivers
- Integrated Starter/Alternator
- Primary Switch for 12V Systems



For current package drawing, please refer to the Fairchild website at www.fairchildsemi.com/packaging

MOSFET Maximum Ratings $T_J = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	60	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current - Continuous ($V_{GS}=10$) (Note 1)	$T_C = 25^\circ\text{C}$	35
	Pulsed Drain Current	$T_C = 25^\circ\text{C}$	See Figure 4
E_{AS}	Single Pulse Avalanche Energy (Note 2)	82	mJ
P_D	Power Dissipation	75	W
	Derate above 25°C	0.5	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature	-55 to + 175	$^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.0	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient (Note 3)	50	$^\circ\text{C}/\text{W}$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS5361L	FDMS5361L_F085	Power 56	13"	12mm	3000 units

Notes:

- 1: Current is limited by junction temperature.
- 2: Starting $T_J = 25^\circ\text{C}$, $L = 0.21\text{ mH}$, $I_{AS} = 28\text{ A}$, $V_{DD} = 60\text{ V}$ during inductor charging and $V_{DD} = 0\text{ V}$ during time in avalanche.
- 3: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.

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Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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Off Characteristics

B_{VDSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	60	-	-	V
I_{DSS}	Drain to Source Leakage Current	$V_{DS} = 60\text{V}, T_J = 25^\circ\text{C}$	-	-	1	μA
		$V_{GS} = 0\text{V}, T_J = 175^\circ\text{C}(\text{Note } 4)$	-	-	1	mA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	1.0	1.84	3.0	V
$R_{DS(on)}$	Drain to Source On Resistance	$I_D = 16.5\text{A}, T_J = 25^\circ\text{C}$	-	11.7	15	$\text{m}\Omega$
		$V_{GS} = 10\text{V}, T_J = 175^\circ\text{C}(\text{Note } 4)$	-	24.5	30	$\text{m}\Omega$
		$I_D = 16.5\text{A}, T_J = 25^\circ\text{C}$	-	14.6	18	$\text{m}\Omega$
		$V_{GS} = 4.5\text{V}, T_J = 175^\circ\text{C}(\text{Note } 4)$	-	29.5	34	$\text{m}\Omega$

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	-	1980	-	pF
C_{oss}	Output Capacitance		-	176	-	pF
C_{riss}	Reverse Transfer Capacitance		-	93	-	pF
R_g	Gate Resistance	$f = 1\text{MHz}$	-	1.6	-	Ω
$Q_{g(ToT)}$	Total Gate Charge at 10V	$V_{GS} = 0 \text{ to } 10\text{V}$	-	37	44	nC
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0 \text{ to } 2\text{V}$				
Q_{gs}	Gate to Source Gate Charge	$V_{DD} = 30\text{V}, I_D = 16.5\text{A}$	-	5.5	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	7.3	-	nC

Switching Characteristics

t_{on}	Turn-On Time	$V_{DD} = 30\text{V}, I_D = 16.5\text{A}, V_{GS} = 10\text{V}, R_{GEN} = 6\Omega$	-	-	30	ns
$t_{d(on)}$	Turn-On Delay		-	16	-	ns
t_r	Rise Time		-	10	-	ns
$t_{d(off)}$	Turn-Off Delay		-	52	-	ns
t_f	Fall Time		-	8	-	ns
t_{off}	Turn-Off Time		-	-	67	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 16.5\text{A}, V_{GS} = 0\text{V}$	-	-	1.25	V
t_{rr}	Reverse Recovery Time	$I_F = 16.5\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	28	32	ns
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 48\text{V}$	-	25	33	nC

Note:

 4: The maximum value is specified by design at $T_J = 175^\circ\text{C}$. Product is not tested to this condition in production.

Typical Characteristics

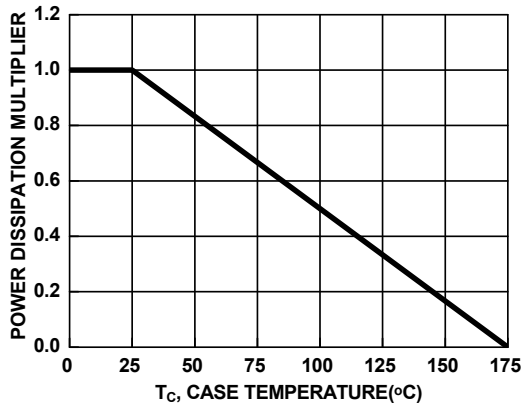


Figure 1. Normalized Power Dissipation vs. Case Temperature

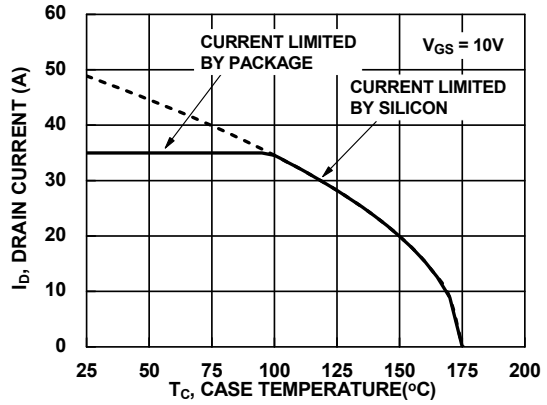


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

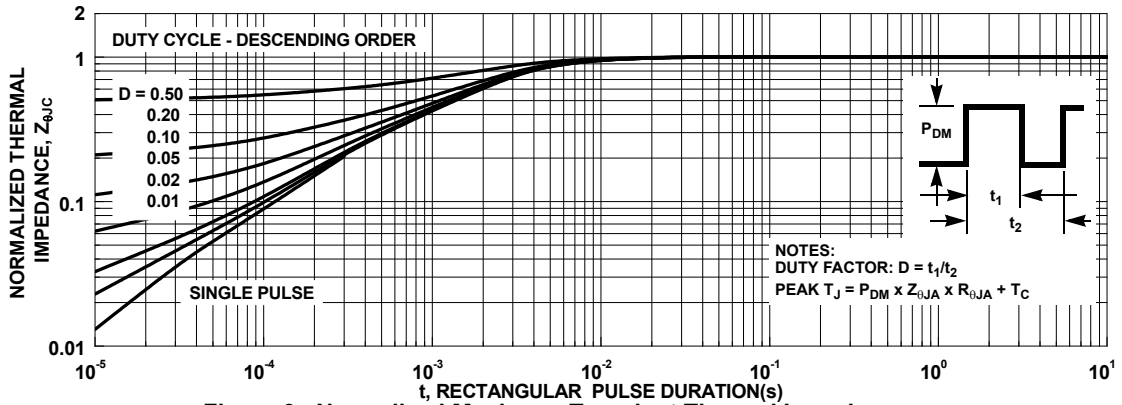


Figure 3. Normalized Maximum Transient Thermal Impedance

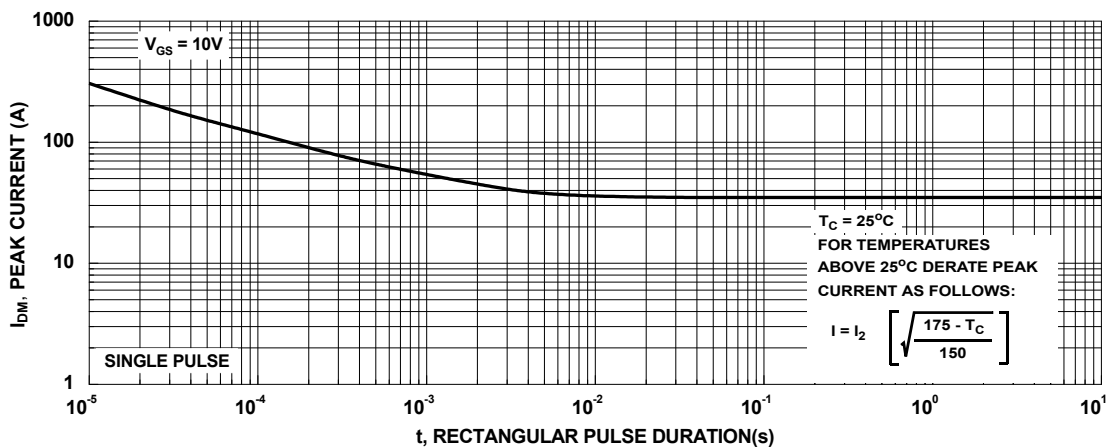


Figure 4. Peak Current Capability

Typical Characteristics

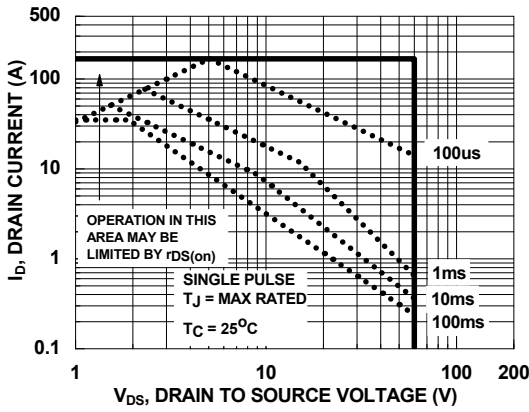
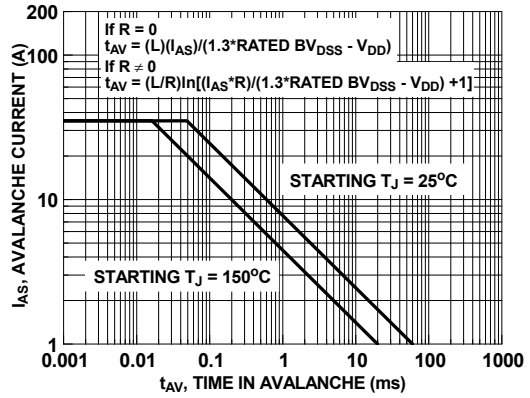


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515
 Figure 6. Unclamped Inductive Switching Capability

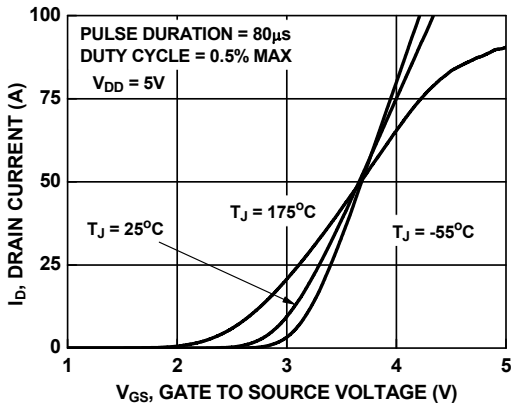


Figure 7. Transfer Characteristics

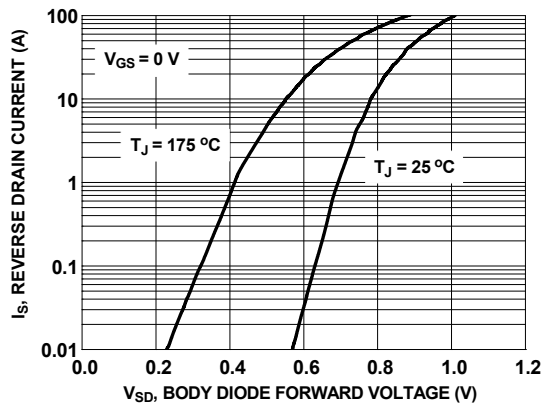


Figure 8. Forward Diode Characteristics

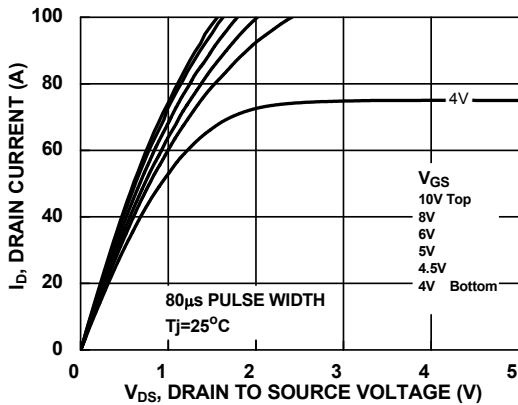


Figure 9. Saturation Characteristics

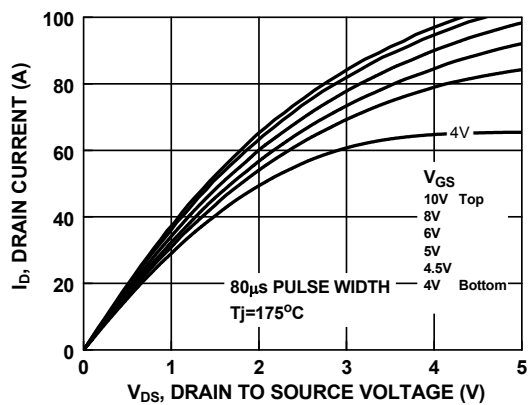


Figure 10. Saturation Characteristics

Typical Characteristics

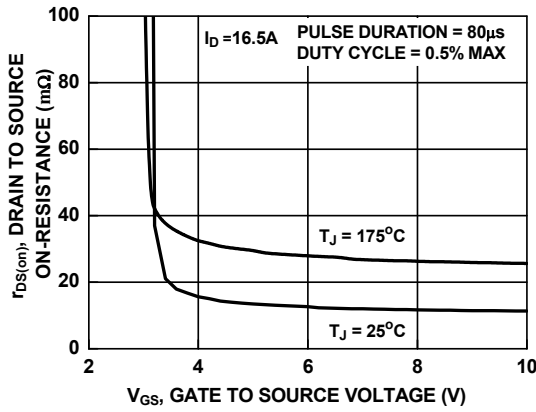


Figure 11. R_{dson} vs. Gate Voltage

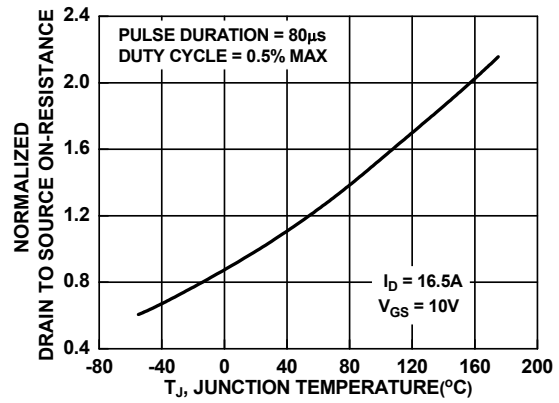


Figure 12. Normalized R_{dson} vs. Junction Temperature

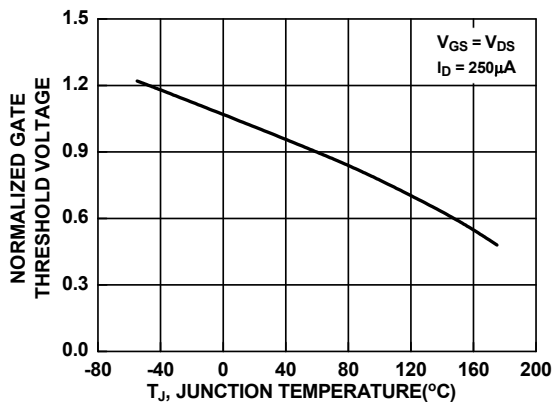


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

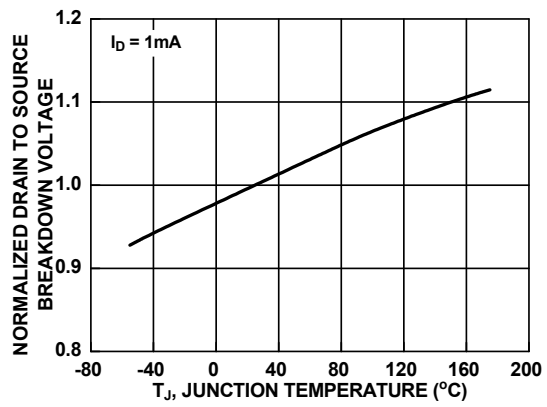


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

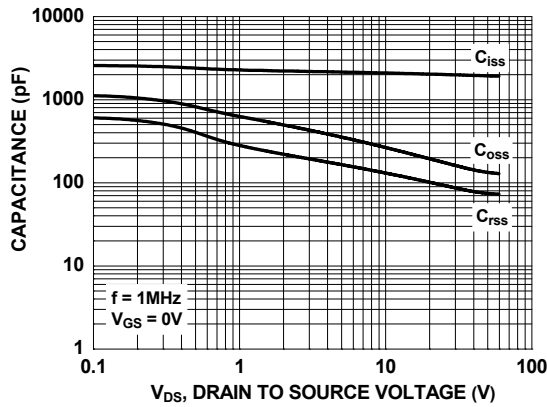


Figure 15. Capacitance vs. Drain to Source Voltage

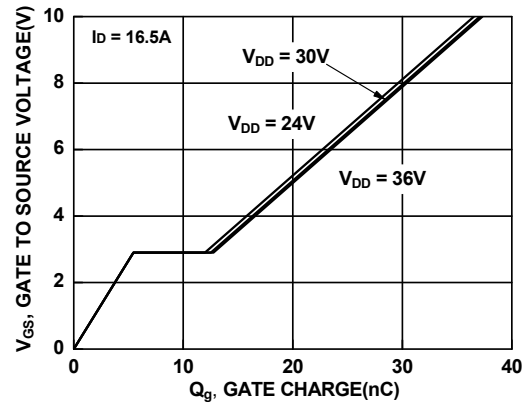
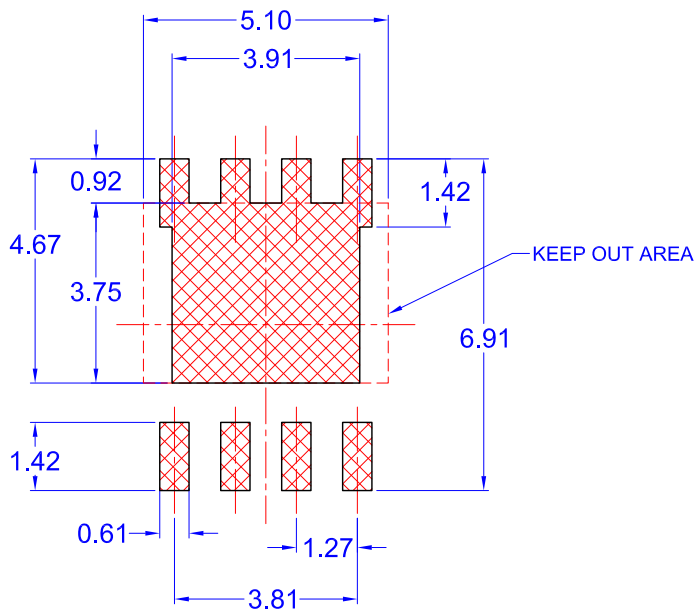
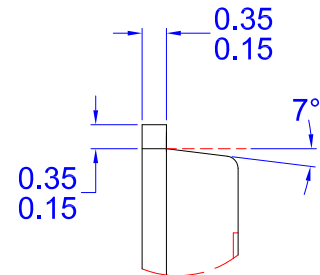
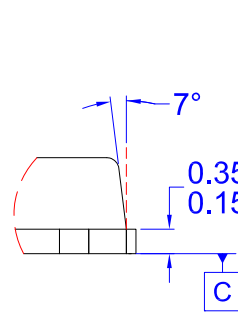
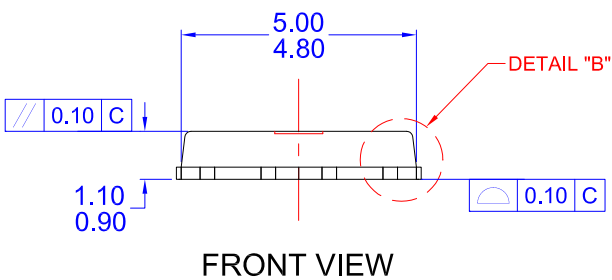
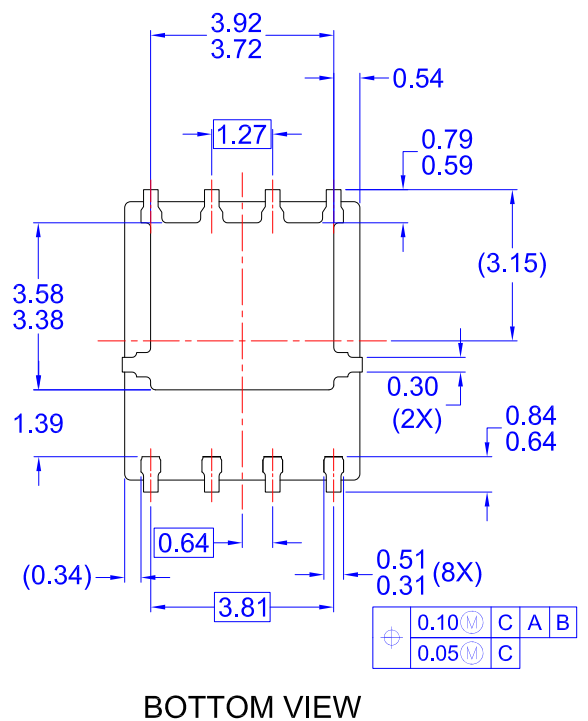
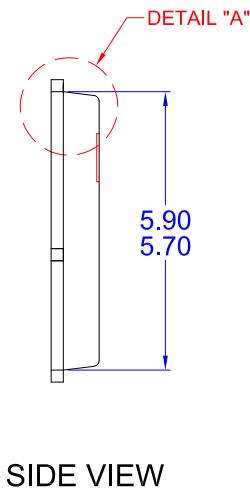
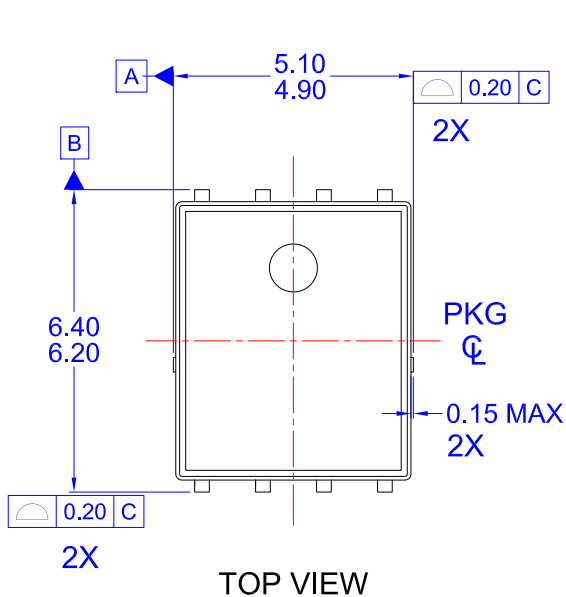


Figure 16. Gate Charge vs. Gate to Source Voltage



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) PACKAGE STANDARD REFERENCE: JEDEC REGISTRATION, MO-240, ISSUE B DATED 10/2009
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
 - D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
 - E) DRAWING FILE NAME: MKT-PQFN08MREV2





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