256M-BIT
3.0-VOLT PARALLEL FLASH MEMORY WITH PAGE MODE

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Preliminary Revision A

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1 GENERAL DESCRIPTION

The W29GL256S Parallel Flash memory provides a storage solution for embedded system applications that require better performance, lower power consumption and higher density. This product fabricated on 58 nm process technology. This device offers a fast page access time as fast as 15ns with a corresponding random access time as fast as 90ns. It features a Write Buffer that allows a maximum of 256 words (512 bytes) to be programmed in one operation, resulting in faster effective programming time than standard programming algorithms. The W29GL256S also offers special features such as Compatible Manufacturer ID that makes the device industry standard compatible without the need to change firmware.

2 FEATURES

- 58 nm Technology
- x16 data bus
- 256-WORD (512-byte) Programming Buffer
  - o Programming in Page multiples, up to a maximum of 512 bytes
- Asynchronous 32-byte Page Read
- Single word and multiple program on same word options
- Sector Erase
  - o Uniform 128-kbyte sectors
- Enhanced Sector Protection (ESP)
  - o Volatile and non-volatile protection methods for each sector
- Security Sector Region
  - o 1024-byte One Time Program (OTP) array divided into two 512-Byte lockable regions
- Suspend and Resume commands for Program and Erase operations
- Status Register, Data Polling, and Ready/Busy pin methods to determine device status
- CFI (Common Flash Interface) support
- Single supply (VCC) for read / program / erase (2.7V to 3.6V)
- Enhanced Variable I/O Feature
  - o Enhanced I/O voltage range (EVIO): 1.65V to VCC
- Industrial Temperature (-40°C to +85°C)
- More than 100,000 erase cycles for any sector typical
- 20-year data retention typical
- Packaging Options
  - o 56-pin TSOP, 14x20mm
  - o 56-ball TFBGA, 7x9mm
  - o 64-ball LFBGA, 13x11 mm

3 PIN CONFIGURATION

Figure 3-1 LFBGA64 TOP VIEW (Face Down)

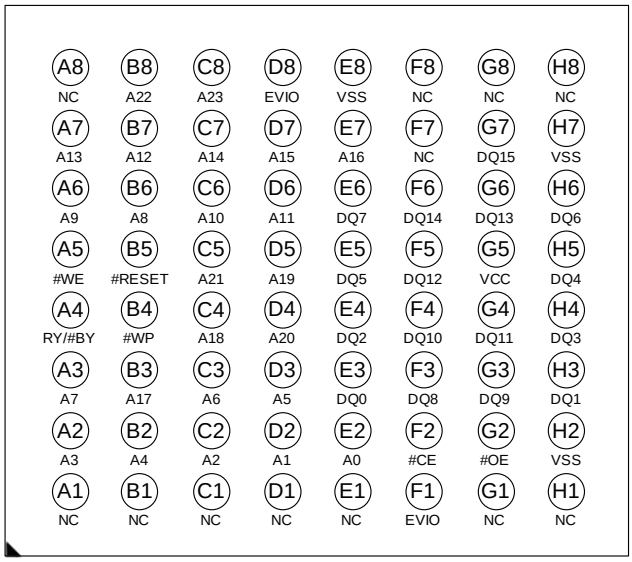


Figure 3-2 56-PIN STANDARD TSOP (Top View)

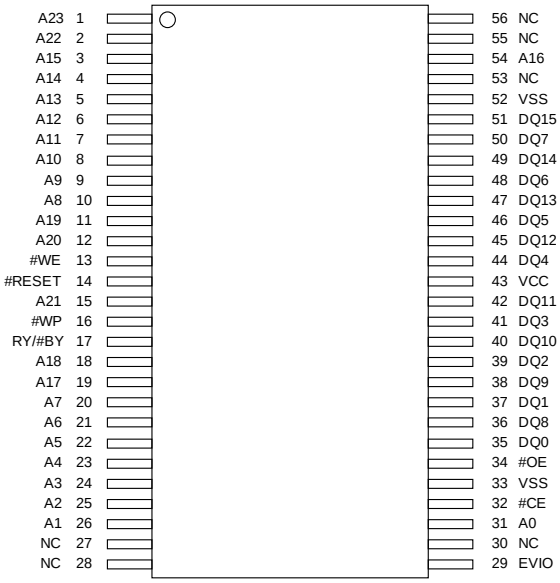
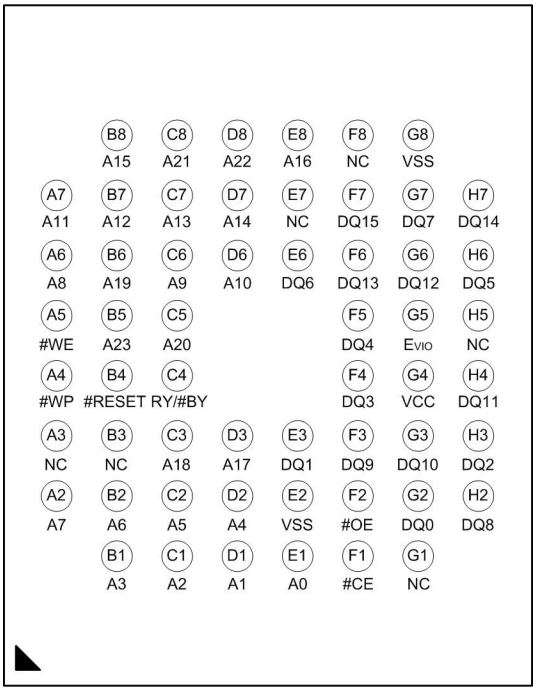
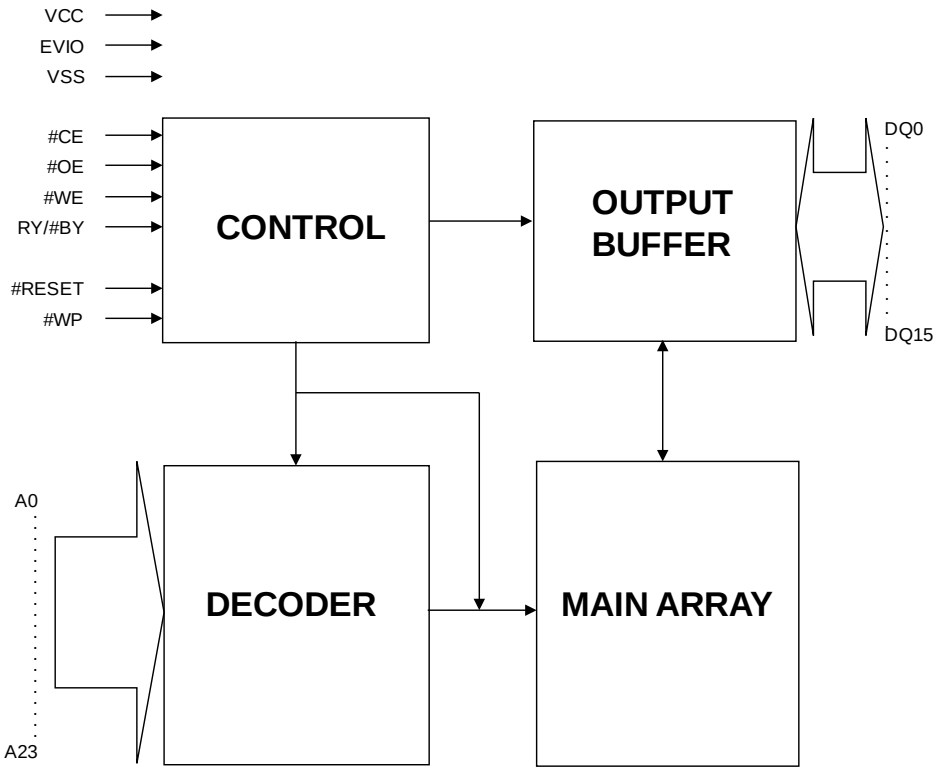


Figure 3-3 TFBGA56 TOP VIEW (Face Down)



4 BLOCK DIAGRAM

Figure 4-1 Simplified Block Diagram



5 PIN DESCRIPTION

Table 5-1 Pin Description

SYMBOL	SIGNAL TYPE	PIN NAME
A0-A23	Input	Address Inputs
DQ0-DQ15	I/O	Data Inputs/Outputs
#CE	Input	Chip Enable, Device selected at VIL
#OE	Input	Output Enable, Output at VIL and HIGH-Z at VIH
#WE	Input	Write Enable, Write Mode at VIL and Read Mode at VIH
#WP	Input	Hardware Write Protect, Highest & Lowest Sector Protect at VIL
#RESET	Input	Hardware Reset, device logic to standby and ready to read.
RY/#BY	Output	Ready/Busy Status, Indicates whether an Embedded Algorithm is in progress or complete. At VIL, the device is actively engaged in an Embedded Algorithm such as erasing or programming. At HIGH-Z, the device is ready for read or a new command write - requires external pull-up resistor to detect the HIGH-Z state. Multiple devices may have their RY/#BY outputs tied together to detect when all devices are ready.
VCC	Power Supply	Power Supply
EVIO	Power Supply	Enhanced Variable IO Supply
VSS	Power Supply	Ground
NC	-	No Connection

6 INTRODUCTION

The W29GL256S is a 3V, 256-Mbit, non-volatile, flash memory device with variable I/O. The device has a bus width of 16-bits (2-Bytes/1-Word) and word address boundaries are what are used. All read accesses provide 16 bits of data on every bus cycle. Every write cycle transfers 16 bits of data on the bus.

XIP and Data Storage flash memories are combined features of the W29GL256S. This enables the ability of fast programming speeds and reduced random access time of XIP flash in higher densities.

Read access to any random location takes 90 ns to 100 ns depending on device I/O power supply voltage. Each random access reads an aligned group of data of 32-bytes called a Page. Other words within the same Page may be read by changing only the low order 4 bits of word address. While in the same Page, access could take between 15 ns to 30 ns. This read operation is referred as Page Mode. Higher word address bits will select a different Page and begin another initial access. All read accesses are asynchronous.

The device control logic is divided into two parallel operating subsections, the Command State Machine (CSM) and the Write State Controller. Device level signals with the host system during read and write transfers are monitored by the CSM as needed for the inputs and drive outputs. CSM delivers data from the current entered address map on read operations; places write address and data information into the Write State Controller command memory; signals the Write State Controller of power level changes, write operations and hardware reset, The Write State Controller looks in the command memory, after a write operation, for correct command sequences and performs Internal Algorithms that are related.

Within the W29GL256S lie internal complex sequential operations or algorithms that are necessary to change the state of non-volatile data in the memory array. The internal Write State Controller manages all device algorithms. The main array data, programming and erasure are the main algorithms that are performed. When the host system sends command instructions to the flash device address space and Write State Controller receives these commands, provides status information during the progress of internal algorithms and performs all the necessary steps to complete the command.

A logical 1 bit is considered an erased cell. Changing a bit from a logical 1 to a logical 0 is considering programming. Note, only an erase operation is able to change a 0 to a 1. A restriction to an erase operation is a minimum of an entire sector (sector erase), which is a 128-kbyte aligned and length group of data is erased or the entire array can be erased (chip erase). Winbond ships the W29GL256S with all sectors erased.

The W29GL256S programming algorithm transfers volatile data from a write buffer to a non-volatile memory array line; this is called Write Buffer Programming. The size of the buffer is 256-Words (512-Bytes). 1 to 256 words can be written at any location in the Write Buffer prior to executing the programming operation. The programming operation can only be performed on an aligned group of 512 bytes in the flash array which is referred to as a Line.

After the completion of any Write Buffer operation or a reset, the buffer is refreshed to all 1's. By default any location that has not be written to a 0 are filled with 1's. Each page of data that was loaded into the Write Buffer during a programming operation, the memory array data is unaffected by 1's in the Write Buffer as it is transferred to a memory array Line.

Program and Erase operations may be affected by the Enhanced Sector Protection (ESP) methods, preventing any erasure or programming in a sector that may have been previously protected.

Table 6-1 W29GL256S Address Map

Addresses	Value	Description
A3 - A0	16	Word Selection
A7 - A0	256	Write Buffer Internal Address
A15 - A4	4096	Page Selection
A15 - A8	256	Write-Buffer-Line Selection
A23 - A16	256	Sector Selection

7 ARRAY ARCHITECTURE

There are several separate address spaces (i.e., Memory Map Overlay) that may appear within the address range of the flash memory device. Only one MMO can exist or be entered at a time.

- Main Memory Array
  - o This non-volatile area is used for storage of data that may be randomly accessed by asynchronous read operations.
- ID/CFI
- A Winbond factory programmed area for device characteristics information. It contains the Common Flash Interface (CFI) and Device Identification (ID) information tables.
- Security Sector Region (SSR)
- A Non-volatile / One Time Programmable (OTP) memory array used for Winbond factory and customer programmable permanent data.
- Lock Register
- This OTP non-volatile word is used to configure the Enhanced Sector Protection (ESP) features and lock the SSR.
- Individual Protection Bits (IPB):
- A non-volatile flash memory array with one bit for its associated sector. Programming this bit protects that sector from programming and erasure.
- IPB Lock
- Program and erase protection for the IPB bits. When the volatile register bit is enabled no programming or erasing of the IPB bits is prohibited.
- Dynamic Protection Bits (DPB)
- Similar to the IPB scheme, this volatile array with one bit for each sector can protect its associated sector from erasure and programming while the device is powered.
- Status Register
- Internal algorithm status monitoring can be done using this volatile register.
- Data Polling Status:
- Legacy software compatible volatile register used as an alternative to the Status Register to monitor internal algorithm status.

The Main Memory Array is the primary and default address space. This area at any time may be overlaid by one other address space. All the aforementioned address spaces are considered as a Memory Map Overlay (MMO). Each MMO replaces the entire address range of the main array. Addresses outside the current MMO address map are considered as not defined and are reserved for future use. Read access is possible outside of an MMO address map and will return non-valid (undefined) data.

What appears in the flash device address space at any given time is one of four address map modes:

- Read Mode
- Memory Map Overlay (MMO) Mode
- Status Register (SR) Mode
- Data Polling Mode

In Read Mode the entire Flash Memory Array may be directly read. Read mode is entered during Power Up, after a Hardware Reset, Command Reset completion, or when an internal algorithm is suspended, all of which is controlled by the Write State Controller. While in the Read Mode, command accesses are permitted when an internal algorithm is suspended. There are subsets of commands that will be accepted in Read Mode while an Internal Algorithm is suspended.

The Status Register read command can be issued in any mode. This execution will cause the MMO of the Status Register to appear in the device address space at every word address location. To do this, the device interface waits for a read access, ignoring any write access. The content of the Status Register is presented at the next read access, after which it exits the Status Register MMO, and returns to the previous mode in which the Status Register read command was received.

While the Write State Controller is performing an internal algorithm, such as a non-volatile memory array program or an erase operation, none of the Main Memory Array is accessible because, the entire flash device address space is replaced by the MMO of the Data Polling Status at every word location in the device address space.

While in an internal algorithm operation, only the Status Register Read command or a Program / Erase suspend command will be accepted, ignoring all other commands. Hence, no other MMO may be entered.

The Data Polling MMO is visible during an internal algorithm operation and once a suspend command has been executed it is present up to the moment the device suspends the internal algorithm. When the internal algorithm is suspended the Data Polling MMO is exited and the Main Memory Array data is available again. The Data Polling MMO is activated again when the suspended internal algorithm operation is resumed. At the completion of an internal algorithm operation, the Data Polling MMO is exited and the device goes back to operation from which it was called.

As mentioned previously, only one MMO may exist at any one time. Device commands affect only the currently entered MMO. Not all commands are valid for each MMO. For a listed of valid commands, see the *Command Definition Tables* in MMO sections of the table.

Some MMOs have non-volatile data that can be programmed

- Individual Protection Bits (IPB), also erase capable
- Lock Register
- Security Sector Region

Operating in a non-volatile MMO mode while performing a program or erase command, the MMO is not readable while the internal algorithms is active. As soon as the function has completed, the MMO mode remains active and is again readable. Suspend and Resume commands are ignored for these non-volatile modes while these internal algorithms are active.

7.1 Flash Main Memory Array

The W29GL256S family is comprised of uniform 128KB sector size architecture. The table below shows the sector architecture of the W29GL256S device.

Table 7-1 W29GL256S Sector and Memory Address Map

Sector	Sector Address A23-A16	Sector Size (KByte)	X16 Start / Finish	
SA00	0000000	128	0000000h	000FFFFh
SA01	0000001	128	0010000h	001FFFFh
. . .	. . .	. . .	. . .	. . .
SA254	11111110	128	0FE0000h	0FEFFFFh
SA255	11111111	128	0FF0000h	0FFFFFFh

Note: This table has been reduced to show relative sector information for the entire device's individual sectors and their address ranges (sectors SA02-SA253 are not shown).

7.2 CFI and Device ID (CFI-ID)

There are two methods for systems to identify the type of flash memory installed in the system. The first method is called the Common Flash Interface (CFI). The second method called Autoselect, which is now referred to as Device Identification (ID).

Device Identification (ID), a command is used to enable a Memory Map Overlay where up to 16 word locations can be read to get JEDEC manufacturer identification (ID), device ID, and some configuration and protection status information from the flash memory.

The Common Flash Interface (CFI) command enables a Memory Map Overlay where a table of standard information about how the flash memory is organized and operates can be read.

Typically, these two address spaces have used separate commands and had separate overlays and are non-overlapping, so they actually can be combined in a single overlay. Either of these two commands can be used to access the combined Autoselect (ID) and CFI overlay.

The CFI-ID address map overlays the Flash Array data of the sector selected by the address used in the CFI-ID enter command. While the CFI-ID MMO is entered, the content of all other sectors is undefined. Address map starts at location 0 of the selected sector. Data is considered as undefined past the maximum defined address of the CFI-ID MMO to the maximum address of the selected sector.

To enter the Manufacturer ID (Autoselect) and Common Flash Interface (CFI) MMO command modes see the *Instruction Definition Table*.

Table 7-2 CFI-ID Address Map Overview

Word Address	Description	Read / Write
(SA) + 0000h to 000Fh	Device ID (traditional Autoselect values)	Read Only
(SA) + 0010h to 0079h	CFI data structure	Read Only
(SA) + 0080h to FFFFh	Undefined	Read Only

For the complete address map see the *Device ID and Common Interface Tables.*

7.3 Status Register

The Status Register, Memory Map Overlay (MMO) contains status for Internal Algorithms in a single volatile word format. When the read command for the Status Register is issued, status at the time of captured is presented in the register and the MMO is entered. All word locations in the device address space contain the Status Register information. Status Register exits the MMO mode after the first read access and returns to the address space map in use when the Status Register read command was issued.

7.4 Data Polling Status

The Data Polling Status, Memory Map Overlay (MMO) monitors the progress of Internal Algorithms which is contained in a single volatile word. Following the last write cycle of any command sequence that initiates an Internal Algorithms, the Data Polling Status will be entered. Internal Algorithms are initiated by one of the following commands:

- Blank Check
- Chip Erase
- Sector Erase
- Erase Resume / Program Resume
- Word Program
- Program Buffer to Flash
- Program Resume Enhanced Method
- Lock Register Program
- IPB Program
- All IPB Erase

At all word locations in the device address space, the Data Polling Status word appears. Data Polling Status MMO is exited and the device address space returns to the address map mode where the Internal Algorithms was started at the completion of the Internal Algorithms.

7.5 Sector Protection Control

7.5.1 Lock Register

The Lock Register, Memory Map Overlay (MMO) mode contains a single word of One Time Programmable (OTP) memory. When the MMO mode is entered the Lock Register appears at all word locations in the device address space. Winbond recommends for future compatibility to read or program the Lock Register only at location 0 of the device address space.

7.5.2 Individual Protection Bits (IPB)

The IPB, Memory Map Overlay (MMO) mode contains a non-volatile bit in each sector in the device. When the mode is entered, the IPB bit for a chosen sector appears in the Least Significant Bit (LSB) of each word in that sector. The non-volatile protection status for that sector is displayed by reading any word location, where the LSB indicates whether or not the sector is protected. The sector is protected against programming and erase operations if the bit is has been programmed to a 0. The sector is not protected by the IPB if the bit has been erased to a 1. Note; there are other features of the Enhanced Sector Protection (ESP) that can protect sectors. Winbond recommends for future compatibility, to read or program the IPB only at word location 0 of the sector.

7.5.3 IPB Lock

The IPB Lock, Memory Map Overlay (MMO) contains a single volatile bit of memory. Programming or erasing of the IPB is controlled by IPB Lock. IPB is protected against programming and erase operations, if the bit is 0. The IPB is not protected, if the bit is 1. When the IPB Lock mode is entered, the IPB Lock bit appears in the Least Significant Bit (LSB) of each word in the device address space. Winbond recommends for future compatibility, to read or program the IPB Lock only at word location 0 of the device.

7.5.4 Dynamic Protection Bits (DPB)

The DPB Memory Map Overlay (MMO) contains one volatile bit of memory for each Sector. The DPB bit for a sector appears in the Least Significant Bit (LSB) of each word in the sector after entering the DPB mode. Reading any word in a sector displays the protection status for that sector. Sectors are protected during program and erase operations, if the DPB is 0 and unprotected if the bit is 1. Note there are other features of ESP that can protect the sector. Winbond recommends for future compatibility to read, set, or clear the DPB only at word location 0 of the sector.

8 FUNCTIONAL DESCRIPTIONS

8.1 Read

8.1.1 Random Read

The memory device is selected by driving Chip Enable (#CE) LOW and the device will leave the Standby mode. If Write Enable (#WE) is disabled, driven HIGH while #CE is LOW, a random read operation is started. The particular data output will depends on the MMO mode and the specific address provided.

The data output is presented on DQ15-DQ0 when #CE is LOW, Output Enable (#OE) is LOW, #WE is HIGH, address is stable, and the asynchronous access times are met. The Address access time (t_{ACC}) is defined to be equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is defined as the delay from a stable #CE to valid data on the outputs. The #OE signal must be LOW for at least the period of the output enable time (t_{OE}), before valid read data is available at the outputs.

Device outputs will provide valid read data from the currently active address map mode at the end of the random read access time from address stable (t_{ACC}), #OE active (t_{OE}), or #CE active (t_{CE}), whichever happens last.

A list of other transitional states during Random Read operation;

- A new random read access begins if #CE remains LOW and any Address[23:4] signals change to a new value.
- In order to get Back to Back accesses, requires an address change to initiate the second access and #CE to remains LOW between accesses Read mode with Outputs Disable, If #CE remains LOW and #OE goes .
- Write mode, if #CE remains LOW, #OE goes HIGH, and #WE goes LOW.
- Standby mode, if #CE returns HIGH.

8.1.2 Page Read

As in the Random Read mode, a random read access sequence is required. Then if #CE remains LOW, #OE remains LOW, Address[23:4] signals remains unchanged, and any of the Address[3:0] signals have change, then a new access within the same Page (32-byte) begins with data appearing on DQ15-DQ0. The Page Read is much faster (t_{PACC}) than a Random Read access. If #CE goes HIGH and returns LOW for another access, a random read access is performed and time is required (t_{ACC} or t_{CE}).

8.2 Device Reset Operations

The Hardware Reset (#RESET) input pin provides a hardware method of resetting the device to a standby mode. Immediately after issuing a Hardware Reset, driving #RESET LOW for at least a period of t_{RP}:

- Any operations in progress are terminated,
- Memory Map Overlays (MMO) is exited.
- All outputs are set to HIGH-Z.
- The Status Register is reset.
- The Write State Controller goes to the standby mode.
- #CE is ignored for a period of (tRPH), during the reset operation.
- #CE must be held HIGH to meet the Reset current specification (I_{CC5}).

Note: An operation that was interrupted should be reinitiated to ensure data integrity. An operation command sequence should be executed once the device is ready.

8.3 Standby Mode

Standby is the default, minimum power condition while the device is not selected (#CE = HIGH). All inputs are ignored in this mode and all outputs, except RY/#BY are at HIGH-Z. The Write State Controller direct output of the RY/#BY determines its state and is not controlled by other devices or interfaces.

8.4 Automatic Sleep

When addresses remain stable for t_{ACC} + 30 ns, the device will automatically enter the Auto Sleep mode and latches the output data. Data on the output pins depends on the level of the #OE signal. The automatic sleep mode is designed to reduce device interface current (I_{CC6}). #OE signal levels are independent of the automatic sleep mode current. The device will remain at the Automatic Sleep current for a period of t_{ASSB}, at which time the device will transition to the standby current level. The automatic sleep mode current (I_{CC6}) specifications can be found in the *DC Characteristics Tables*.

It's important to note that slow clock durations help reduce current consumption when the Automatic Sleep mode goes active. During slow clock periods, read and write cycles may extend many times their length versus when the clock is operating at high speed. Even when the chip enable is LOW throughout these extended data transfer cycles, the memory device Command State Machine (CSM) will enter the Automatic Sleep mode and will remain in the Automatic Sleep until the t_{ASSB} parameter is met at which time the device will go into the standby mode. This keeps the device in the Automatic Sleep or standby power level for most of the extended duration of the data transfer cycles. Obviously this method is beneficial rather than consuming full read power all the time that the device is selected.

Note, the Write State Controller operates independent of the automatic sleep mode of the Command State Machine (CSM) and will continue to draw current during an active Internal Algorithm. Only when both entities are in their standby modes is the standby level current minimized.

8.5 Output Disable Mode

When the #CE signal is driven LOW, either a controlled read or write data transfer may begin. When there is a period at the start of a data transfer when Chip Enable is LOW, Address has become valid, #WE is HIGH and Output Enable (#OE) is HIGH. During this point a Random Read process is started while the data outputs remain at HIGH-Z (Output Disabled). Driving the #OE signal LOW, the device interface transitions to the Random Read mode and output data is actively driven. If in the event the Write Enable (#WE) signal is driven LOW, the device interface transitions to the Write mode. The host system interface should never drive #OE and #WE LOW at the same time; this will prevent conflicts with the device.

8.6 Program Methods

8.6.1 Asynchronous Write

When #WE goes LOW after CE is LOW, there is a transition from one of the read modes to the Write mode. If #WE is LOW before #CE goes LOW, there is a transition from the Standby mode directly to the Write mode without beginning a read access. At this point setting Output Enable (#OE) HIGH will start a write data transfer.

Address is captured by the falling edge of #WE or #CE, whichever occurs last. Data is captured by the rising edge of #WE or #CE, whichever occurs first.

A #WE controlled Write access is when the #CE goes LOW before #WE goes LOW and stays LOW after #WE goes HIGH. When #WE are HIGH and #CE goes HIGH, there is a transition to the Standby mode. If #CE remains LOW and #WE goes HIGH, there is a transition to the Read with Output Disable state.

A #CE controlled write mode is when #WE is LOW before #CE goes LOW, the write transfer is started by #CE going LOW. Then if #WE goes LOW after #CE goes HIGH, the address and data is latch by the rising edge of #CE.

Another #CE controlled write mode access is when #WE is LOW before #CE goes LOW and remains LOW after #CE goes HIGH. This is a #CE controlled Write transitions to the Standby mode.

An address change is required to initiate a Read access following a Write access, if #CE remains LOW between accesses.

An address change is required to initiate the second write access in a Back to Back write in which #CE remains LOW between accesses.

The Write State Controller command memory array is not readable by the host system and has no MMO. Its purpose is to examine the address and data in each write transfer to determine if the write is a legal command sequence. If the command sequence is correct, the Write State Controller will initiate the appropriate Internal Algorithms.

8.6.2 Word Programming

Word programming programs a single word anywhere in the Main Memory Array.

The Word Programming command is a four write cycle sequence. This is done by writing the unlock write command in the first two cycles, a program set up command in the third cycle and finally, in the fourth cycle the program address and data are written. This will initiate the Internal Word Program algorithm. No further input controls are required. The Internal Algorithm generates all the programming pulses and programmed cell verifications. When the Internal Word Program algorithm is complete, the Write State Controller then returns to its standby mode.

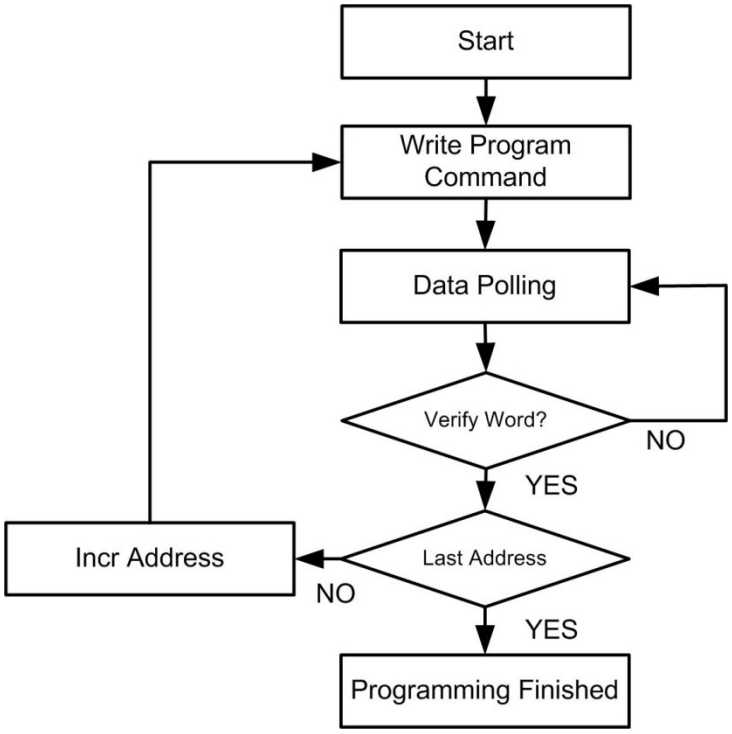
Program operation status can be determined by monitoring the RY/#BY output, reading the Status Register, or by using Data Polling Status.

Program Suspend is the only command that can be written to the device during the Internal Program Algorithm, all others are ignored. However, a hardware reset (#RESET = V_{IL}) will immediately terminates the programming operation. Then after t_{RPH} time, returns the device to read mode. It is recommended to reinitiate the Word Program command sequence after the device has completed the hardware reset operation to insure data integrity.

The Security Sector Region (SSR) mode may also use the Word Programming command when is entered.

The Word Programming command has a modified version without unlock write cycles when it is used for programming the Lock Register and IPB MMOs. The same command is also used to change volatile bits when entered in to the IPB Lock, and DPB MMOs. See the *Instruction Definition Tables* for program command sequences.

Figure 8-1 Word Program Operation



8.6.3 Write Buffer Programming

A 512-byte address range write buffer is used to program data within an aligned 512-byte boundary Line, (example, addresses: 100h to 1FFh). Hence, a Write Buffer Programming operation must be setup on a Line boundary. If the Programming operation is less than 512-bytes, it may start on any word boundary, but may not cross a Write-Buffer-Line boundary. All bit locations in the buffer at the start of a Write Buffer programming operation are in the One's state (FFFFh/Word). Thus, any locations not loaded will retain the existing data.

The Main Memory Array and the Secure Sector Region (SSR) are the areas that are supported by the Write Buffer Programming operation. It is possible to program from 1 bit, up to 512 bytes in one Write Buffer Programming operation. The recommended write buffer method is to only write each page once in a multi-page scenario. Programming should be done in full Lines of 512 bytes setup on 512-byte boundaries, for the very best performance.

To initiate a Write Buffer Programming operation, the first 2 cycles are the unlock write commands. The 3rd write cycle contains the Write to Buffer command with the program targeted Sector Address (SA). The fourth cycle is to write the number of planned word locations minus 1. This will indicate the number of write buffer addresses that are to be loaded with data. This also indicates when to expect the Program Buffer to flash confirm command. The Write to Buffer command and the Write Word Count command Sector Addresses must match. In order to program, the sector must be unlocked (unprotected).

Cycle 5, the starting address / data combination is written. This will be the first address / data pair to be programmed, and selects the write-buffer-Line address. The operation will abort and return to the initiating state if the Sector Address does not match the Write to Buffer Sector Address. In the following cycles, each address / data pairs must be in sequential order and all write buffer addresses must be within the same Line, otherwise the operation will abort and return to the initiating state.

For each data write operation, the WC counter will decrement and every write is data being loaded into the write buffer. During the write buffer loading period no commands are accepted. The only way to stop writing data to the write buffer is to abort the Write to Buffer command. This is done by writing an invalid address that is outside the Write Buffer Line of the programming operation.

The Program Buffer to Flash command must be issued immediately after the specified number of write buffer locations has been loaded at the sector address. At this point the program algorithm starts and the device status will be busy. The Internal Program Algorithm will program and verifies the data that has been programmed into the selected sector of the Main Memory Array. No control signals or timing parameters during this internal operation is required. The operation will abort and return to the initiating state anytime an incorrect number of write buffer locations have been loaded. The abort occurs because anything other than the expect Program Buffer to Flash command happened at the end of the word count.

The write-buffer internal programming operation can be suspended using the Program Suspend command. When the Internal Program Algorithm is complete, the Write State Controller then returns to the Write State Controller standby mode where the programming operation was started.

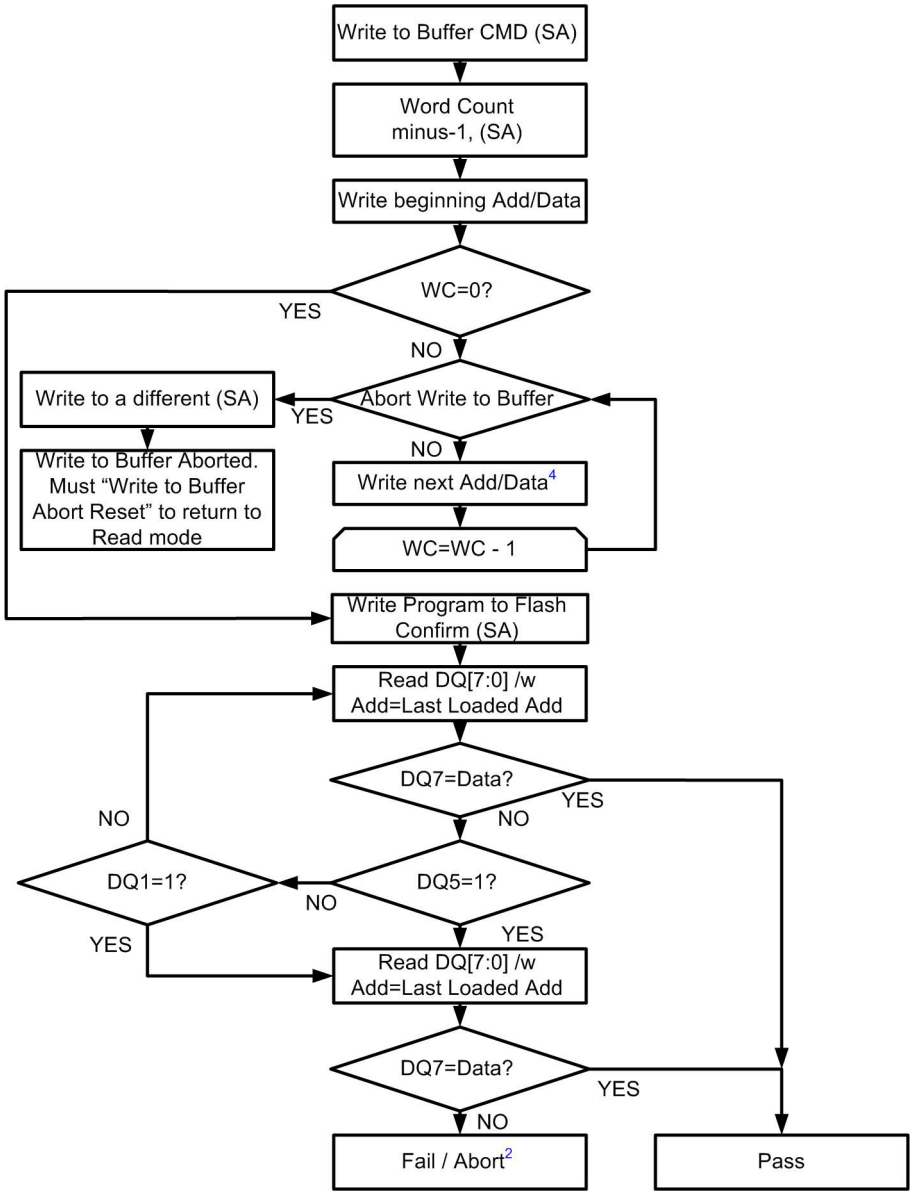
Under the following conditions the Write Buffer Programming sequence will be aborted:

- The Word Count cannot exceed a value greater than the buffer size, which is 255 (256 minus 1).
- The Write to Buffer command cannot contain an address that is outside the Line.
- After the Write Word Count number of data words is loaded the Program Buffer to Flash command is not issued

Data Polling Status, reading the Status Register, or monitoring the RY/#BY output can determine the status of the program operation. An abort of the Write Buffer command will occur immediately after an invalid condition, and will indicate a Program Fail in the Status Register at Program Status Bit (Bit 4=1), because of the Write Buffer Abort Status Bit (Bit 3) equals 1. A Clear Status Register command may be issued to clear the Program Status Bit or the next successful program operation will clear the failure status bit.

Caution should be taken when stopping the Write Buffer Programming Sequence by the following methods: Power cycling the device or a Hardware Reset. Using either of these methods may leave the area being programmed in an unknown state with unstable or invalid data. If this is the case reprogrammed with the same data or performing an erased to ensure data values are properly programmed or erased.

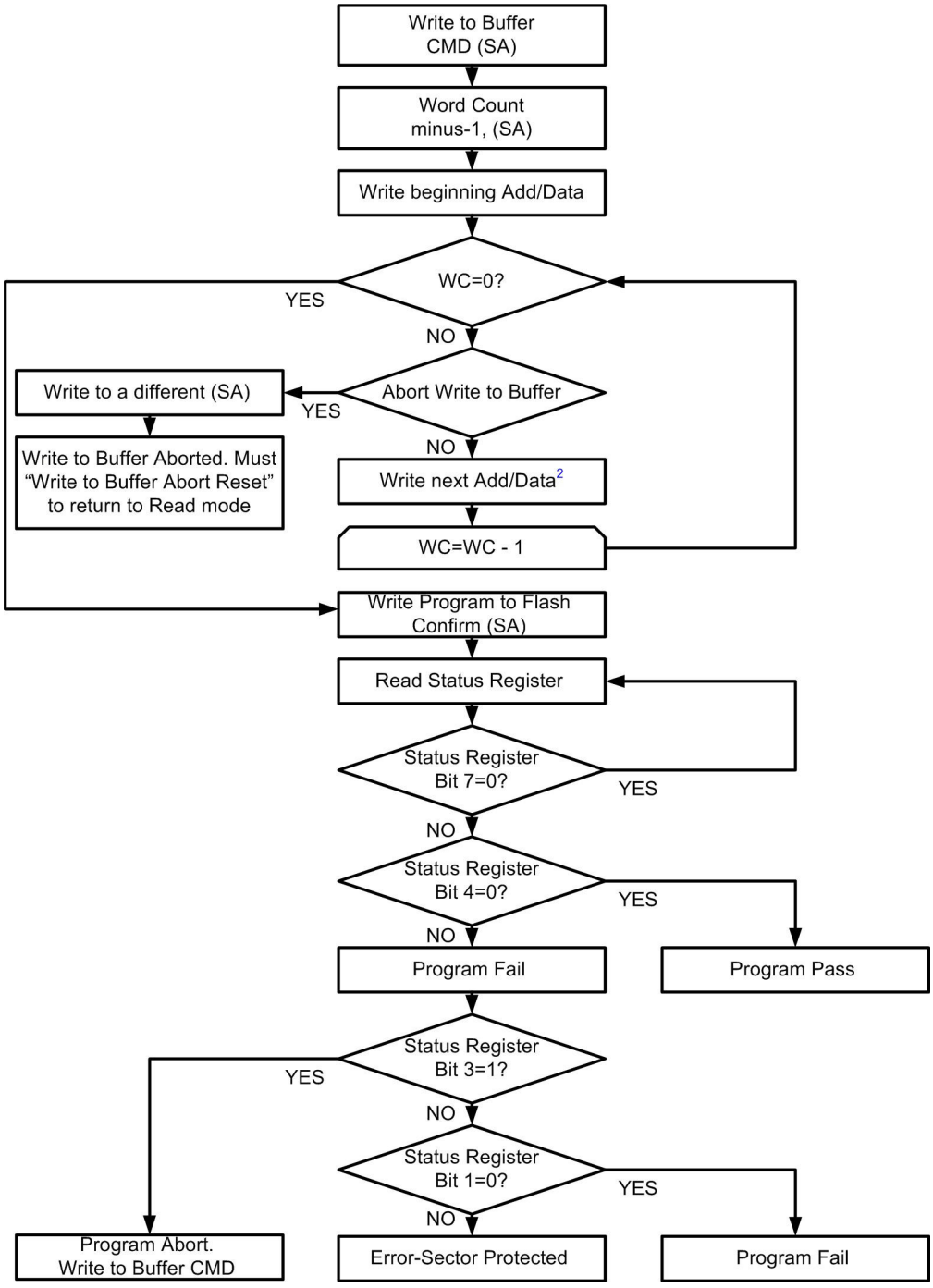
Figure 8-2 Write Buffer Programming Operation with Data Polling Status



Notes:

1. DQ7 should be rechecked even if DQ5 = 1 because DQ7 may change simultaneously with DQ5.
2. If this flowchart location was reached because DQ5 = 1, then the device FAILED. If this flowchart location was reached because DQ1 = 1, then the Write Buffer operation was ABORTED. In either case the proper RESET command must be written to the device to return the device to READ mode. Write-Buffer-Programming-Abort-Rest if DQ1 = 1, either Software RESET or Write-Buffer-Programming-Abort-Reset if DQ5 = 1.
3. See Instruction Definitions Tables for the command sequence as required for Write Buffer Programming.
4. When Sector Address is specified, any address in the selected sector is acceptable. However, when loading Write-Buffer address locations with data, all addresses MUST fall within the selected Write-Buffer Page.

Figure 8-3 Write Buffer Programming Operation with Status Register



Notes:

1. See Instruction Definitions Tables for the command sequence as required for Write Buffer Programming.
2. When Sector Address is specified, any address in the selected sector is acceptable. However, when loading Write-Buffer address locations with data, all addresses MUST fall within the selected Write-Buffer Page.

Table 8-1 Write Buffer Programming Command Sequence

Address	Data	Sequence	Comment
555	AA	Unlock Command 1.	
2AA	55	Unlock Command 2.	
SA	0025h	Write to Buffer Command at Sector Address.	
SA	WC	Number of Locations at Sector Address.	WC = number of words to program minus 1
		WC set to 1 = 2 words to program.	Example
Starting Address	PD	Write Starting Address / Data pair.	Selects Write-Buffer-Page and loads first Address/Data Pair.
WBL	PD	Write next Address / Data pair.	All addresses MUST be within the selected write-buffer-page boundaries, and have to be loaded in sequential order.
WBL	PD	Write LAST Address/Data pair.	All addresses MUST be within the selected write-buffer-page boundaries, and have to be loaded in sequential order.
SA	0029h	Write Buffer Program Confirm at Sector Address.	This command MUST follow the last write buffer location loaded, or the operation will ABORT.
		Device goes busy.	

Legend:

SA = Sector Address (Non-Sector Address bits are don't care. Any address within the Sector is sufficient.)

WBL = Write Buffer Location (MUST be within the boundaries of the Write-Buffer-Line specified by the Starting Address.)

WC =Word Count

PD = Program Data

8.7 Program Suspend / Program Resume Commands

An internal programming operation can be interrupted so that data can read from any non-suspended Boundary Line by using the Program Suspend command. During a programming process and the Program Suspend command is written, the programming operation will halt within the period of t_{PSL} and the status bits will be updated. When writing the Program Suspend command addresses are don't care.

Program Suspend has two commands available; The Erase/Program suspend command (B0h command code), which is a combined legacy command. The Program Suspend command (51h command code). Program resume also has two possible commands; The Erase / Program resume command (30h command code) legacy combined command. Program Resume command (50h command code). It is recommended not to use the combine Erase/Program suspend or the combined Erase/Program resume commands for programming and for the erase suspend and resume use the legacy combined commands.

After suspending the programming operation, any non-suspended Line of array data can be read. If during an Erase Suspended operation to start a Programming operation that was suspended, only addresses not in the Erase or Program Suspend may be read.

The device returns back to program operation and the status bits are updated after the Program Resume command is executed. Monitoring the Status Register or using the Data Polling method, the programming operation status can be determined.

During Program Suspend, valid accesses and commands:

- Any non-erase suspended sector can be Read
- Any non-program suspended Line can be Read.
- Status Read command
- Exit MMO or Command Set Exit
- Program Resume command

Program Resume command must be executed to exit the Program Suspend mode to continue the programming operation. Resume commands are ignored once the device has returned to the programming operation. After the device has resumed programming operation a Program Suspend command can be re-written.

Programming operations can be interrupted as often as necessary but, the minimum requirement between a Program Resume and the next Program Suspend must be greater than or equal to t_{PRS}.

Not supported is Program suspend and resume mode while entered in an MMO. Likewise, there is no support while in program suspend to enter into MMO.

8.8 Erase Methods

8.8.1 Chip Erase

The entire Main Memory Array is erased by chip erase function. The Internal Erase Algorithm will first program and verifies the entire memory prior to an electrical erase. All locations within the device will contain FFFFh after a successful chip erase. There is no need to provide any control signals or timing parameters during this operation. Initiating the chip erase command sequence requires writing two unlock cycles, the a setup command cycle, two additional unlock write cycles and then the chip erase command, which in turn actives the Internal Erase Algorithm.

While the Internal Erase operation is in progress, no data can be read from the device. Chip Erase operation status can be determined by reading the Status Register or using Data Polling. Only a Status Read, Hardware RESET or Power cycle are valid, once the chip erase operation has begun, ignoring all other commands. When the Internal Erase Algorithm has finished, the Write State Controller will return to the standby mode. However, in the case of a Hardware Reset or Power Cycle, the erase operation immediately terminates and returns to read mode after a period of t_{RPH}. In the event the chip erase operation is terminated and to insure the integrity of the device data, the chip erase command sequence should be reinitiated once the device has returned to an idle state.

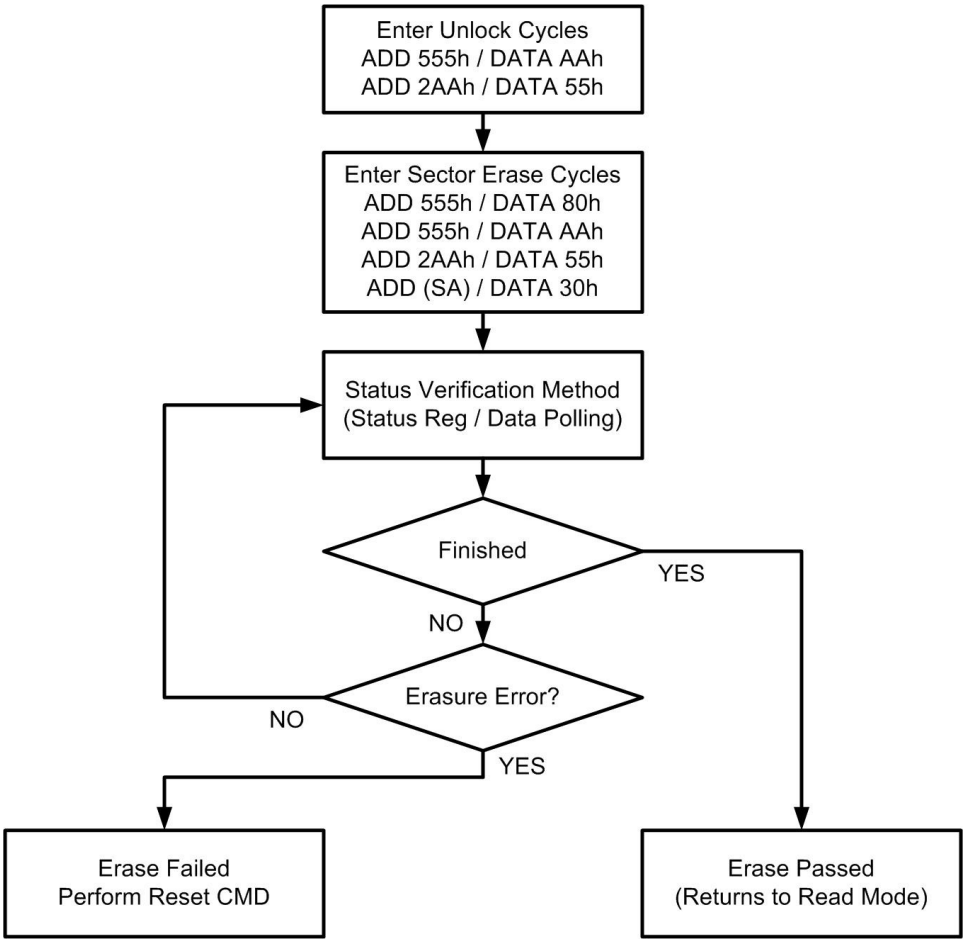
If a sector is protected during chip erase, the Internal Erase Algorithm will ignore the protected sector and move on to the next sector erase.

8.8.2 Sector Erase

The sector erase function erases a selected 128-kbyte sector in the main memory array. The Internal Erase Algorithm programs and verifies the select sector prior to an electrical erase. There are no requirements for any control signals or timing parameters during this internal operation. All locations within the erased sector will contain an FFFFh pattern, indicating a successful sector erase. If the sector has been protected, the sector will not be erased. Reading the Status Register or using Data Polling can be used to determine the status of the erase operation. It takes six cycles to perform a sector erase command sequence; writing two unlock cycles, followed by a setup command, writing two more unlock cycles, and the sector erase command that contains the address of the desired sector to be erased.

The Status Register Read and Erase Suspend commands are the only valid commands that can be used after the sector erase operation has commenced, ignoring all other commands. The sector erase operation and be terminated abruptly by a hardware reset at which time the device returns to read mode after a period t_{RPH}. If this is the case, the sector erase command procedure must be redone again once the device has completed the reset operation to ensure integrity of the data.

Figure 8-4 Sector Erase operation



8.9 Erase Suspend / Erase Resume

The Erase Suspend command interrupts a sector erase operation making it possible to read data or program data in the main memory array. The Erase Suspend command is valid when a sector erase or a program operation is in progress. Executing an Erase Suspend command during a chip erase operation will be ignored. The device requires a maximum of t_{ESL} to suspend the erase operation and update the status bits any time the Erase Suspend command is executed during the a sector erase operation.

Once in the erase-suspend mode, the Main Memory Array can be read or programmed. Reading at any address outside erase-suspended sectors produces valid data. Reading within the suspended sectors will result in invalid data. Monitoring the Status Register or Data Polling can be used to determine the status of the device actively performing an erase or erase-suspended function.

The Write State Controller will return the device back to the erase-suspend mode after a program operation has completed that was called from the erase suspend mode. The status of the program operation can be determined by reading the Status Register, the same as in the standard program operation.

In the event there is a program failure during an Erase Suspend operation, it is necessary to initiate a Clear or Reset command to return the device to the Erase Suspended mode. Before trying another

program operation on the main memory array, the erase function will need to be resumed and completed.

During Erase Suspend, valid accesses and commands:

- Any other non-suspended sector can be read.
- Any other non-suspended sector can be programmed.
- Status Read command
- Enter DPB MMO
- DPB Set
- DPB Clear
- DPB Status Read
- Exit MMO or Command Set Exit
- Erase Resume command

To resume the sector erase operation, an Erase Resume command must be executed. The device will return back to erasing at which point the status bits will be updated. If another Erase Resume is attempted it will be ignored. Once the device has resumed erase operation another Erase Suspend command can be initiated.

While entered in an MMO, Erase Suspend and Resume is not supported. Likewise, entry into a MMO while an erase suspend is not supported.

8.10 Blank Check

To confirm if a selected sector is erased a Blank Check command should be used. Reads to the main memory array are not supported during a Blank Check operation. Trying to do so will return unknown data. To execute a Blank Check operation on a specific Sector, write the address (SA)555 and the data 33h after the Write State Controller is in the standby mode.

If the device is in a programming or erase mode of operation a Blank Check command cannot be written.

The Status Register can confirm if the device is still busy and when it has completed the Blank Check operation, whether or not the sector is blank. Bit 7, Device Ready Bit of the Status Register will show if a Blank Check is being performed by the device. Bit 5, Erase Status Bit of the Status Register will indicate an erased sector when reading a ‘0’ or a non erased sector when reading a ‘1’. The device will immediately halt the Blank Check operation and update the status as soon as any bit in the selected sector is found not to be erased.

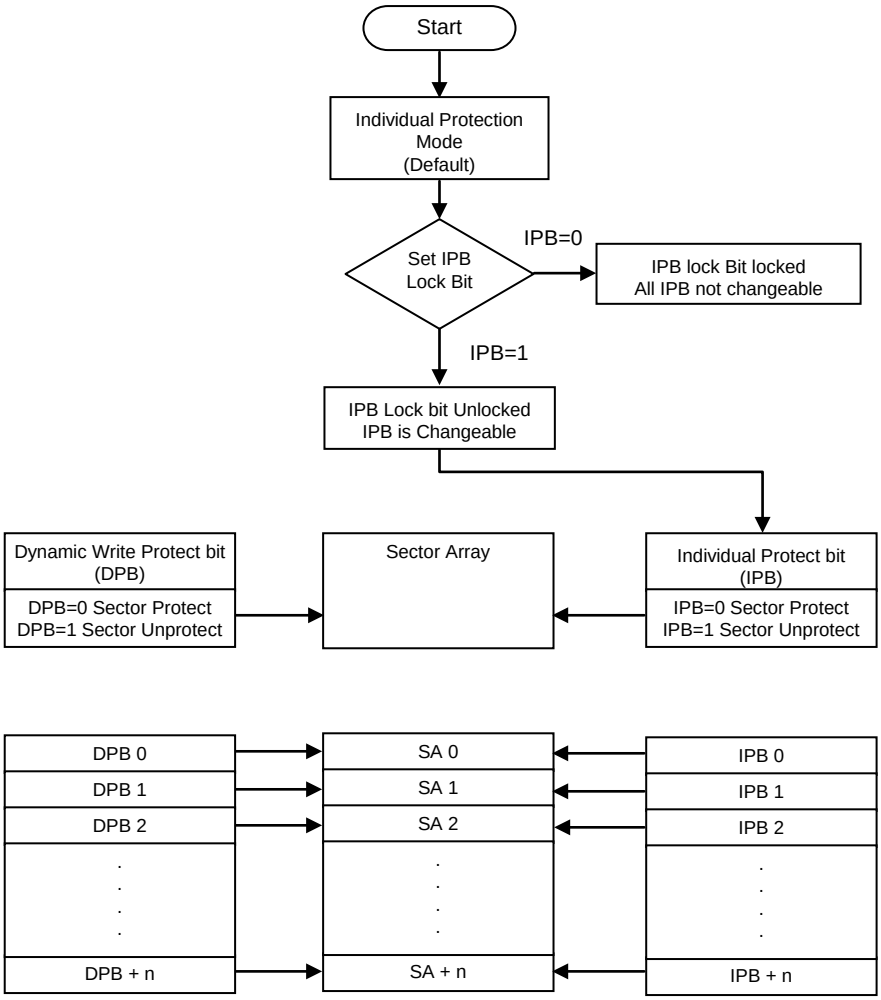
The Write State Controller will return to the Standby mode, as soon as the Blank Check is completed.

8.11 Enhanced Sector Protection Methods

8.11.1 Enhanced Sector Protection (ESP)

Enhanced Sector Protection is a method used to enable or disable program and erase operations, in any or all sectors. Described in the section are the various methods of protecting data stored in the main memory array. An outline of these methods is shown in the following figure.

Figure 8-5 Enhanced Sector Protection IPB Program Algorithm



Each sector has a non-volatile Individual Protection Bit (IPB) and a volatile Dynamic Protection Bit (DPB) associated with it. If in either case the bit is 0, the sector becomes protected from both program and erase operations.

Program and erase of the IPB bits are protected when the IPB Lock bit is 0.

The Individual Protection mode (default) clears the IPB Lock to a 1 during a Power Up Reset or Hardware Reset. This is done so that the IPB bits are unprotected after device reset. When needed there is a IPB Lock bit command to write the volatile IPB Lock bit to a 0 to protect the all the IPB. There is no command in the Individual Protection mode to clear the IPB Lock bit to 1 after it is programmed to 0, except for the Power Up Reset or Hardware resets.

The selection of the Individual Protection mode is set at the factory by programming OTP bit in the Lock Register.

When shipped from Winbond, all the sector IPB bits are erased so that all main memory array sectors are unprotected.

8.11.2 IPB Lock

This one per device volatile Individual Protection Bit Lock is a bit that will protect all IPB bits. When programmed to 0, it locks all sector IPBs and if the bit is 1, it allows the all sector IPBs to be changed.

Only after the sector IPBs are configured to the desired state should the IPB Lock bit be programmed to 0. Note the IPB Lock command can only program the bit to 0.

To erase the IPB Lock bit, only a Power Up Reset or a hardware reset will restore the value to 1 to allow sector IPB bits to be changed. There is no software command operation that can clear the IPB Lock to a 1.

8.11.3 Individual Protection Bits (IPB)

The non-volatile Individual Protection Bits (IPB) is located in a separate non-volatile flash array. There is one IPB bit assigned to each sector. When an IPB is 0 their corresponding sectors is protected from program and erase operations. The IPB can be programmed individually, but are erased as a group. Important to note, the Write State Controller takes care of the preprogramming and verification prior to erasure.

When programming an IPB bit the typical word programming time is required. To monitor the operation status of an IPB bit programming or erase, DQ6 Toggle Bit I of the Data Polling Status will toggle until the operation is complete. Note; typical sector erase time is required to erasing all the IPBs.

Program or erase command will not execute and will time-out, if the IPB Lock is equal 0, without programming or erasing the IPB.

The IPB Status Read command can be used to check the protection state of an IPB for a given sector, but you must first enter the IPB MMO mode. *See Instruction Definition Tables*.

8.11.4 Dynamic Protection Bits (DPB)

The volatile Dynamic Protection Bits are exclusive for each sector and can be individually changed. Only sectors that have their IPBs clear to 1 (unprotected) can the DPBs control. By issuing the DPB Set or Clear command sequences, the DPB are clear to 1 or set to 0, thus placing each sector in the unprotected or protected state respectively. The DPB can be set to 0 or cleared to 1 as often as needed.

8.11.5 Sector Protection Bit Status Summary

Sector Protection status base on IPB, DPB and IPB Lock bit weight is as follows:

Table 8-2 Sector Protection Status

Sector Status	Sector Protection Bit Status		
	IPB Lock	IPB	DPB
Unprotected: IPB and DPB are changeable	1	1	1
Protected : IPB and DPB are changeable	1	1	0
Protected: IPB and DPB are changeable	1	0	1
Protected: IPB and DPB are changeable	1	0	0
Unprotected: DPB is changeable	0	1	1
Protected: DPB is changeable	0	1	0
Protected: DPB is changeable	0	0	1
Protected: DPB is changeable	0	0	0

8.11.6 Lock Register

The Lock Register is a non-volatile One Time Programmable (OTP) register where the bits control protection of the SSR, and the default Individual Protection Mode, programmed at the factory.

The Security Sector Region (SSR) protection bits are OTP and once programmed (locked); there is no command for unlocking the protected portion of the Security Sector Region. At this point no program or erase operations are allow in the SSR.

The Lock Register programming time is typically the same as word programming. Monitoring Data polling Status DQ6 Toggle Bit I during a Lock Register programming Internal Algorithm will toggle until the operation is finished. Another method to monitor the programming status of the Lock Register can be done reading the Status Register's bit 4 and 7. See *Status Register Operations* for information on these status bits.

The Reserved Bits must be 1 (masked), when programming the Lock Register Bits.

Table 8-3 Lock Register

Name	Bit	Default Value
Reserved	15-9	1
Reserved	8	0
Reserved	7	X
SSR Customer Lock Bit	6	1
Reserved	5	1
Reserved	4	1
Reserved	3	1
Reserved	2	1
Individual Protection Mode (Factory Locked)	1	0
SSR Factory Lock Bit	0	0

8.12 Security Sector Region

The Security Sector Region (SSR) MMO provides an extra flash memory area that can be programmed once and permanently protected from further changes. The SSR is 1024 bytes in length. It consists of two 512 bytes regions, Factory Locked Security Sector Region and 512 bytes for Customer Locked Security Sector Region.

The Secure Silicon Entry command sequence contains the sector address; this will overlay the Security Sector Region address map on the Main Memory Array selected sector. The overlay starts at location 0 in the selected sector. While the SSR MMO is entered the contents of locations exceeding the maximum SSR MMO address of that sector are consider as undefined data.

Table 8-4 Security Sector Region

Word Address Range	Content	Size
(SA) + 0000h to 00FFh	Factory Locked Security Sector Region	512 bytes
(SA) + 0100h to 01FFh	Customer Locked Security Sector Region	512 bytes
(SA) + 0200h to FFFFh	Undefined	127 Kbytes

8.13 Monitoring Device Status

Status Register, Data Polling and the Ready/Busy# (RY/#BY) Signal are the three methods for monitoring Internal Algorithms status.

8.13.1 Status Register

The Status Register MMO is a 16-bit register that provides status of program and erase operations. The Status Register Read command is a two cycle command. First cycle overlays the contents of the status register in all locations of the device address space. The second cycle reads the information contents of the status register. The Status Register MMO is exited automatically after the read access.

After the status register read access, #CE or #OE must go HIGH for a period of t_{CEPH} or t_{OEPH}, respectively to return to the active address space at the time the initial Status Register Read command was executed.

Some of the Status Register bits are associated to the results indicating success / failure of the most recently completed Internal Algorithm, while remaining bits are for current status of an Internal Algorithm that is in progress, suspended or has completed.

The upper 8 bits DQ[15:8] are reserved. They are undefined bits that should be treated as don't care and ignored. The Clear Status Register Command will turn results related bits to 0, but will not affect the current state bits.

Table 8-5 Status Register

Bit #	Bit Description	Reset Status	Busy Status	Read Status
15:8	Reserved	X	Invalid	X
7	Device Ready Bit	1	0	1
6	Erase Suspend Status Bit	0	Invalid	Erase not Suspended=0 Erase is Suspended=1
5	Erase Status Bit	0	Invalid	Erase successful=0 Erase fail=1
4	Program Status Bit	0	Invalid	Program successful=0 Program fail=1
3	Write Buffer Abort Status Bit	0	Invalid	Program not aborted=0 Program aborted during Write to Buffer command=1
2	Program Suspend Status Bit	0	Invalid	No Program in suspension=0 Program in suspension=1
1	Sector Lock Status Bit	0	Invalid	Sector not locked during operation=0 Sector locked error=1
0	Reserved	0	Invalid	X

Notes:

1. DQ 7 is '1' when there is no Internal Algorithm in progress in the device. 2. DQ[6:1] are valid only if DQ7 is '1'. 3. All bits are put in their reset status by Power-up reset or Hardware reset. 4. DQ[5:3, 1] is cleared to 0 by the Clear Status Register command or Reset command. 5. Upon issuing the Erase Suspend Command, the user must continue to read status until DQ7=1. 6. DQ6=0 by the Erase Resume Command. 7. DQ5 indicates either a success or failure of the most recent erase operation. 8. DQ4 indicates a success or failure of the most recent program operation. 9. During erase suspend, programming to the suspended sector, will cause program failure and set the DQ4=1. 10. Upon issuing the Program Suspend Command, the user must continue to read status until DQ7=1. 11. DQ2=0 by the Program Resume Command. 12. DQ1 indicates the status of the most recent program or erase operation that a program or erase and if the operation failed because the sector was locked.

8.13.2 Data Polling Status

During an active Internal Algorithm the Write State Controller switches to the Data Polling MMO to display Internal Algorithms status to any read access. A single word (2-Bytes) of status information is available in all locations of the device address space. In the status word there are several bits to determine the status of an Internal Algorithms. These are the DQ bits as they appear on the I/O data bus during a read access while an Internal Algorithms is in progress. The upper byte (DQ[15:8]), DQ4, and DQ0 are reserved and are undefined data and should be treated as don't care. See *Data Polling Status Table.*

8.13.2.1 Data# Polling (DQ7)

I/O pin DQ7 is the Data# Polling bit that indicates whether the device has an Internal Algorithm in progress or has completed. Data# Polling becomes valid on DQ7 on the last rising edge of #WE after a Program or Erase command sequence. During a Write Buffer Programming operation, the final word being programmed in the write buffer-page is the only time Data# Polling is valid. Polling Status is undefined at any other location.

The device outputs complement of the data on DQ7 during an Internal Program algorithm. The same applies during Erase Suspend mode while a programming operation is in effect. The device outputs the programmed data bit to DQ7 of the last word programmed after the Internal Program algorithm has complete. Note the device allows only reading array data during a Program Suspend. A program address falling in a protected sector will cause Data# Polling on DQ7 to be active for approximately 20 µs, at which time the device returns to reading the Main Memory array.

During the Internal Erase or blank check algorithms, Data# Polling produces a 0 on DQ7. When the algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a 1 on DQ7. This is similar to the complement data polling output described for the Internal Program algorithm. Addresses must be within the sector selected for erase to read valid status on DQ7.

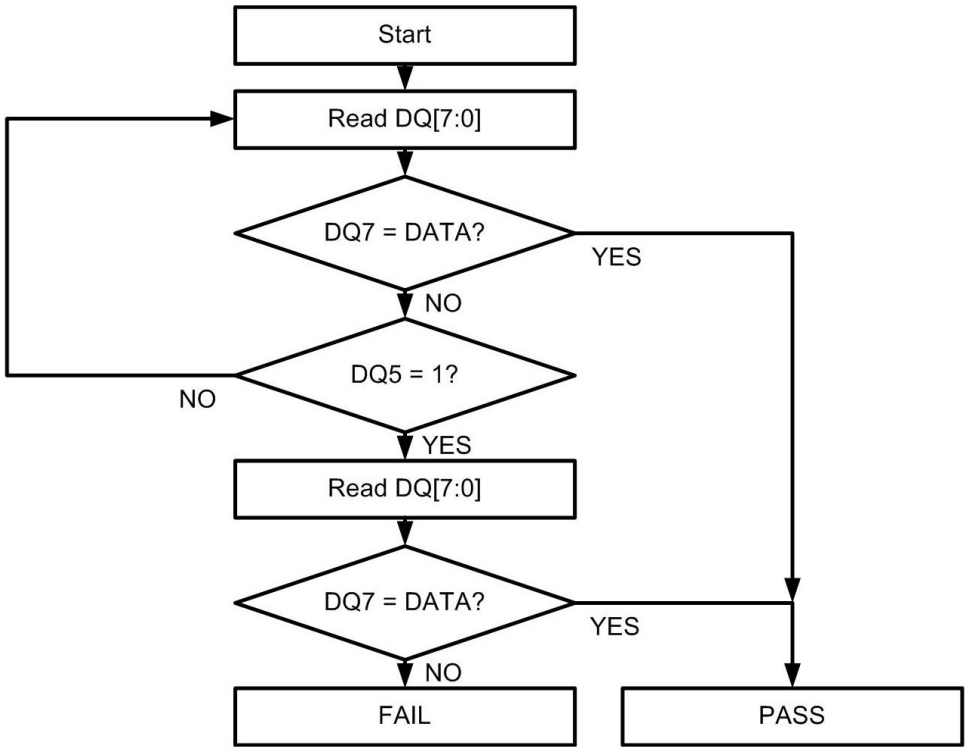
If the sector selected for erasing is protected and an erase command sequence is written, DQ7, Data# Polling is active for approx. 100 µs, then the device returns to reading the Main Memory array.

When DQ7 has changed from the complement to true data, valid data can be read on DQ[15:0] on the next read cycles. This is because DQ7 may change independently with DQ[6:0] while Output Enable (#OE) is held LOW. *See Data# Polling (During Embedded Algorithms) Figure or Data Polling Status Table* these shows the outputs for DQ7, Data# polling. *Figure for Write Buffer Programming Operation with Data Polling Status* shows the Data# polling.

DQ7 Data# Polling status may only be read:

- At the address of the last word loaded into the Write Buffer for a Write Buffer programming operation;
- The location of a single word programming operation.
- A location in a sector being erased or blank checked.

Figure 8-6 Data# Polling Algorithm



Note:
DQ7 should be rechecked even if DQ5 = 1 because DQ7 may change simultaneously with DQ5.

8.13.2.2 DQ6: Toggle Bit I

Data IO Pin, DQ6 (Toggle Bit I), when monitored can indicate if there is an Internal Program or Erase algorithm in progress or has completed. It also can indicate whether the device is in a Program or Erase Suspended mode. Toggle Bit I, is valid and can be read at any address after the rising edge of the last #WE pulse in a program or erase operation command sequence. Successive read cycles to any address during an internal program or erase algorithm operation will cause DQ6 to toggle. DQ6 stops toggling when either the program or erase operation has complete.

After the execution of an erase command sequence and that selected sector is protected, DQ6 will toggle for about 100µs at which time the Write State Controller returns to the standby mode.

Data IO Pins DQ6 and DQ2 together can determine whether a sector is actively erasing or erase-suspended. When the device has an internal erase algorithm in progress, DQ6 will toggle. If the device enters a Program Suspend or Erase Suspend mode, DQ6 will stop toggling. To determine which sectors are erasing or erase suspended, DQ2 must also be monitored. Alternative to this, DQ7 can be used (see *DQ7: Data# Polling*).

During the Erase Suspend Program mode DQ6 also toggles and once the internal program algorithm has finished, DQ6 will stop toggling.

Refer to the Data Polling Status Table, Toggle Bit Program flowchart, DQ2: Toggle II section, Reading Toggle Bits DQ6/DQ2 section and the Toggle Bit Timing Diagrams for more information.

8.13.2.3 DQ3: Sector Erase Timer

To determine whether or not a sector erase has begun after a sector erase command sequence, DQ3 may be monitored. Refer to *Sector Section* for more details.

After the sector erase command has been entered, it is recommended to read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to determine that the device has received the command sequence, followed by reading DQ3. If Internal Erase algorithm has begun, then DQ3 should have a value of 1. Refer *Data Polling Status Table* for more information.

8.13.2.4 DQ2: Toggle Bit II

Data IO Pin, DQ2 (Toggle Bit II) when accompanied with DQ6 (Toggle Bit I), monitors whether the selected sector is actively performing an Internal Erase algorithm or if the sector is erase-suspended. Toggle Bit II status becomes valid after the command sequence and the final rising edge of #WE pulse.

DQ2 toggles when read at addresses within the selected sector that which the erase algorithm was started. Use either #OE or #CE to control the read cycles. Monitoring just DQ2 is not enough to tell whether the sector is currently erasing or is in an erase-suspended state. By comparing DQ6 which indicates if the device is currently erasing, or is in an Erase Suspend state, but is not capable of distinguishing the selected sector for erase. So, to discern the correct sector and mode of operation, both status bits is required.

Refer to the *Data Polling Status Table*, *Toggle Bit Program flowchart*, DQ2: Toggle II section, Reading Toggle Bits DQ6/DQ2 section and the *Toggle Bit waveform figure* for more information.

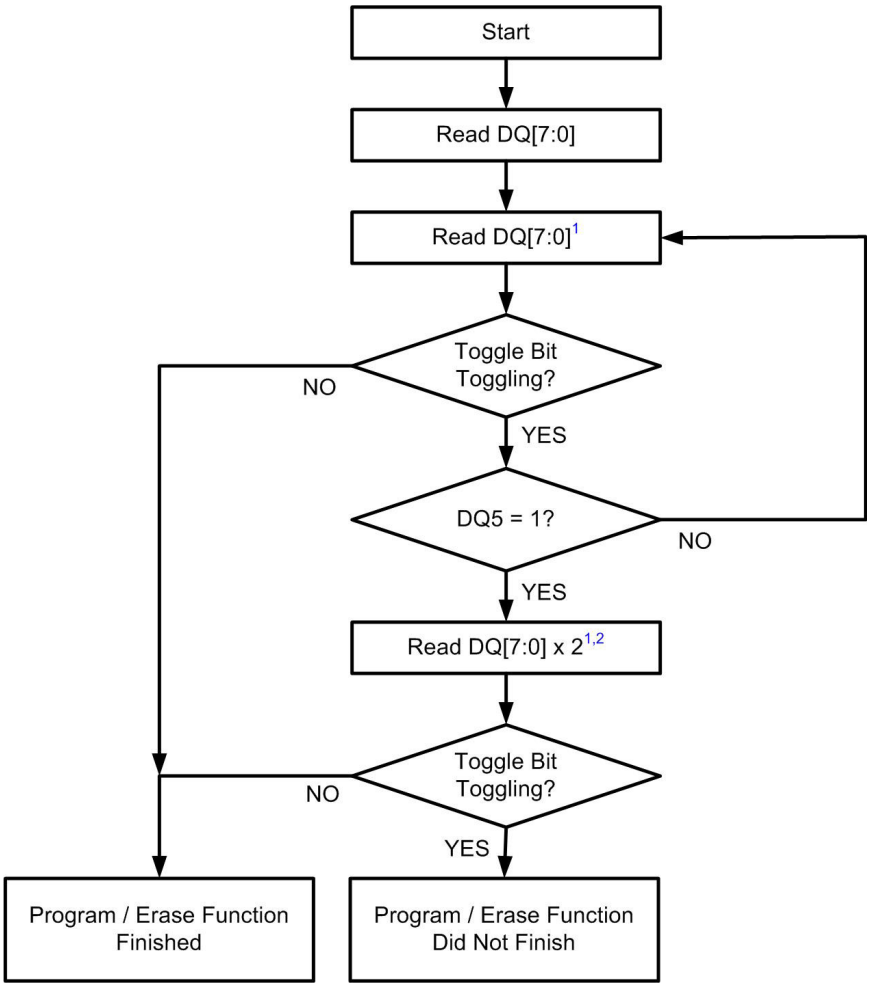
8.13.2.5 Toggle Bits DQ6/DQ2

In order to discern Toggle bit status, DQ7-DQ0 must be read at least twice in a row to determine if a toggle bit is actually toggling. If it is determined that the toggle bit has stopped toggling, this would indicate that the device has either completed the program or erase operation. This being the case, on the next read cycle array data on DQ15-DQ0 can be read.

If it is determines that the toggle bit is still toggling, then DQ5 (Exceeded Timing Limits) should be read to see if the current operation has exceeded its timed limit (DQ5=1). If the value of DQ5 is '1' then another read of the toggle bit should be done in case DQ5 went high at the same time the toggle bit stop toggling. A successful completion of a program or erase operation is indicated by the toggle bit has stopped toggling. If the toggle bit is toggling, the operation did not complete successfully and then must issue the reset command to return to reading array data.

Refer to *Toggle Bit Program Figure*.

Figure 8-7 Toggle Bit Program



Notes:

1. Read toggle bit twice to determine whether or not it is toggling. See text.
2. Recheck toggle bit because it may stop toggling as DQ5 changes to 1. See text.

8.13.2.6 DQ5: Exceeded Timing Limits

There is in place a specified internal pulse count for program or erase operations that when exceeded, DQ5 value will be equal to '1'. This is considered a fail for a program or erase operation

that has not completed successfully. In this situation, a reset command must be executed to return back to a read array mode. It is possible that the device will continue to indicate busy for up to 2 µs following the reset command.

8.13.2.7 DQ1: Write-to-Buffer Abort

Write-to-Buffer operation was aborted if DQ1 equals '1'. If this happens, a Write-to-Buffer-Abort-Reset command sequence must be executed to bring the Write State Controller to standby and clear the Status Register failed bits. For more details, see *Write Buffer Programming section*.

Table 8-6 Data Polling Status

Operation		DQ7[2]	DQ6	DQ5[1]	DQ3	DQ2[2]	DQ1[4]	RY/#BY
Standard Mode	Internal Program Algorithm	DQ7#	Toggle	0	N/A	No Toggle	0	0
	Reading within Erasing Sector	0	Toggle	0	1	Toggle	N/A	0
	Reading Outside erasing Sector	0	Toggle	0	1	No Toggle	N/A	0
Program Suspend Mode[3]	Reading within Program Suspended Sector	INVALID (Not Allowed)	INVALID (Not Allowed)	INVALID (Not Allowed)	INVALID (Not Allowed)	INVALID (Not Allowed)	INVALID (Not Allowed)	1
	Reading within Non-Program Suspended Sector	Data	Data	Data	Data	Data	Data	1
Erase Suspend Mode	Reading within Erase Suspended Sector	1	No Toggle	0	N/A	Toggle	N/A	1
	Reading within Non-Erase Suspend Sector	Data	Data	Data	Data	Data	Data	1
	Programming within Non-Erase Suspended Sector	DQ7#	Toggle	0	N/A	N/A	N/A	0
Write-to-Buffer[4]	BUSY State	DQ7#	Toggle	0	N/A	N/A	0	0
	Exceeded Timing Limits	DQ7#	Toggle	1	N/A	N/A	0	0
	ABORT State	DQ7#	Toggle	0	N/A	N/A	1	0

Notes:

1. DQ5 switches to '1' when an Internal Program or Internal Erase operation has exceeded the maximum timing limits. See *DQ5: Exceeded Timing Limits* for more information.
2. DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.
3. Data are invalid for addresses in a Program Suspended Line.
4. DQ1 indicates the Write-to-Buffer ABORT status during Write-Buffer-Programming operations.

8.14 Enhanced Variable I/O

The Data I/O maximum drive and receive voltages are determined by the EVIO supply. This feature allows the device IO pins to be compatible with signal buses that have different voltage levels than the core device voltage.

8.15 Ready/#Busy

The Ready/#Busy (RY/#BY) is a dedicated output pin that indicates whether a Hardware Reset, a Power Up Reset, or an internal algorithm operation is in progress or has finished. A valid output from the RY/#BY is after the falling edge of #RESET, VCC is higher than VCC minimum during Power Up Reset or after the rising edge of the final #WE pulse during a command sequence. The RY/#BY pin is an open drain output that should have a pull up resistor tied to EVIO.

While the Ready/#Busy output is HIGH (Ready), the device is capable of reading data in the Read, Erase Suspend, or in standby modes. When the device is actively performing an erase, program, or reset operation, the RY/#BY output is LOW (Busy), including in an Erase Suspend Programming mode.

A reset command needs to be executed and Status Register bits 4 and 5 need to be cleared if a program or erase operation failed as a result of a timeout or a locked sector leaving the RY/#BY in a LOW state (busy).

Refer to the *Data Polling Status Table* for Ready/#Busy output status.

8.16 Hardware Data Protection Options

8.16.1 Write Protect (#WP)

The lowest or highest sector is protected from program or erase operations while Write Protect (#WP) equals V_{IL}, independent of the Enhanced Sector Protection (ESP) configuration. Consequently, if #WP equals V_{IH}, the lowest or highest address sector is not protected by the #WP. The Wrote Protect pin has an internal pull-up circuit so the default is at V_{IH}. It is important to note the High or low sector protection depends on the device ordering option.

8.16.2 Write Pulse “Glitch” Protection

Glitch pulses of less than 5 ns on the #WE pin will not initiate a write cycle.

8.16.3 Power Up Write Inhibit

During Power Up Reset, #RESET, #CE, #WE, and #OE are ignored. The device is unable to be selected, commands are not accepted on the rising edge of #WE, and will not drive outputs during a Power Up Reset. During a Power-up Reset the Command State Machine (CSM) and Write State Controller are reset to their standby modes, ready for reading array data. Before the end of Power Up Reset (t_{VCS}), #CE or #OE must go to V_{IH}.

8.16.4 Logical Inhibit

Write cycles are prevented by holding #OE at V_{IL}, or #CE at V_{IH}, or #WE at V_{IH}. To start a write cycle, #CE and #WE must be equal to V_{IL} while #OE is equal to V_{IH}.

8.17 Inherent Data Protection

8.17.1 Command Protection

Internal Algorithms are started by writing command sequences into the Write State Controller command memory. The command memory array is not readable from the bus interface and has no memory map overlay. Each bus interface write is a command or a segment of a command sequence to the device. The Write State Controller analyses the address and data in each write transfer to decide whether the write is part of a legitimate command sequence. When a correct command sequence is finished the Write State Controller will start the appropriate Internal Algorithm.

Writing an incorrect command sequence, can most likely result in the Write State Controller returning to its Standby mode. However, there is a possibility that an improper command sequence may cause the device to go into an unknown state, in that case a reset command must be executed or possibly a hardware reset, to return the Write State Controller to its Standby mode.

8.18 Operating Modes and Signal States Table

Table 8-7 Interface Conditions

Mode / Signal	Page Read	Random Read	Read with Output Disabled[2]	Write	Automatic Sleep[1,3]	Standby	Hardware Reset	Power Up Reset
VCC	≥ VCC min	≥ VCC min	≥ VCC min	≥ VCC min	≥ VCC min	≥ VCC min	≥ VCC min	≥ VCC min
EVIO	≥ EVIO min ≤ VCC	≥ EVIO min	≥ EVIO min ≤ VCC	≥ EVIO min ≤ VCC	≥ EVIO min ≤ VCC	≥ EVIO min ≤ VCC	≥ EVIO min ≤ VCC	≥ EVIO min ≤ VCC
#CE	VIL	VIL	VIL	VIL	VIL	VIH	X	X
#OE	VIL	VIL	VIH	VIH	X	X	X	X
#WE	VIH	VIH	VIH	VIL	X	X	X	X
#RESET	VIH	VIH	VIH	VIH	VIH	VIH	VIL	X
A[23:0]	A[23:4] Valid A[3:0] Modified	Valid	Valid	Valid	Valid	X	X	X
DQ[15:0]	Valid Output	Valid Output	HI-Z	Valid Input	Available Output	HI-Z	HI-Z	HI-Z

This table describes the required condition of each interface signal for each operating mode.

Legend:
X = Don't Care
Valid = all bus signals have stable L or H level
Modified = valid state different from a previous valid state
Available = read data is internally stored with output driver controlled by #OE

Notes:

1. #WE and #OE cannot be at VIL at the same time.
2. Read with Output Disable is a read initiated with #OE HIGH.
3. Automatic Sleep is a read/write operation where data has been driven on the bus for an extended period, without #CE going HIGH and the device internal logic has gone into standby mode to conserve power.

8.19 Instruction Definition Tables

Table 8-8 Read, Write, Program and Erase Definitions

Read, Write, Program and Erase Definitions															
Command Sequence[1]	Cycles	Bus Cycles[2-5]													
		1		2		3		4		5		6		7	
		Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Read[6]	1	RA	RD												
Reset/MMO Exit[7,14]	1	XXX	F0												
Status Register Read	2	555	70	XXX	RD										
Status Register Clear	1	555	71												
Word Program	4	555	AA	2AA	55	555	A0	PA	PD						
Write to Buffer	6	555	AA	2AA	55	SA	25	SA	WC	WBL	PD	WBL	PD		
Program Buffer to Flash (confirm)	1	SA	29												
Write-to-Buffer-Abort Reset[11]	3	555	AA	2AA	55	555	F0								
Chip Erase	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10		
Sector Erase	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30		
Erase Suspend/Program Suspend Legacy Method[9]	1	XXX	B0												
Erase Suspend Enhanced Method															
Erase Resume/Program Resume Legacy Method[10]	1	XXX	30												
Erase Resume Enhanced Method															
Program Suspend Enhanced Method	1	XXX	51												
Program Resume Enhanced Method	1	XXX	50												
Blank Check	1	(SA) 555	33												

Table 8-9 CFI-ID (Autoselect) Definitions

CFI-ID (Autoselect) Definitions															
Command Sequence[1]	Cycles	Bus Cycles[2-5]													
		1		2		3		4		5		6		7	
		Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
ID (Autoselect) Entry	3	555	AA	2AA	55	(SA) 555	90								
CFI Enter[8]	1	(SA) 55	98												
CFI-ID Read	1	XXX	RD												
Reset/MMO Exit[7,14]	1	XXX	F0												

Table 8-10 Security Sector Region Command Definitions

Security Sector Region Command Definitions															
Command Sequence[1]	Cycles	Bus Cycles[2-5]													
		1		2		3		4		5		6		7	
		Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
SSR Entry	3	555	AA	2AA	55	(SA) 555	88								
Read[6]	1	RA	RD												
Word Program	4	555	AA	2AA	55	555	A0	PA	PD						
Write to Buffer	6	555	AA	2AA	55	SA	25	SA	WC	WBL	PD	WBL	PD		
Program Buffer to Flash (confirm)	1	SA	29												
Write-to-Buffer-Abort Reset[11]	3	555	AA	2AA	55	555	F0								
SSR Exit[11]	4	555	AA	2AA	55	555	90	XX	0						
Reset/MMO Exit[7,14]	1	XXX	F0												

Table 8-11 Lock Register Command Set Definitions

Lock Register Command Set Definitions															
Command Sequence[1]	Cycles	Bus Cycles[2-5]													
		1		2		3		4		5		6		7	
		Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Lock Register Entry	3	555	AA	2AA	55	555	40								
Program[13]	2	XXX	A0	XXX	PD										
Read[13]	1	0	RD												
Command Set Exit[12,14]	2	XXX	90	XXX	0										
Reset/MMO Exit[7,14]	1	XXX	F0												

Table 8-12 IPB Non-Volatile Sector Protection Command Set Definitions

IPB Non-Volatile Sector Protection Command Set Definitions															
Command Sequence[1]	Cycles	Bus Cycles[2-5]													
		1		2		3		4		5		6		7	
		Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
IPB Entry	3	555	AA	2AA	55	555	C0								
IPB Program[15]	2	XXX	A0	SA	0										
All IPB Erase[15]	2	XXX	80	0	30										
IPB Read[15]	1	SA	RD (0)												
Command Set Exit[12,14]	2	XXX	90	XXX	0										
Reset/MMO Exit[7,14]	1	XXX	F0												

Table 8-13 Global Non-Volatile Sector Protection Freeze Command Set Definitions

Global Non-Volatile Sector Protection Freeze Command Set Definitions(IPB Lock Bit)															
Command Sequence[1]	Cycles	Bus Cycles[2-5]													
		1		2		3		4		5		6		7	
		Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
IPB Lock Entry	3	555	AA	2AA	55	555	50								
IPB Lock Bit Cleared	2	XXX	A0	XXX	0										
IPB Lock Status Read[15]	1	XXX	RD (0)												
Command Set Exit[12,14]	2	XXX	90	XXX	0										
Reset/MMO Exit[14]	1	XXX	F0												

Table 8-14 DPB Volatile Sector Protection Command Set Definitions

DPB Volatile Sector Protection Command Set Definitions															
Command Sequence[1]	Cycles	Bus Cycles[2-5]													
		1		2		3		4		5		6		7	
		Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
DPB MMO Entry	3	555	AA	2AA	55	555	E0								
DPB Erase[15]	2	XXX	A0	SA	0										
DPB PGM[15]	2	XXX	A0	SA	1										
DPB Status Read[15]	1	SA	RD (0)												
Command Set Exit[12,14]	2	XXX	90	XXX	0										
Reset/MMO Exit[14]	1	XXX	F0												

Legend:

X = Don't care.

RA = Address of the memory to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed.

PD = Data to be programmed at location PA.

SA = Address of the sector selected. Address bits A23-A16 uniquely select any sector.

WBL = Write Buffer Location. The address must be within the same Line.

WC = Word Count is the number of write buffer locations to load minus 1.

Notes:

1. See *Interface Condition Table* for description of bus operations.
2. All values are in hexadecimal.
3. Except for the following, all bus cycles are write cycle: read cycle during Read, ID/CFI Read (Manufacturing ID / Device ID), Indicator Bits, Security Sector Region Read, SSR Lock Read, and 2nd cycle of Status Register Read.
4. Data bits DQ15-DQ8 are don't care in command sequences, except for RD, PD, WC and PWD.
5. Address bits A23-A11 is don't care for unlock and command cycles, unless SA or PA required. (A23 is the Highest Address pin.).
6. No unlock or command cycles required when reading array data.
7. The Reset command is required to return to reading array data when device is in the CFI-ID (Autoselect) mode, or if DQ5 goes HIGH (while the device is providing status data).
8. Command is valid when device is ready to read array data or when device is in CFI-ID (Autoselect) mode.
9. The system can read and program/program suspend in non-erasing sectors, or enter the CFI-ID MMO, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.
10. The Erase Resume/Program Resume command is valid only during the Erase Suspend/Program Suspend modes.
11. Issue this command sequence to return to READ mode after detecting device is in a Write-to-Buffer-Abort state. IMPORTANT: the full command sequence is required if resetting out of ABORT.
12. The Exit command returns the device to reading the array.
13. All Lock Register bits are one-time programmable. The program state = 0 and the erase state = 1. Also, the Individual Protection mode Lock Bit cannot be programmed at the same time or the Lock Register Bits Program operation aborts and returns the device to read mode. Lock Register bits that are reserved for future uses are undefined and may be 0's or 1's.
14. If any of the Entry commands was issued, an Exit command must be issued to reset the device into read mode.
15. Protected State = 00h, Unprotected State = 01h. The sector address for DPB set, DPB clear, or IPB Program command may be any location within the sector - the lower order bits of the sector address are don't care.

8.20 Common Flash Interface and Device ID (CFI-ID)

The Manufacturer ID, Device ID, Sector Protection status, and basic feature information for the device are available when the Device ID portion of the MMO is read, locations 0h to 0Fh.
The sector protection status can be read by entering the CFI-ID command which contains the sector address (SA) and location 02h. If another sector protection status is required, it will be necessary to exit ID MMO and re-enter the CDI-ID command again with the new sector address. Reading location 02h requires an access time of t_{ACC}, #CE should go HIGH before the read and to initiate an asynchronous read access #CE should return LOW again. Page mode read is not support for reading between location 02h and the other ID locations. However, Page mode read supports reads between ID locations other than 02h.

Table 8-15 ID (Autoselect) Address Map

Description	Address	Data
Manufacture ID	(SA) + 0000h	00EFh
Device ID	(SA) + 0001h	227Eh
Protection Verification	(SA) + 0002h	0000h/0001h
Indicator Bits DQ15-DQ08 = 1 (Reserved) DQ7: Factory Locked Security Sector Region 1 = Locked, 0 = Not Locked DQ6: Customer Locked Security Sector Region 1 = Locked, 0 = Not Locked DQ5 = 1 (Reserved) DQ4 - WP# Protects 0 = lowest address Sector, 1 = highest address Sector DQ3 - DQ0 = 1 (Reserved)	(SA) + 0003h	Same as description
RFU	(SA) + 0004h	Reserved
	(SA) + 0005h	Reserved
	(SA) + 0006h	Reserved
	(SA) + 0007h	Reserved
	(SA) + 0008h	Reserved
	(SA) + 0009h	Reserved
	(SA) + 000Ah	Reserved
	(SA) + 000Bh	Reserved
Lower Software Bits Bit 0: Status Register Support 1 = Yes, 0 = No Bit 1:DQ Polling Support 1 = Yes, 0 = No Bit 3-2: Command Set Support 11 = reserved 10 = reserved 01 = Reduced Command Set 00 = Classic Command set Bits 4-15: Reserved = 0	(SA) + 000Ch	0003h
Upper Software Bits	(SA) + 000Dh	Reserved
Device ID	(SA) + 000Eh	2222h
Device ID	(SA) + 000Fh	2201h

Table 8-16 CFI Query Identification String

Description	Address	Data
Query-unique ASII string “QRY”	(SA) + 10h	0051h
	(SA) + 11h	0052h
	(SA) + 12h	0059h
Primary vendor instruction set and control interface ID code	(SA) + 13h	0006h
	(SA) + 14h	0000h
Address for primary algorithm extended query table	(SA) + 15h	0040h
	(SA) + 16h	0000h
Alternate vendor instruction set and control interface ID code	(SA) + 17h	0000h
	(SA) + 18h	0000h
Address for alternate algorithm extended query table	(SA) + 19h	0000h
	(SA) + 1Ah	0000h

Table 8-17 CFI System Interface String

Description	Address	Data
VCC supply minimum program/erase voltage	(SA) + 1Bh	0027h
VCC supply maximum program/erase voltage	(SA) + 1Ch	0036h
VPP supply minimum program/erase voltage	(SA) + 1Dh	0000h
VPP supply maximum program/erase voltage	(SA) + 1Eh	0000h
Typical timeout per single word/byte write, 2^n µs	(SA) + 1Fh	0008h
Typical timeout for maximum-size buffer write, 2^n µs (00h, not support)	(SA) + 20h	0009h
Typical timeout per individual block erase, 2^n ms	(SA) + 21h	0008h
Typical timeout for full chip erase, 2^n ms (00h, not support)	(SA) + 22h	0010h
Maximum timeout for word/byte write, 2^n times typical	(SA) + 23h	0001h
Maximum timeout for buffer write, 2^n times typical	(SA) + 24h	0002h
Maximum timeout per individual block erase, 2^n times typical	(SA) + 25h	0003h
Maximum timeout for chip erase, 2^n times typical (00h, not support)	(SA) + 26h	0003h

Table 8-18 CFI Device Geometry Definition

Description	Address	Data
Device size = 2^n in number of bytes	(SA) + 27h	0019h
Flash device interface description (01=asynchronous x16 only)	(SA) + 28h	0001h
	(SA) + 29h	0000h
Maximum number of bytes in buffer write = 2^n (00h, not support)	(SA) + 2Ah	0009h
	(SA) + 2Bh	0000h
Number of erase regions within device (01h:uniform, 02h:boot)	(SA) + 2Ch	0001h
Index for Erase Bank Area 1: [2E,2D] = # of same-size sectors in region 1-1 [30, 2F] = sector size in multiples of 256K-bytes	(SA) + 2Dh	00FFh
	(SA) + 2Eh	0000h
	(SA) + 2Fh	0000h
	(SA) + 30h	0002h
Index for Erase Bank Area 2	(SA) + 31h	0000h
	(SA) + 32h	0000h
	(SA) + 33h	0000h
	(SA) + 34h	0000h
Index for Erase Bank Area 3	(SA) + 35h	0000h
	(SA) + 36h	0000h
	(SA) + 37h	0000h
	(SA) + 38h	0000h
Index for Erase Bank Area 4	(SA) + 39h	0000h
	(SA) + 3Ah	0000h
	(SA) + 3Bh	0000h
	(SA) + 3Ch	0000h

Table 8-19 CFI Primary Vendor-Specific Extended Query

Description	Address	Data
Query - Primary extended table, unique ASCII string, PRI	(SA) + 40h	0050h
	(SA) + 41h	0052h
	(SA) + 42h	0049h
Major version number, ASCII	(SA) + 43h	0031h
Minor version number, ASCII	(SA) + 44h	0035h
Unlock recognizes address	(SA) + 45h	001Ch
Erase suspend (2= to both read and program)	(SA) + 46h	0002h
Sector protect (N= # of sectors/group)	(SA) + 47h	0001h
Temporary sector unprotect (1=supported)	(SA) + 48h	0000h
Sector protect/Chip unprotect scheme	(SA) + 49h	0008h
Simultaneous R/W operation (0=not supported)	(SA) + 4Ah	0000h
Burst mode (0=not supported)	(SA) + 4Bh	0000h
Page mode (0=not supported, 01 = 4 word page, 02 = 8 word page)	(SA) + 4Ch	0003h
Minimum ACC(acceleration) supply (0= not supported), [D7:D4] for volt, [D3:D0] for 100mV	(SA) + 4Dh	0000h
Maximum ACC(acceleration) supply (0= not supported), [D7:D4] for volt, [D3:D0] for 100mV	(SA) + 4Eh	0000h
WP# Protection 04=Uniform sectors bottom WP# protect 05=Uniform sectors top WP# protect	(SA) + 4Fh	00xxh
Program Suspend (0=not supported, 1=supported)	(SA) + 50h	0001h
Unlock Bypass (0=Not supported, 1=supported)	(SA) + 51h	0000h
Secured Silicon Sector (Customer OTP Area) Size 2^N (bytes)	(SA) + 52h	0009h
Software Features bit 0: status register polling (1 = supported, 0 = not supported) bit 1: DQ polling (1 = supported, 0 = not supported) bit 2: new program suspend/resume commands (1 = supported, 0 = not supported) bit 3: word programming (1 = supported, 0 = not supported) bit 4: bit-field programming (1 = supported, 0 = not supported) bit 5: autodetect programming (1 = supported, 0 = not supported) bit 6: RFU bit 7: multiple writes per Line (1 = supported, 0 = not supported)	(SA) + 53h	008Fh
Page Size = 2^N bytes	(SA) + 54h	0005h
Erase Suspend Time Maximum <2^N (µs)	(SA) + 55h	0006h
Program Suspend Timeout Maximum < 2^N (µs)	(SA) + 56h	0006h
Embedded Hardware Reset Timeout Maximum < 2^N (µs) Reset with Reset Pin	(SA) + 78h	0006h
Non-Embedded Hardware Reset Timeout Maximum < 2^N (µs) Power on Reset	(SA) + 79h	0009h

9 ELECTRICAL SPECIFICATIONS

9.1 Absolute Maximum Ratings

Table 9-1 Absolute Maximum Ratings

PARAMETER	Values
VCC	-0.5V to +4.0V
EVIO	-0.5V to +4.0V
All pins other than #RESET[1]	-0.5V to (EVIO + 0.5V)
#RESET[1]	-0.5V to (VCC + 0.5V)
Output Short Circuit Current[2]	100 mA
Storage Temperature Plastic Packages	-65°C to +150°C
Ambient Temperature with Power Applied	-65°C to +125°C

Notes:

1. During signal transitions the I/O or input pins can undershoot VSS to a maximum of -2.0V or overshoot to a maximum of VCC +2.0V for periods of up to 20 ns. See *Maximum Negative Overshoot Waveform and Maximum Positive Overshoot Waveform*. Minimum DC voltage on input or I/O pins is -0.5V and the Maximum DC voltage on input or I/O pins is VCC +0.5V.
2. Duration of an output short circuit should not be greater than one second and more than one output may be shorted to ground at a time.
3. Permanent damage to the device can be cause by stressing the device above those listed under *Absolute Maximum Ratings*. Device reliability may be affected by operating the device at Absolute Maximum Ratings for a prolonged period of time.

9.1.1 Input Signal Overshoot

Figure 9-1 Max Negative Overshoot Waveform

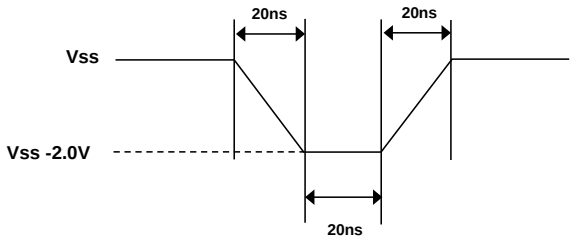
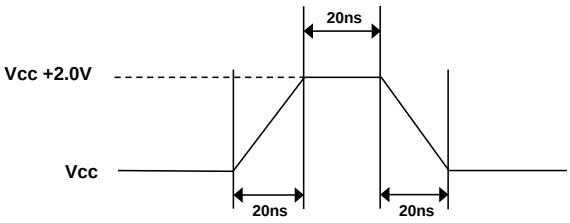


Figure 9-2 Max Positive Overshoot Waveform



9.2 Operating Ranges

9.2.1 Temperature Ranges

Industrial (I)
Ambient Temperature (T_A) -40°C to +85°C

9.2.2 Power Supply Voltages

VCC 2.7V to 3.6V
E_{VIO} 1.65V to VCC + 200 mV
These voltages ranges are guaranteed in which the devices will functionally operation.

9.2.3 Power Up and Power-Down

VCC must at all times be greater than or equal to E_{VIO}. E_{VIO} must follow the rise and fall of VCC within 200 mV when E_{VIO} is under the E_{VIO} minimum.

During period of t_{VCS}, which starts the moment that VCC and E_{VIO} both raise above the minimum VCC and E_{VIO} thresholds and remains stable, the device will perform power on reset operations and will ignore all inputs until t_{VCS} period has elapsed.

In an event of a power down or voltage drop, it is important that VCC and E_{VIO} voltages must drop below V_{RST} minimum for a period of at least t_{PD} to ensure the device will initialize properly when VCC and E_{VIO} rise to their operating ranges once again. *See Power-down and Voltage Drop Figure*. A hardware reset can be used to initialize the device, if the device locks up from incorrect initialization.

Power supply decoupling of VCC and E_{VIO} should have a suitable capacitor (in the order of 0.1 µF) near the package connections.

Table 9-2 Power Up/Power-Down Voltage and Timing

Description	Parameter	Min	Max	Unit
VCC and E_{VIO} ≥minimum to first access[1]	t_{VCS}	300		µs
Duration of VCC ≤ V_{RST}(min)[1]	t_{PD}	15		µs
VCC Power Supply	VCC	2.7	3.6	V
VCC and E_{VIO} LOW voltage needed to ensure initialization will occur[1]	V_{RST}	1.0		V

Notes:
1. Not 100% tested.

Figure 9-3 Power-up

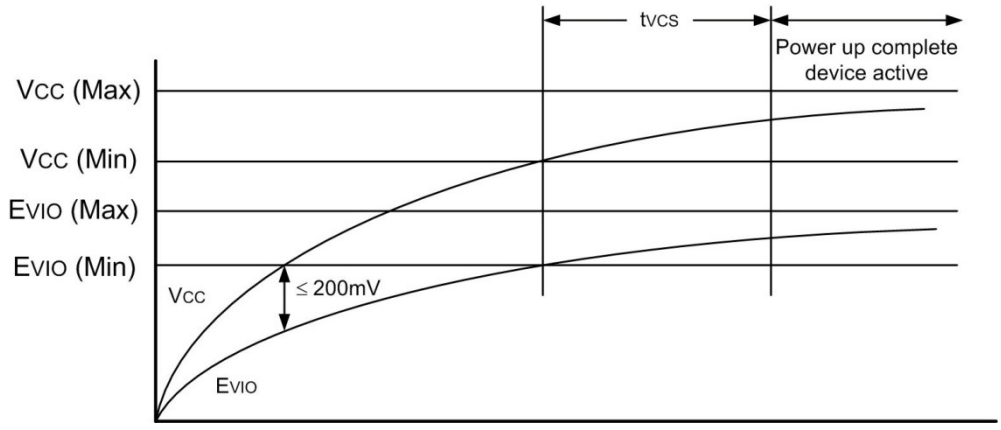
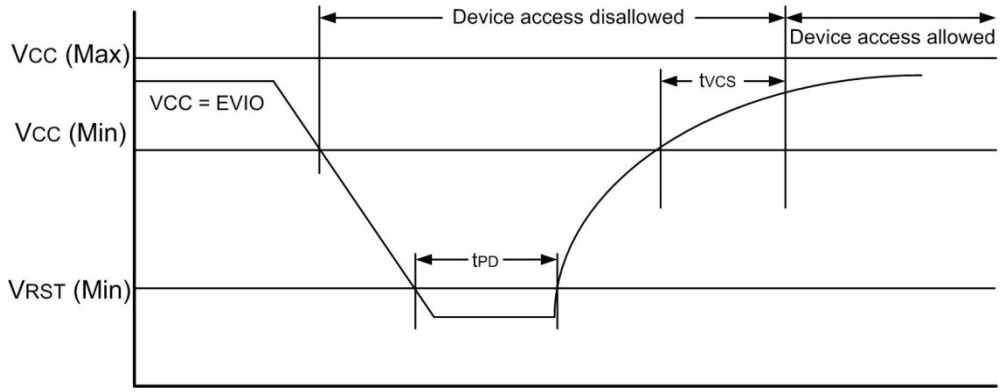


Figure 9-4 Power-down and Voltage Drop



9.3 DC Characteristics

Table 9-3 DC Characteristics

Description	Param	Test Conditions	Min	Type[2]	Max	Unit
Input Load Current	I_{LI}	VIN=VSS to VCC, VCC=VCC max		+0.02	±1.0	µA
Output Leakage Current	I_{LO}	VOUT=VSS to VCC, VCC=VCC max		+0.02	±1.0	µA
VCC Active Read Current	I_{CC1}	#CE=V_{IL}, #OE=V_{IH}, Address switching@ 5 MHz, VCC=VCC max		55	60	mA
VCC Intra-Page Read Current	I_{CC2}	#CE= V_{IL}, #OE= V_{IH}, Address switching@ 33 MHz, VCC=VCC max		9	25	mA
VCC Active Erase/Program Current[1,2]	I_{CC3}	#CE= V_{IL}, #OE= V_{IH}, VCC=VCC max		45	100	mA
VCC Standby Current	I_{CC4}	#CE, #RESET, #OE= V_{IH}, VIH=E_{VIO} V_{IL} =VSS, VCC=VCC max		70	100	µA
VCC Reset Current[2,6]	I_{CC5}	#CE= V_{IH}, #RESET= V_{IL}, VCC=VCC max		10	20	mA
Automatic Sleep Mode[3]	I_{CC6}	V_{IH} =E_{VIO}, V_{IL} =VSS , VCC=VCC max, t_{ACC} + 30 ns		3	6	mA
		V_{IH} =E_{VIO}, V_{IL} =VSS, VCC=VCC max, t_{ASSB}		100	150	µA
VCC Current during power up[2]	I_{CC7}	#RESET=E_{VIO}, #CE=E_{VIO}, #OE=E_{VIO}, VCC=VCC max,		53	80	mA
Input LOW Voltage[4]	V_{IL}		-0.5		0.3xE_{VIO}	V
Input HIGH Voltage[4]	V_{IH}		0.7xE_{VIO}		E_{VIO}+0.4	V
Output LOW Voltage[4,7]	V_{OL}	I_{OL}=100µA for DQ15-DQ0; I_{OL}=2mA for RY/#BY			0.15xE_{VIO}	V
Output HIGH Voltage[4]	V_{OH}	I_{OH}=100µA	0.85xE_{VIO}			V
LOW VCC Power on Reset Voltage[2]	V_{RST}			1.0		V

Notes:

1. I_{CC} active, if there is an internal Algorithm in progress.
2. Not 100% tested.
3. When addresses remain stable for the specified period of time, Automatic sleep mode will enter the lower power mode.
4. E_{VIO} = 1.65V to VCC or 2.7V to VCC.
5. VCC = 3V and E_{VIO} = 3V or 1.8V. When E_{VIO} is at 1.8V, I/O pins cannot operate at >1.8V.
6. If an internal operation is in progress at the beginning of a reset, the current consumption will remain at the internal operation specification until the internal operation is terminated by the reset. If no internal operation is in progress when reset has begun or following the termination of an internal operation, I_{CC7} will draw current during what's left of the t_{RPH} period. At the end of the t_{RPH} period, the device transitions to the standby mode until the next read or write cycle.
7. The RY/#BY suggested pull-up resistor for the output is 5k to 10k Ohms.

9.4 Capacitance Characteristics

Table 9-4 Connector Capacitance for FBGA (LFBGA64) Package

Description	Parameter	Test Setup	Typ	Max	Unit
Input Capacitance	C_{IN}	VIN = 0	8	9	pF
Output Capacitance	C_{OUT}	VOUT = 0	5	7	pF
Control Pin Capacitance	C_{IN2}	VIN = 0	4	8	pF
Output Capacitance	RY/#BY	VOUT = 0	3	4	pF

Notes:
1. Sampled, not 100% tested.
2. Test conditions TA = 25°C, f = 1.0 MHz

Table 9-5 Connector Capacitance for TSOP (TSOP56) Package

Description	Parameter	Test Setup	Typ	Max	Unit
Input Capacitance	C_{IN}	VIN = 0	7	8	pF
Output Capacitance	C_{OUT}	VOUT = 0	5	6	pF
Control Pin Capacitance	C_{IN2}	VIN = 0	3	7	pF
Output Capacitance	RY/#BY	VOUT = 0	3	4	pF

Notes:
1. Sampled, not 100% tested.
2. Test conditions TA = 25°C, f = 1.0 MHz

Table 9-6 Connector Capacitance for TFBGA (TFBGA56) Package

Description	Parameter	Test Setup	Typ	Max	Unit
Input Capacitance	C_{IN}	VIN = 0	7	8	pF
Output Capacitance	C_{OUT}	VOUT = 0	5	6	pF
Control Pin Capacitance	C_{IN2}	VIN = 0	3	7	pF
Output Capacitance	RY/#BY	VOUT = 0	3	4	pF

Notes:
1. Sampled, not 100% tested.
2. Test conditions TA = 25°C, f = 1.0 MHz

10 TIMING SPECIFICATIONS

10.1 AC Test Conditions

Figure 10-1 Device Under Test Setup

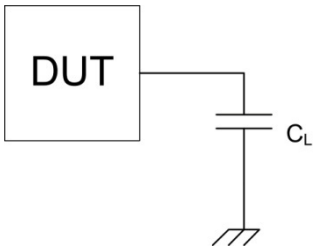


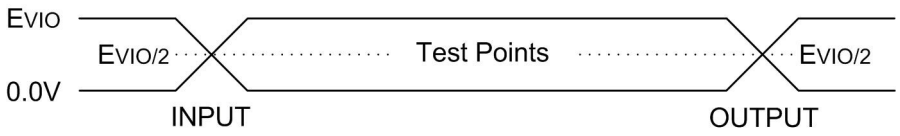
Table 10-1 Test Specification

Parameter Description	All Speeds	Units
Output Load Capacitance, C_L	30	pF
Input Rise and Fall Times[1]	1.5	ns
Input Pulse Levels	0.0-E_{VIO}	V
Input timing measurement reference levels	E_{VIO}/2	V
Output timing measurement reference levels	E_{VIO}/2	V

Note:

1. Measured between V_{IL} max and V_{IH} min.

Figure 10-2 Input Switching Test Waveforms



10.2 Power Up Reset and Hardware Reset

Decoupling the VCC and EVIO power supplies are normal precautions that should be taken. Generally, a suitable capacitor would be on the order of 0.1 µF tied close to the package.

Table 10-2 Power ON and Reset Parameters

Description	Parameter	Limit	Value	Unit
VCC Setup Time to first access[1,2]	tVCS	Min	300	µs
EVIO Setup Time to first access[1,2]	tVIOS	Min	300	µs
#RESET LOW to #CE LOW	tRPH	Min	35	µs
#RESET Pulse Width	tRP	Min	200	ns
Time between #RESET (HIGH) and #CE (LOW)	tRH	Min	50	ns
#CE Pulse Width HIGH	tCEH	Min	20	ns

Notes:

1. Not 100% tested.
2. Timing measured from VCC minimum and EVIO minimum to VIH on Reset and VIL on #CE.
3. #RESET low is possible during Power Up Reset. If RESET is asserted during Power Up Reset, the later period of tRPH, tVIOS, or tVCS will determine when #CE may go LOW. If #RESET stays LOW after tVIOS, or tVCS is fulfilled, tRPH is measured from the end of tVIOS, or tVCS. RESET is required also to be HIGH tRH before #CE goes LOW.
4. During power-up, VCC ≥ (EVIO - 200 mV).
5. The ramp rate for VCC and EVIO can be non-linear.
6. tRPH must be ≤ (tRP + tRH).

10.2.1 Power Up Reset

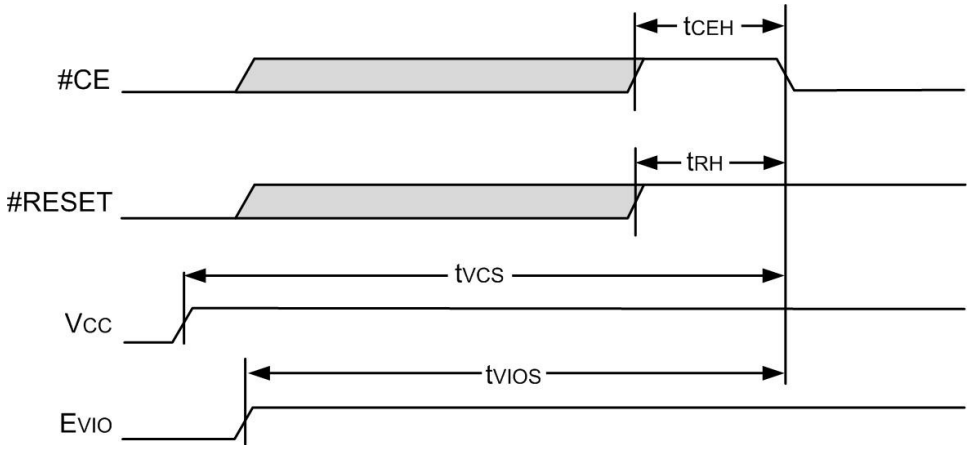
The device will draw ICC7 current during Power-up Reset.

As power supplies voltage ramps up, the EVIO voltage must remain less than or equal to the VCC voltage. VIH also has to be less than or equal to the EVIO voltage.

The Power-up Reset Internal Algorithm requires a period of tVCS to load all of the Write State Controller algorithms and default data from non-volatile memory. All control signals including #CE and #RESET during the Power-up Reset period are ignored. Higher than normal Power Up Reset current during tVCS may occur if #CE is LOW, but the level of #CE will not influence the Power-up Reset Internal Algorithms. For a valid read or write operation, #CE or #OE must transition from HIGH to LOW after the tVCS period. During the period of tVCS, #RESET can be HIGH or LOW. When #RESET is LOW during the period of tVCS, it may stay LOW at the end of tVCS to keep the device in the Hardware Reset mode. The device will go to the Standby mode if #RESET is HIGH at the end of tVCS.

When the power first starts to ramp up and the supply voltage is below VRST, then increases to the operating level minimum, internal device configuration and Hardware reset operations are initiated. The #CE signal level is ignored for the period of the Power Up Reset operation (tVCS or tVIOS). Having #RESET signal LOW during this Power Up Reset period is discretionary. However, if #RESET is asserted LOW during Power up Reset sequence, it must satisfy the Hardware Reset parameters; tRP and tRPH. In that case, the Reset operations will be finished at the later of tVCS, tVIOS or tRPH.

Figure 10-3 Power Up Reset



10.2.2 Hardware Reset

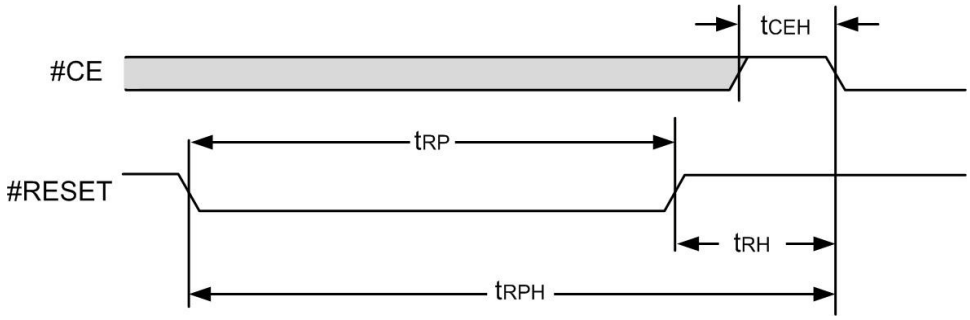
Hardware Reset is initiated by the #RESET signal going to V_{IL}. The device will draw I_{CC7} current during Hardware Reset (t_{RPH}). The device draws CMOS standby current (I_{CC4}), if #RESET is constantly held at V_{SS}, but if #RESET is held at V_{IL} and not V_{SS}, the standby current is higher.

If #RESET is asserted LOW after t_{VCS} and Power-up Reset has not completed, in this case the Power-up #RESET Internal Algorithms will be performed instead and not Hardware #RESET, requiring a period of t_{VCS} to complete.

After the device has completed Power Up Reset and entered the Standby mode, any transition to the Hardware Reset mode will initiate the Hardware Reset Internal Algorithm. A Hardware Reset is considerably shorter than a Power-up Reset (t_{RPH}) to complete. During the Hardware Reset Internal Algorithms, any Internal Algorithm in progress will be terminated and the Write State Controller is returned to its Power Up Reset mode without reloading Write State Controller algorithms from non-volatile memory. When the Hardware Reset Internal Algorithms finishes, the device will remain in the Hardware Reset mode, if #RESET stays LOW. If #RESET returns HIGH, the device will go into the Standby mode. If #RESET is HIGH at the end of the Hardware Reset Internal Algorithms, the device will go into the Standby mode.

If the Power Up Reset cycle was not properly finished by the end of t_{VCS} period, a transition to the Hardware Reset mode will only cause a transition to the Power Up Reset mode and initiate the Power-up Reset Internal Algorithm. This makes sure the device can complete a Power-up Reset sequence even if some portion of the Power Up voltage ramp-up causes the Power Up Reset to not initiate or finish properly. During Power-up or Hardware reset, the RY/#BY pin is LOW as an indicating the device is busy.

Figure 10-4 Hardware Reset



10.3 AC Characteristics

10.3.1 Internal Algorithm Performance Table

Table 10-3 Internal Algorithm Characteristics

Parameter		Type[2]	Max[3]	Unit
Sector Erase Time 128 kbyte[5]		275	1100	ms
Single Word Programming Time[1]		125	400	µs
Buffer Programming Time	2-byte[1]	125	750	µs
	32-byte[1]	160	750	
	64-byte[1]	175	750	
	128byte[1]	198	750	
	256byte[1]	239	750	
	512-byte	340	750	
Effective Write Buffer Program Operation per Word	512-byte	1.33		µs
Sector Programming Time 128 kB (full Buffer Programming)[6]		108	192	ms
Erase Suspend/Erase Resume (t_{ESL})			40	µs
Program Suspend/Program Resume (t_{PSL})			40	µs
Erase Resume to next Erase Suspend (t_{ERS})[7]		100		µs
Program Resume to next Program Suspend (t_{PRS})[7]		100		µs
Blank Check		6.2	8.5	ms
NOP (Number of Program-operations, per Line)			256	

Notes:

1. Not 100% tested.
2. Program and erase typical times presume the following conditions: 25°C, 3.0V VCC, a random data pattern and 10,000 cycles.
3. 90°C, VCC = 2.70V, 100,000 cycles, and a random data pattern are considered under worst case conditions.
4. Specifications are based upon a 512-byte write buffer for Effective write buffer operations.
5. All words are programmed to 0000h before Sector and Chip erasure as part of the pre-programming step of the Internal Erase algorithm.
6. System-level overhead is the time required to execute the bus-cycle sequence for the program command.
7. In order for Program or Erase operations to progress to completion requires the time period to be ≥ typical periods. However, a minimum of 60 ns is required between Resume and Suspend.

10.3.2 Asynchronous Read Operations

Table 10-4 Read Operation E_{VIO} = 1.65V to VCC, VCC = 2.7V to 3.6V

Description			Symbol		VCC=2.7~3.6V			
			ALT	STD	Min	TYP	Max	Unit
Valid Data Output after Address		E_{VIO}=VCC	t_{ACC}	t_{AA}			90	ns
		E_{VIO}=1.65V to VCC					100	ns
Read Period Time		E_{VIO}=VCC		t_{RC}	90			ns
		E_{VIO}=1.65V to VCC			100			ns
Valid data output after #CE Low		E_{VIO}=VCC		t_{CE}			90	ns
		E_{VIO}=1.65V to VCC					100	ns
Page Access Time		E_{VIO}=VCC	t_{PACC}	t_{PA}			15	ns
		E_{VIO}=1.65V to VCC					25	ns
Valid data output after #CE Low		E_{VIO}=VCC		t_{OE}			25	ns
		E_{VIO}=1.65V to VCC					35	ns
Output Hold time from addresses, #CE or #OE, Whichever Occurs First		E_{VIO}=VCC		t_{OH}	0			ns
		E_{VIO}=1.65V to VCC			0			ns
Chip Enable or Output Enable to Output HIZ[1]		E_{VIO}=VCC		t_{DF}			15	ns
		E_{VIO}=1.65V to VCC					20	ns
Output Enable Hold Time[1]	Read	E_{VIO}=VCC		t_{OEH}	0			ns
		E_{VIO}=1.65V to VCC			10			ns
	Toggle and Data# Polling	E_{VIO}=VCC			0			ns
		E_{VIO}=1.65V to VCC			10			ns
Automatic Sleep to Standby time[1]	#CE = V_{IL}, Address stable	E_{VIO}=VCC		t_{ASSB}		5	8	µs
		E_{VIO}=1.65V to VCC				5	8	µs

Note:
1. Not 100% tested.

Figure 10-5 Back to Back Read (tACC) Operation

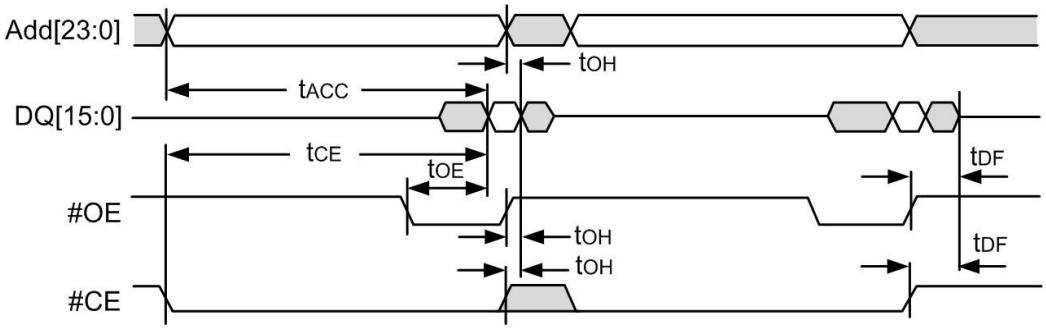
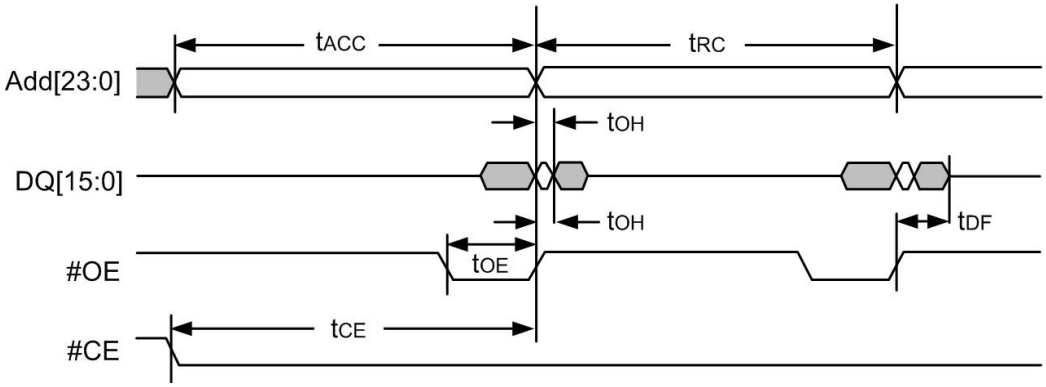
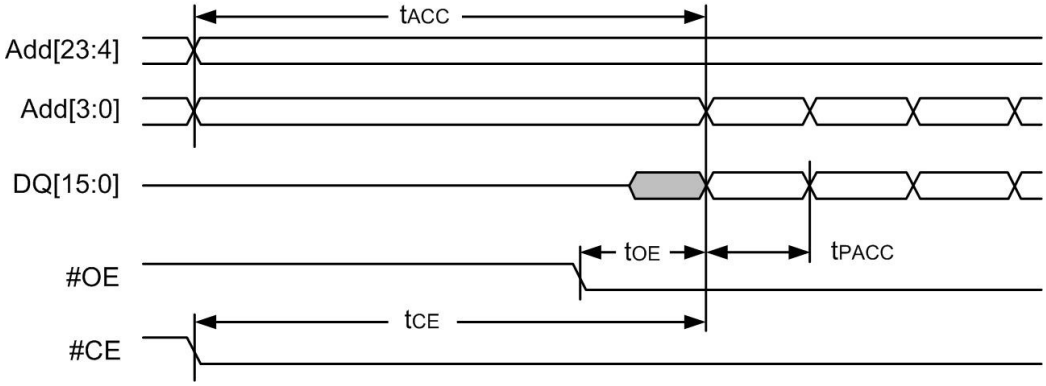


Figure 10-6 Back to Back Read Operation (tRC)



Note:
A back to back operation, in which #CE remains LOW between accesses, requires an address change to initiate the second access.

Figure 10-7 Page Read



Note:
Word Configuration: Toggle A0, A1, A2, and A3.

10.3.3 Asynchronous Write Operations

Table 10-5 Write Operations

Description	Symbols		E_{VIO} = VCC=2.7~3.6V			
	ALT	STD	Min	Typ	Max	Unit
Write Cycle Time [1]		t_{WC}	60			ns
Address Setup Time		t_{AS}	0			ns
Address Setup Time to #OE LOW during toggle bit polling		t_{ASO}	15			ns
Address Hold Time		t_{AH}	45			ns
Address Hold Time From #CE or #OE HIGH during toggle bit polling		t_{AHT}	0			ns
Data Setup Time		t_{DS}	30			ns
Data Hold Time		t_{DH}	0			ns
Output Enable HIGH during toggle bit polling or following status register read.		t_{OEPH}	20			ns
Read Recovery Time Before Write (#OE HIGH to #WE LOW)		t_{GHWL}	0			ns
#CE Setup Time		t_{CS}	0			ns
#CE Hold Time		t_{CH}	0			ns
#WE Pulse Width		t_{WP}	25			ns
#WE Pulse Width HIGH		t_{WPH}	20			ns

Note:
1. Not 100% tested.

Figure 10-8 Back to Back Write Operation

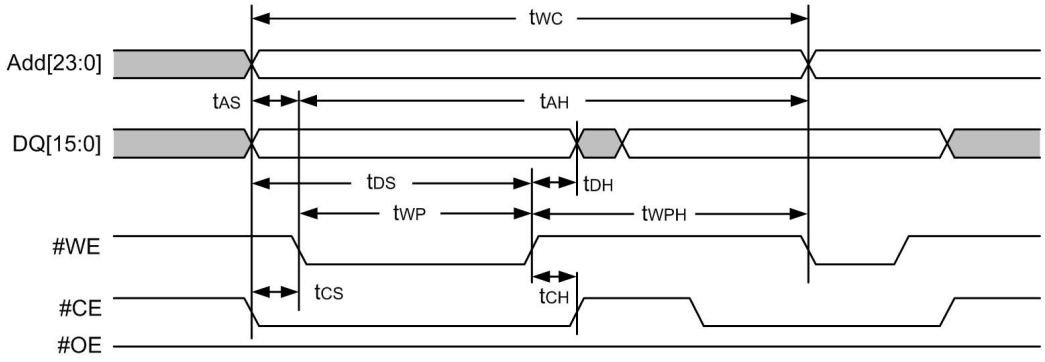


Figure 10-9 Back to Back (#CE VIL) Write Operation

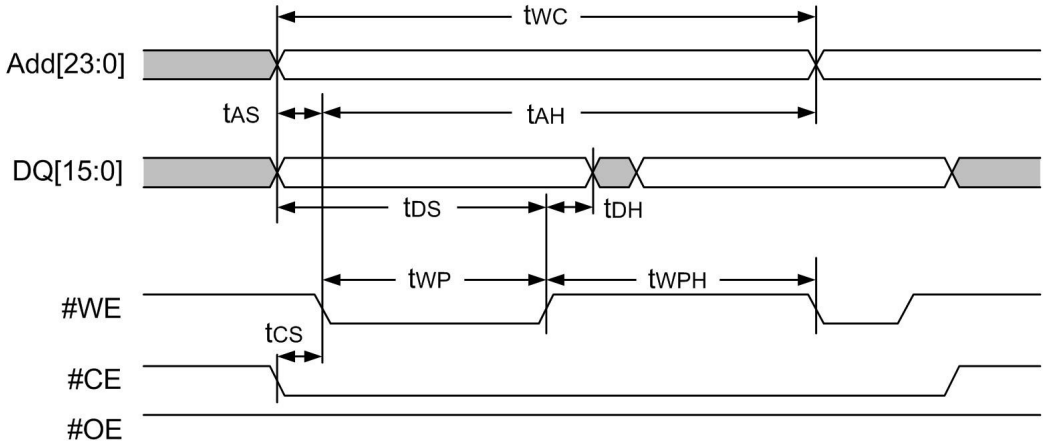


Figure 10-10 Write to Read (tACC) Operation

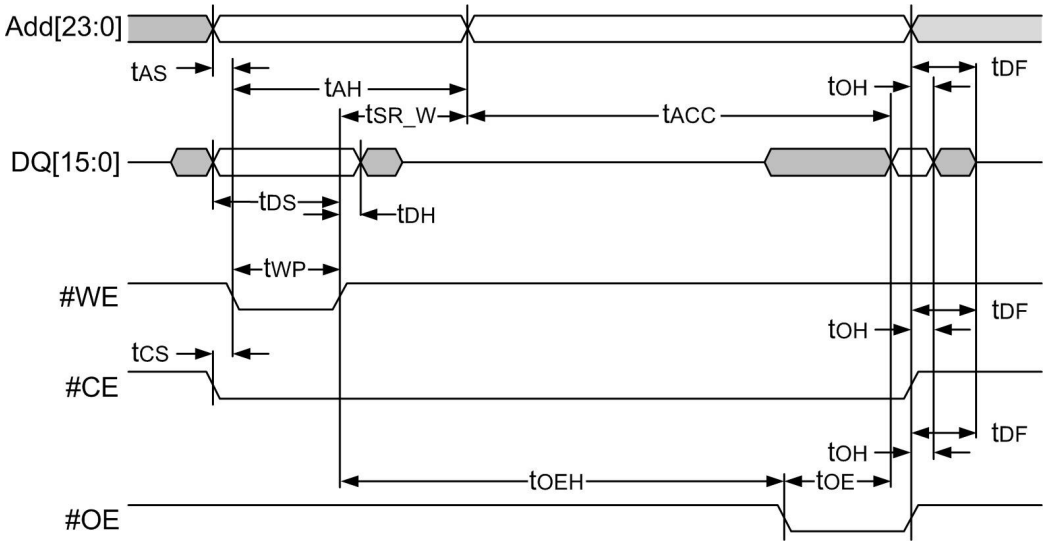


Figure 10-11 Write to Read (tCE) Operation

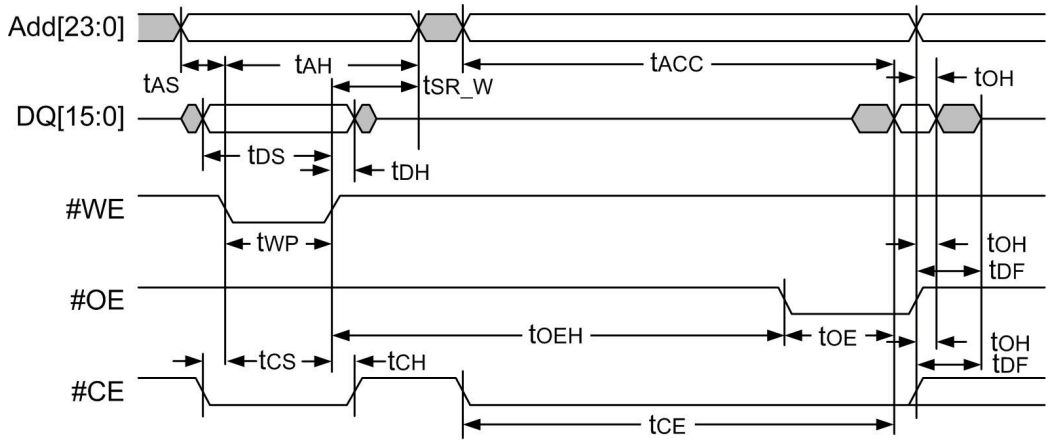


Figure 10-12 Read to Write (#CE VIL) Operation

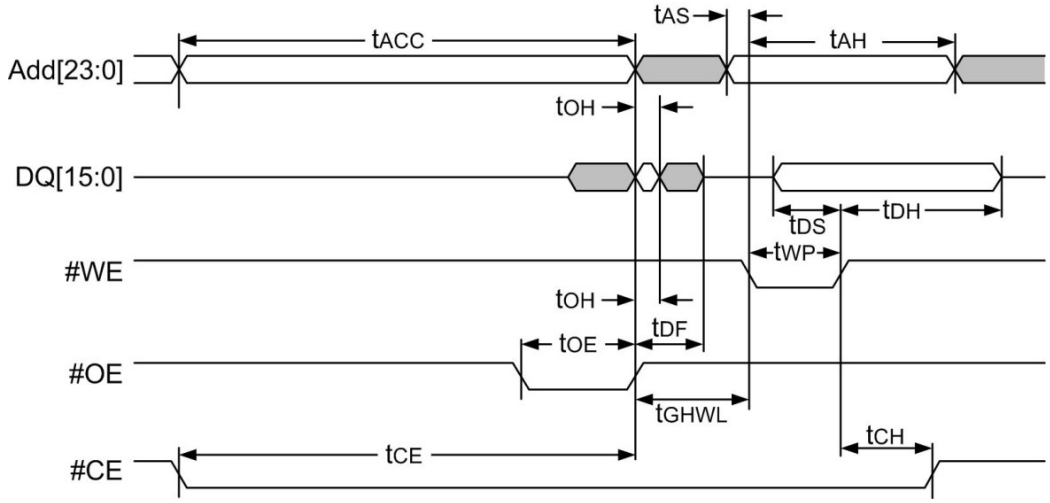


Figure 10-13 Read to Write (#CE Toggle) Operation

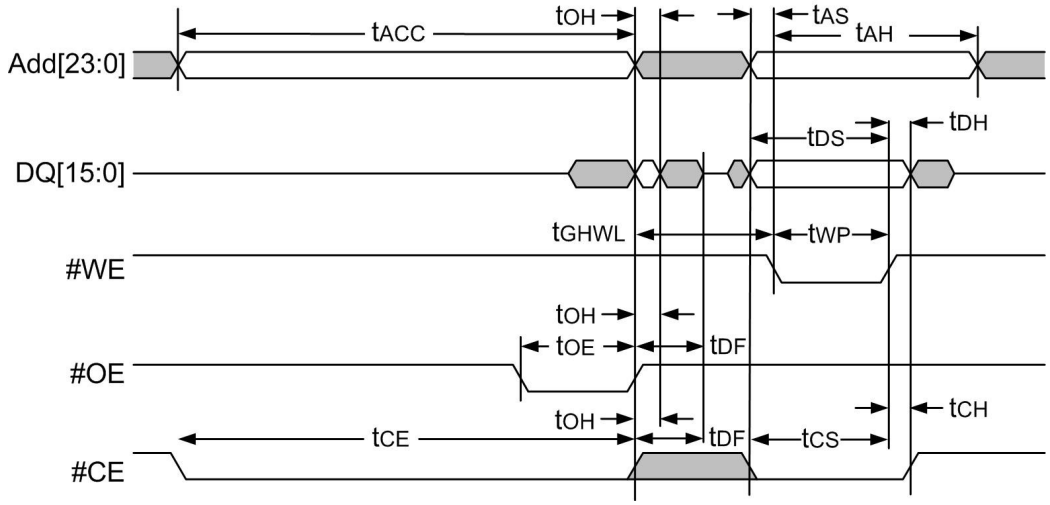


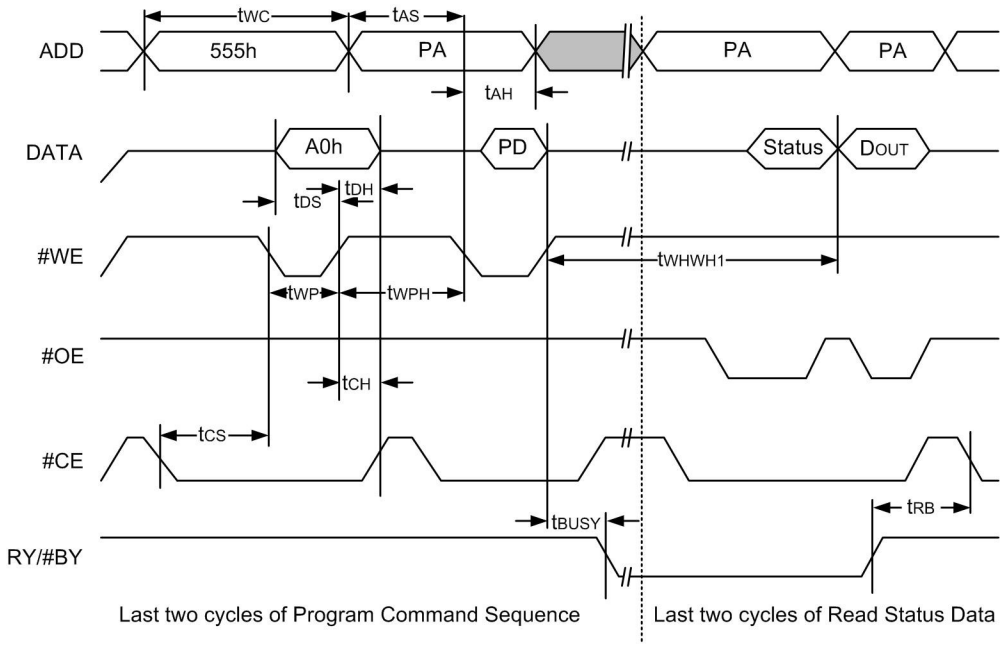
Table 10-6 Erase/Program Operations

Description	SYMBOL		E_{VIO} = VCC=2.7~3.6V			
	ALT	STD	Min	Typ	Max	Unit
Write Buffer Program Operation (512-byte)		t_{WHWH1}[5]		340	750	µs
Effective Write Buffer Program Operation per Word[2, 3]				5.2		µs
Program Operation per Word				125	400	µs
Sector Erase Operation[1]		t_{WHWH2}		200		ms
Erase/Program Valid to RY/#BY Delay		t_{BUSY}			80	ns
Latency between Read and Write operations[4]		t_{SR_W}	30			ns
Erase Suspend Latency		t_{ESL}			40	µs
Program Suspend Latency		t_{PSL}			40	µs
RY/#BY Recovery Time		t_{RB}	0			µs

Notes:

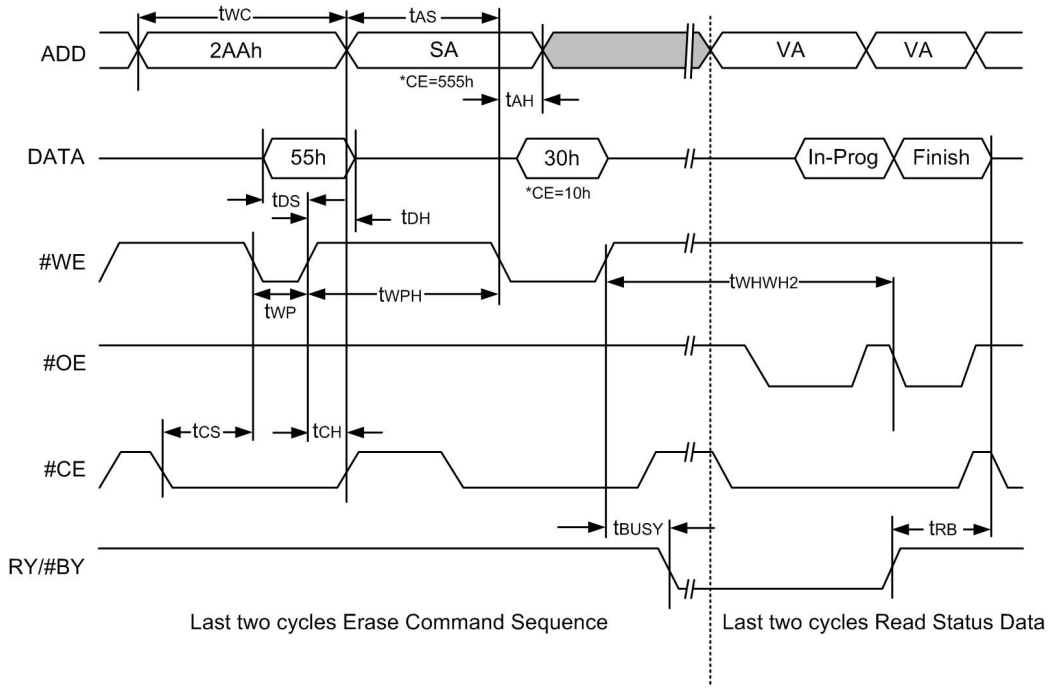
1. Not 100% tested.
2. For one 512bytes programmed.
3. Effective write buffer specification is based upon a 256-word write buffer operation
4. Upon the rising edge of #WE, must wait t_{SR_W} before switching to another address.
5. See Internal Algorithm Characteristics table for specific values

Figure 10-14 Program Operation



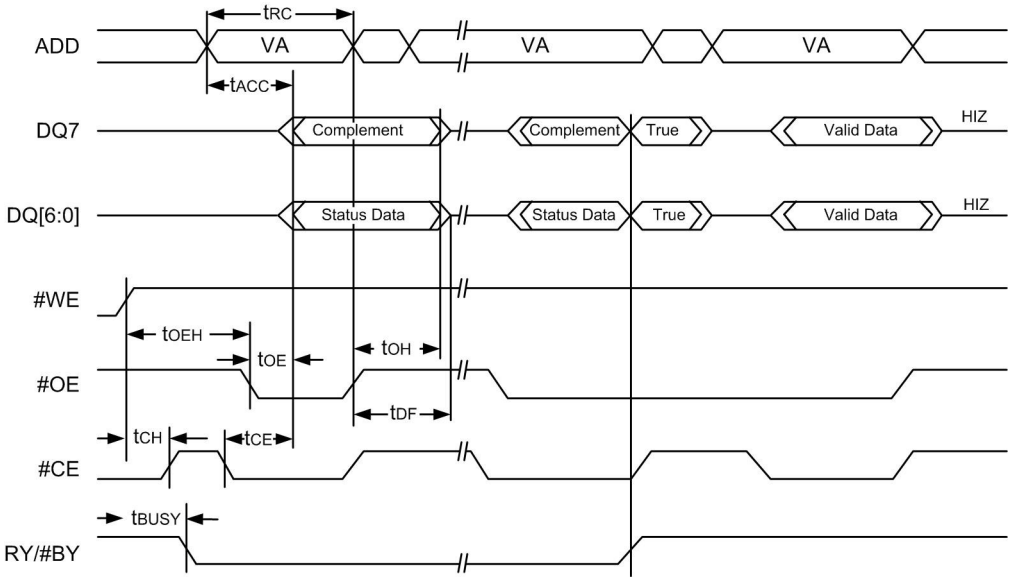
Note:
PA = program address, PD = program data, DOUT is the true data at the program address.

Figure 10-15 Chip/Sector Erase Operation



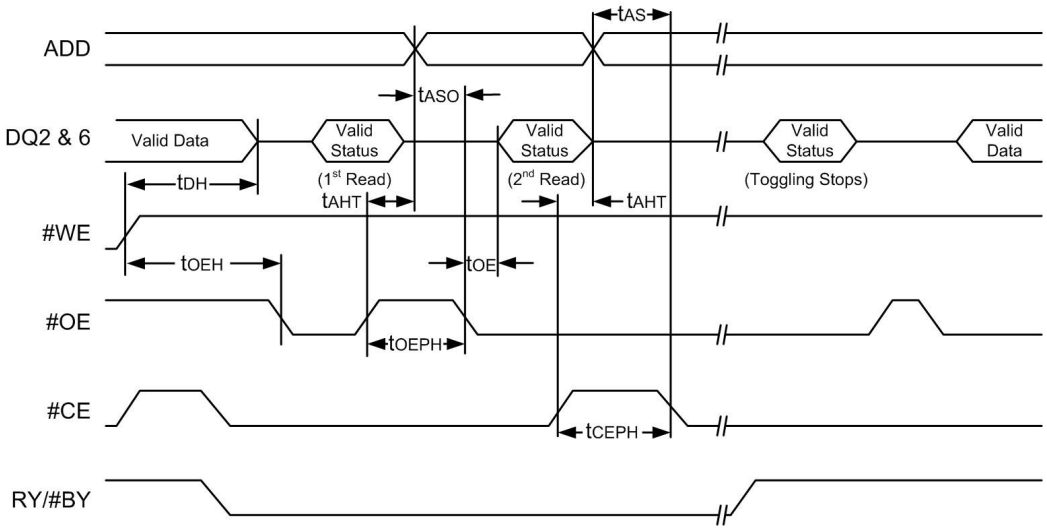
Note:
SA = sector address (for sector erase), VA = valid address for reading status data.

Figure 10-16 Data# Polling (During Internal Algorithms)



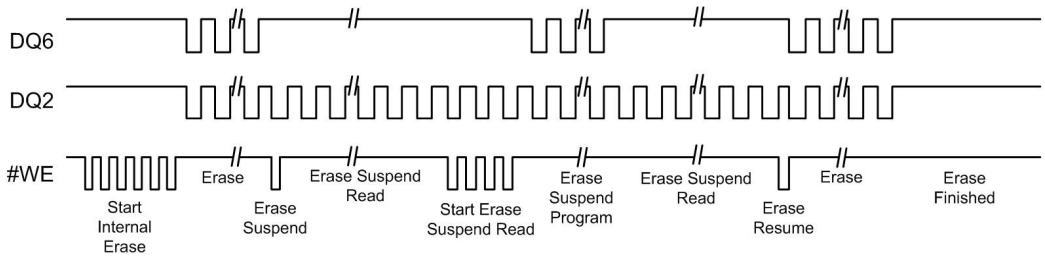
Note:
VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.

Figure 10-17 Toggle Bit (During Internal Algorithms)



Note:
DQ6 will toggle at any read address while the device is busy. DQ2 will toggle if the address is within the actively erasing sector.

Figure 10-18 DQ2 vs. DQ6 Comparison Timing



Note:
The system may use #OE or #CE to toggle DQ2 and DQ6. DQ2 toggles only when read at an address within the erase-suspended sector.

10.3.4 Alternate #CE Controlled Write Operations

Table 10-7 Alternate #CE Controlled Write Operations

Description	SYMBOL		E_{VIO} = VCC=2.7~3.6V			
	ALT	STD	Min	Typ	Max	Unit
Write Cycle Time[1]		t_{WC}	60			ns
Address Setup Time		t_{AS}	0			ns
Address Setup Time to #OE LOW during toggle bit polling		t_{ASO}	15			ns
Address Hold Time		t_{AH}	45			ns
Address Hold Time From #CE or #OE HIGH during toggle bit polling		t_{AHT}	0			ns
Data Setup Time		t_{DS}	30			ns
Data Hold Time		t_{DH}	0			ns
#CE HIGH during toggle bit polling		t_{CEPH}	20			ns
#OE HIGH during toggle bit polling		t_{OEPH}	20			ns
Read Recovery Time Before Write (#OE HIGH to #WE LOW)		t_{GHEL}	0			ns
#WE Setup Time		t_{WS}	0			ns
#WE Hold Time		t_{WH}	0			ns
#CE Pulse Width		t_{CP}	25			ns
#CE Pulse Width HIGH		t_{CPH}	20			ns

Note:
1. Not 100% tested.

Figure 10-19 Back to Back (#CE) Write Operation

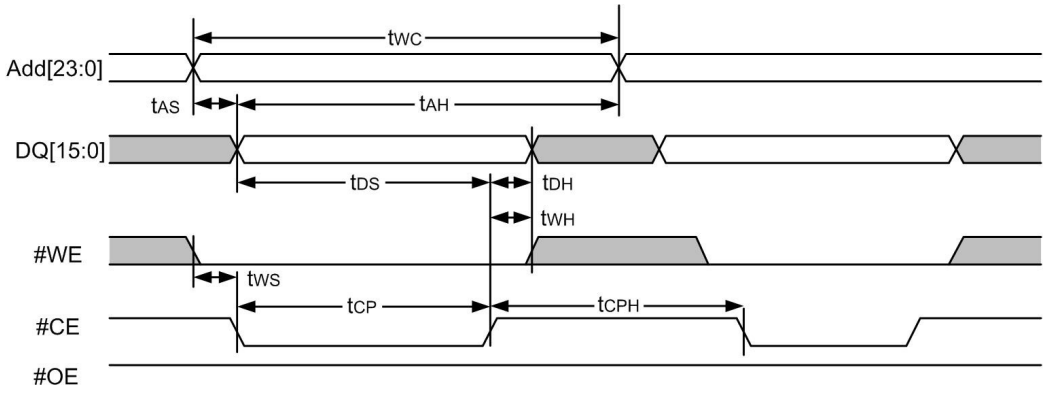
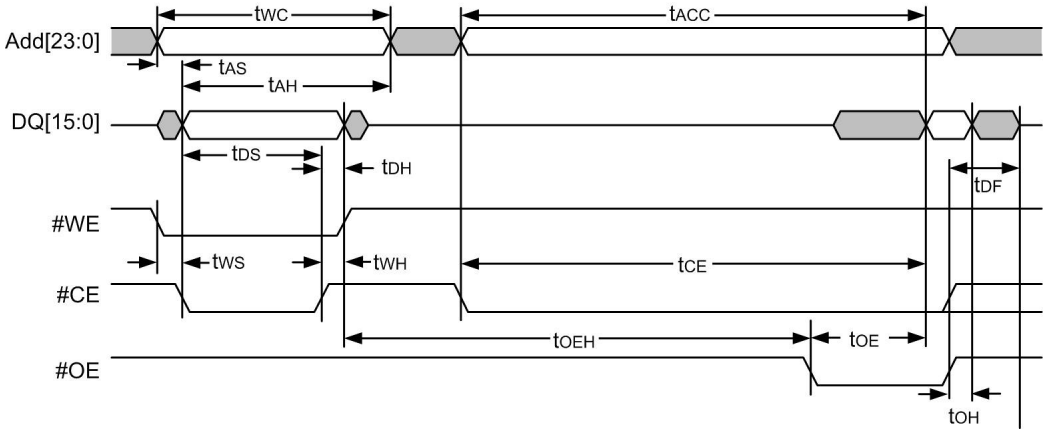


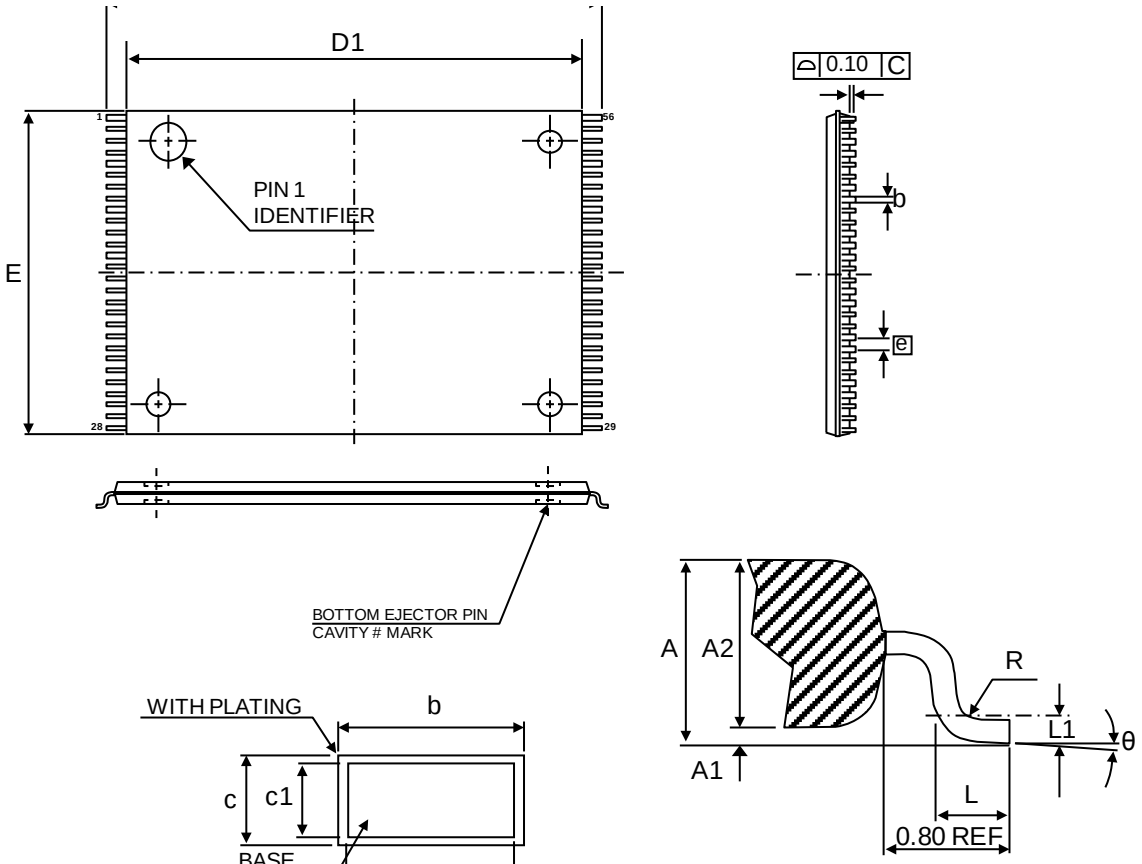
Figure 10-20 (#CE) Write to Read Operation



11 PACKAGE DIMENSIONS

11.1 TSOP 56-pin 14x20mm

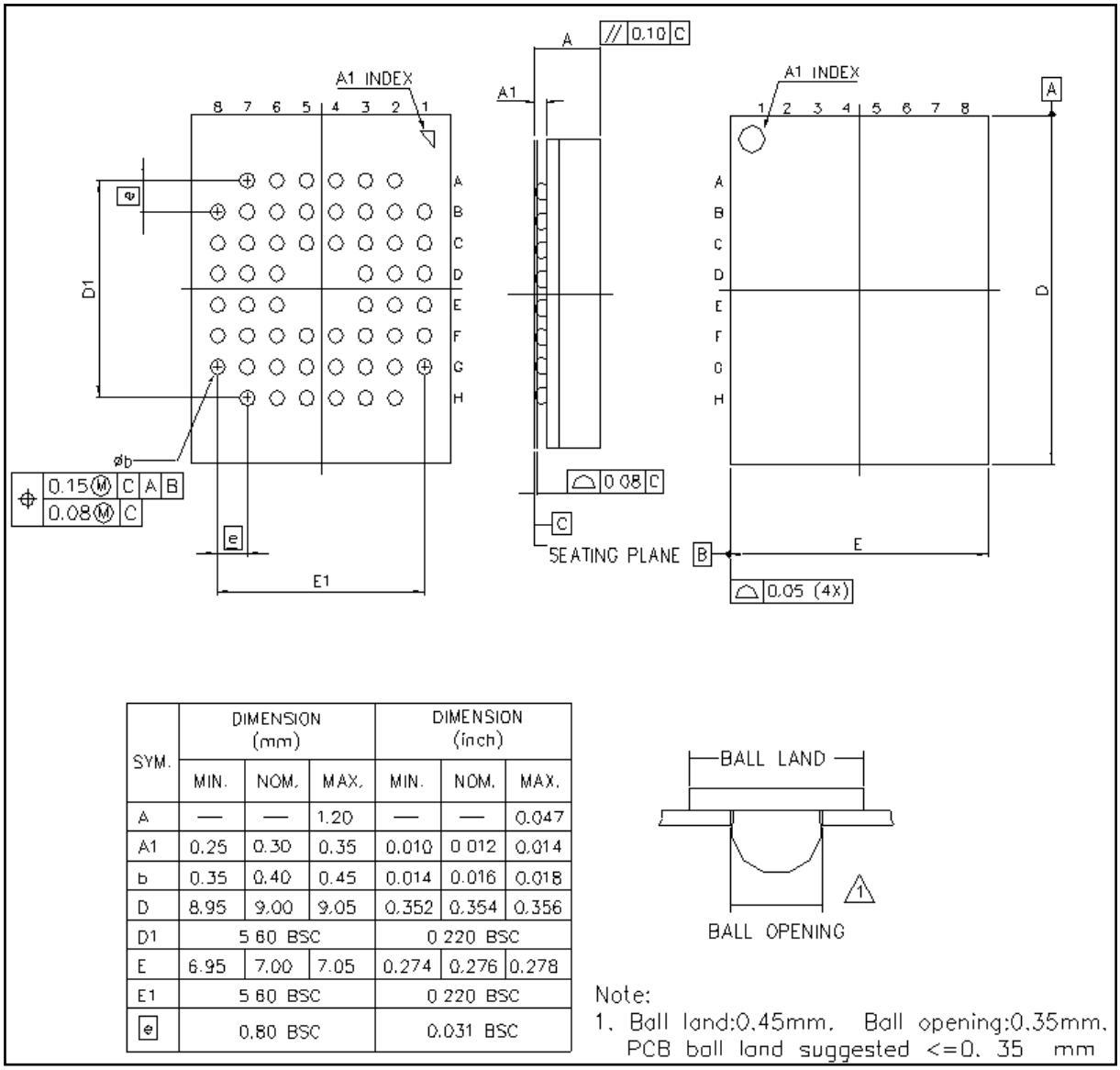
Figure 11-1 TSOP 56-pin 14x20mm Package



Symbol	Dimension in MM			Dimension Inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.2	-	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.17	0.22	0.27	0.007	0.009	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.10	-	0.21	0.004	-	0.008
c1	0.10	0.13	0.16	0.004	0.005	0.006
D	20.00 BSC			0.787 BSC		
D1	18.40 BSC			0.724 BSC		
E	14.00 BSC			0.551 BSC		
L	0.50	0.60	0.70	0.020	0.024	0.028
L1	0.25 BSC			0.010 BSC		
e	0.5 BSC			0.020 BSC		
R	0.08	-	0.35	0.003	-	0.008
θ	0°	-	8°	0°	-	8°

11.2 Thin & Fine-Pitch Ball Grid Array, 56 ball, 7x9mm (TFBGA56)

Figure 11-2 TFBGA-56, 7x9mm package

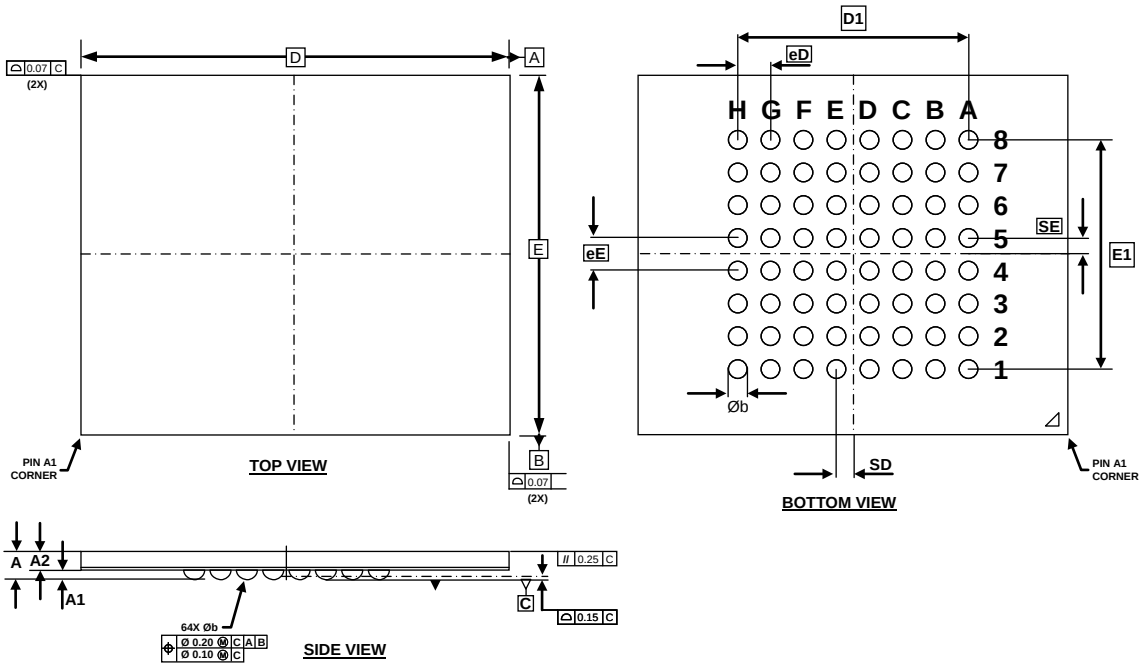


SYM.	DIMENSION (mm)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.25	0.30	0.35	0.010	0.012	0.014
b	0.35	0.40	0.45	0.014	0.016	0.018
D	8.95	9.00	9.05	0.352	0.354	0.356
D1	5.60 BSC			0.220 BSC		
E	6.95	7.00	7.05	0.274	0.276	0.278
E1	5.60 BSC			0.220 BSC		
e	0.80 BSC			0.031 BSC		

Note:
1. Ball land:0.45mm. Ball opening:0.35mm, PCB ball land suggested <=0.35 mm

11.3 Low-Profile Fine-Pitch Ball Grid Array, 64-ball 11x13mm (LFBA64)

Figure 11-3 LFBGA 64-ball 11x13mm Package

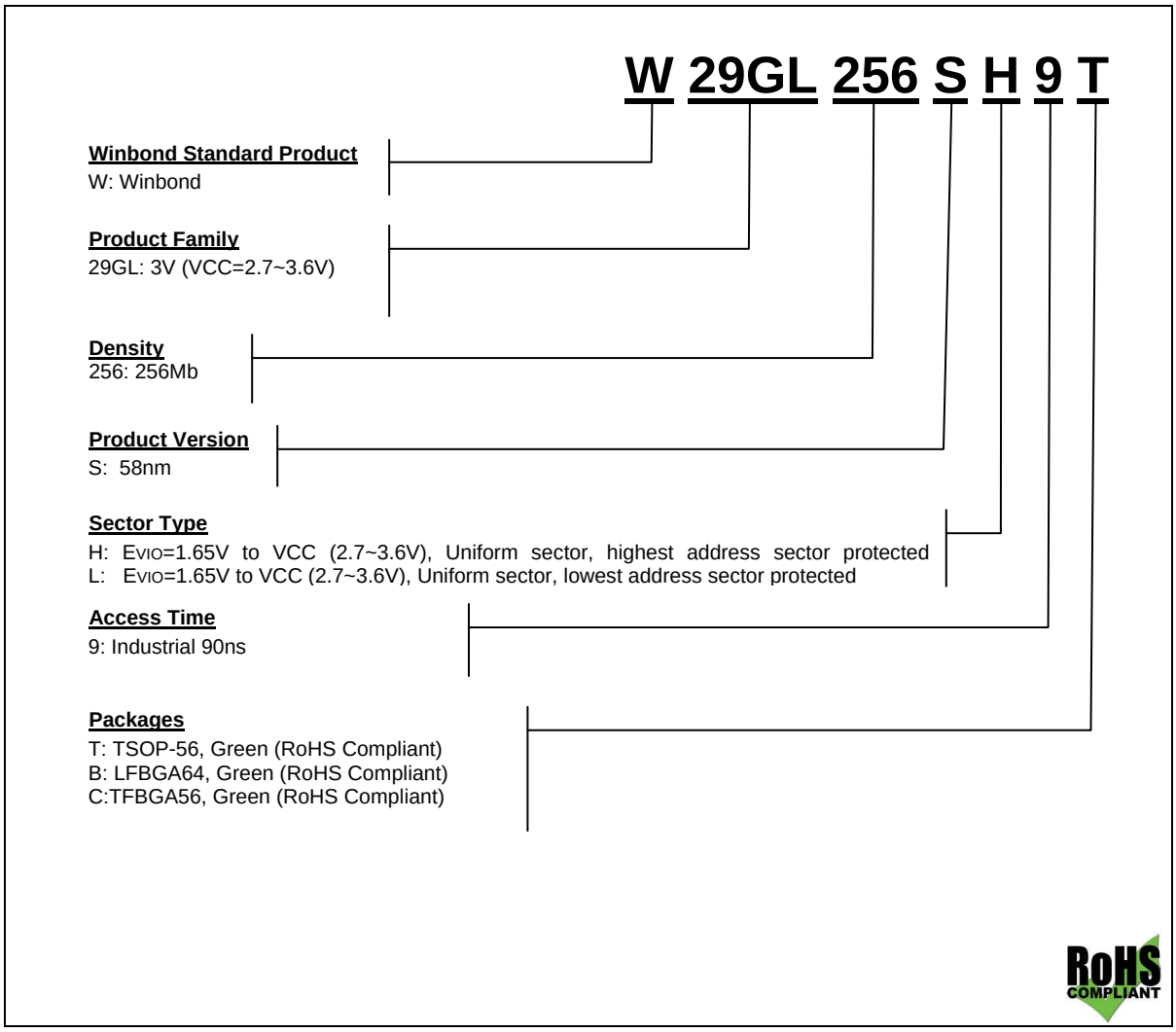


SYMBOL	DIMENSION (MM)			NOTE
	MIN	NOM	MAX	
A	-	-	1.40	PROFILE
A1	0.40		-	BALL HEIGHT
A2	0.60		-	BODY THICKNESS
D	13.00 BSC			BODY SIZE
E	11.00 BSC			BODY SIZE
D1	7.00 BSC			MATRIX FOOTPRINT
E1	7.00 BSC			MATRIX FOOTPRINT
n	64			BALL COUNT
Øb	0.5	0.6	0.7	BALL DIAMETER
eE	1.00 BSC			BALL PITCH
eD	1.00 BSC			BALL PITCH
SD/SE	0.50 BSC			SOLDER BALL PLACEMENT
	NONE			DEPOPULATED SOLDER BALLS

12 ORDERING INFORMATION

12.1 Ordering Part Number Definitions

Figure 12-1 Ordering Part Numbering



Notes:
1. Winbond reserves the right to make changes to its products without prior notice.
2. Contact Winbond Sales for Secured Sector Lock Options.
3. For more details on Product Version's Temperature Ranges, contact Winbond.

12.2 Valid Part Numbers and Top Side Marking

The following table provides the valid part numbers for the W29GL256S Parallel Flash Memory. Please contact Winbond for specific availability by density and package type. Winbond Parallel memories use a 12-digit Product Number for ordering.

Table 12-1 Valid Part Numbers and Markings

PACKAGE TYPE	DENSITY	PRODUCT NUMBER	TOP SIDE MARKING
TSOP-56	256Mb	W29GL256SH9T	W29GL256SH9T
TSOP-56	256Mb	W29GL256SL9T	W29GL256SL9T
TFBGA56	256Mb	W29GL256SH9C	W29GL256SH9C
TFBGA56	256Mb	W29GL256SL9C	W29GL256SL9C
LFBGA64	256Mb	W29GL256SH9B	W29GL256SH9B
LFBGA64	256Mb	W29GL256SL9B	W29GL256SL9B

13 HISTORY

Table 13-1 Revision History

VERSION	DATE	PAGE	DESCRIPTION
A	05-10-2013	-	Preliminary Release

Preliminary Designation

The "*Preliminary*" designation on a *Winbond* datasheet indicates that the product is not full characterized. The specifications are subject to change and are not guaranteed. *Winbond* or an authorized sales representative should be consulted for current information before using this product.

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