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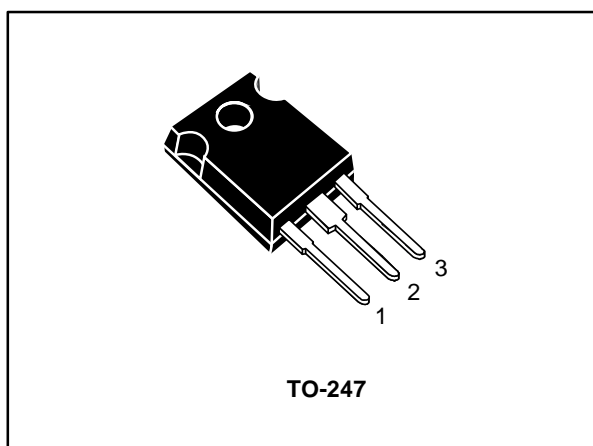
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STW48N60M2

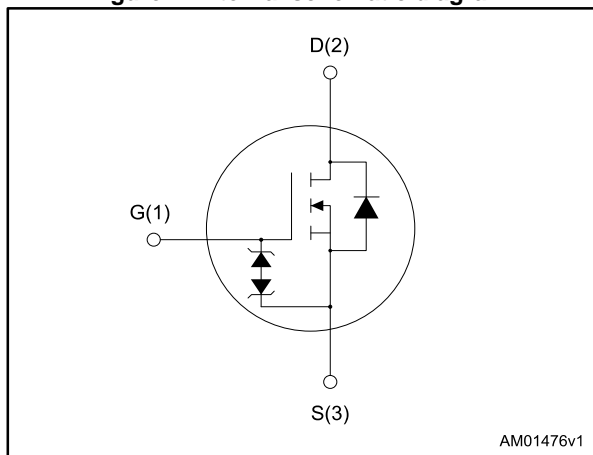
N-channel 600 V, 0.06 Ω typ., 42 A MDmesh™ M2 Power MOSFET in a TO-247 package

Datasheet - production data



TO-247

Figure 1: Internal schematic diagram



Features

| Order code | V _{DS} @ T _{Jmax} | R _{DS(on)} max | I _D |
|------------|-------------------------------------|-------------------------|----------------|
| STW48N60M2 | 650 V | 0.07 Ω | 42 A |

- Extremely low gate charge
- Excellent output capacitance (C_{oss}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

Table 1: Device summary

| Order code | Marking | Package | Packaging |
|------------|---------|---------|-----------|
| STW48N60M2 | 48N60M2 | TO-247 | Tube |

Contents

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1 Electrical ratings

Table 2: Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|--------------------------------|---|-------------|------|
| V _{GS} | Gate-source voltage | ± 25 | V |
| I _D | Drain current (continuous) at T _C = 25 °C | 42 | A |
| I _D | Drain current (continuous) at T _C = 100 °C | 26 | A |
| I _{DM} ⁽¹⁾ | Drain current (pulsed) | 168 | A |
| P _{TOT} | Total dissipation at T _C = 25 °C | 300 | W |
| dv/dt ⁽²⁾ | Peak diode recovery voltage slope | 15 | V/ns |
| dv/dt ⁽³⁾ | MOSFET dv/dt ruggedness | 50 | V/ns |
| T _{stg} | Storage temperature | - 55 to 150 | °C |
| T _j | Max. operating junction temperature | | |

Notes:

(1)Pulse width limited by safe operating area.

(2)I_{SD} ≤ 42 A, di/dt ≤ 400 A/μs; V_{DSpeak} < V_{(BR)DSS}, V_{DD}=400 V.

(3)V_{DS} ≤ 480 V

Table 3: Thermal data

| Symbol | Parameter | Value | Unit |
|-----------------------|---|-------|------|
| R _{thj-case} | Thermal resistance junction-case max | 0.42 | °C/W |
| R _{thj-amb} | Thermal resistance junction-ambient max | 50 | °C/W |

Table 4: Avalanche characteristics

| Symbol | Parameter | Value | Unit |
|-----------------|---|-------|------|
| I _{AR} | Avalanche current, repetitive or not repetitive (pulse width limited by T _{jmax}) | 7 | A |
| E _{AS} | Single pulse avalanche energy (starting T _j =25°C, I _D = I _{AR} ; V _{DD} =50) | 4500 | mJ |

Electrical characteristics

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2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5: On /off states

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------------|-----------------------------------|---|------|------|------|------|
| V _{(BR)DSS} | Drain-source breakdown voltage | V _{GS} = 0, I _D = 1 mA | 600 | | | V |
| I _{DSS} | Zero gate voltage drain current | V _{GS} = 0, V _{DS} = 600 V | | | 1 | μA |
| | | V _{GS} = 0, V _{DS} = 600 V, T _C = 125 °C | | | 100 | μA |
| I _{GSS} | Gate-body leakage current | V _{DS} = 0, V _{GS} = ± 25 V | | | ±10 | μA |
| V _{GS(th)} | Gate threshold voltage | V _{DS} = V _{GS} , I _D = 250 μA | 2 | 3 | 4 | V |
| R _{DS(on)} | Static drain-source on-resistance | V _{GS} = 10 V, I _D = 21 A | | 0.06 | 0.07 | Ω |

Table 6: Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------------------|-------------------------------|---|------|------|------|------|
| C _{iss} | Input capacitance | V _{GS} = 0, V _{DS} = 100 V, f = 1 MHz, | - | 3060 | - | pF |
| C _{oss} | Output capacitance | | - | 143 | - | pF |
| C _{rss} | Reverse transfer capacitance | | - | 4.3 | - | pF |
| C _{oss eq. (1)} | Equivalent output capacitance | V _{GS} = 0, V _{DS} = 0 to 480 V | - | 630 | - | pF |
| R _G | Intrinsic gate resistance | f = 1 MHz, I _D = 0 | - | 4.6 | - | Ω |
| Q _g | Total gate charge | V _{DD} = 480 V, I _D = 42 A, V _{GS} = 10 V (see Figure 15: "Gate charge test circuit") | - | 70 | - | nC |
| Q _{gs} | Gate-source charge | | - | 10.5 | - | nC |
| Q _{gd} | Gate-drain charge | | - | 31 | - | nC |

Notes:

(1)C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7: Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------------|---------------------|--|------|------|------|------|
| t _{d(on)} | Turn-on delay time | V _{DD} = 300 V, I _D = 21 A, R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 14: "Switching times test circuit for resistive load") | - | 18.5 | - | ns |
| t _r | Rise time | | - | 17 | - | ns |
| t _{d(off)} | Turn-off-delay time | | - | 13 | - | ns |
| t _f | Fall time | | - | 119 | - | ns |

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Electrical characteristics

Table 8: Source drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|---|------|------|------|---------------|
| I_{SD} | Source-drain current | | - | | 42 | A |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) | | - | | 168 | A |
| $V_{SD}^{(2)}$ | Forward on voltage | $V_{GS} = 0, I_{SD} = 21 \text{ A}$ | - | | 1.6 | V |
| t_{rr} | Reverse recovery time | $I_{SD} = 42 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ (see <i>Figure 17: "Unclamped inductive load test circuit"</i>) | - | 487 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 9.1 | | μC |
| I_{RRM} | Reverse recovery current | | - | 37.5 | | A |
| t_{rr} | Reverse recovery time | $I_{SD} = 42 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}, T_j = 150 \text{ }^\circ\text{C}$ (see <i>Figure 17: "Unclamped inductive load test circuit"</i>) | - | 605 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 12.5 | | μC |
| I_{RRM} | Reverse recovery current | | - | 41.5 | | A |

Notes:

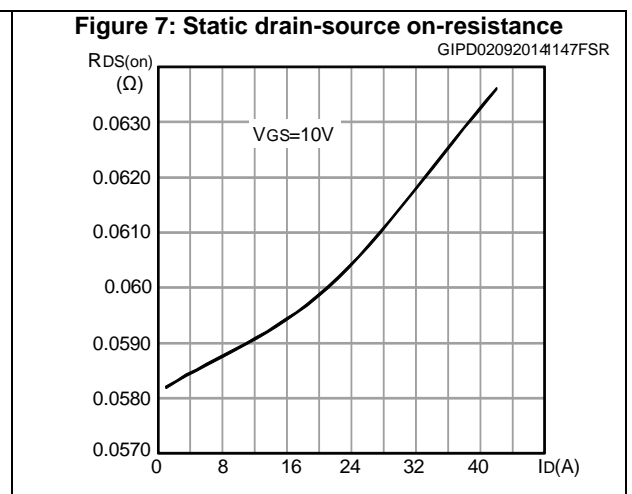
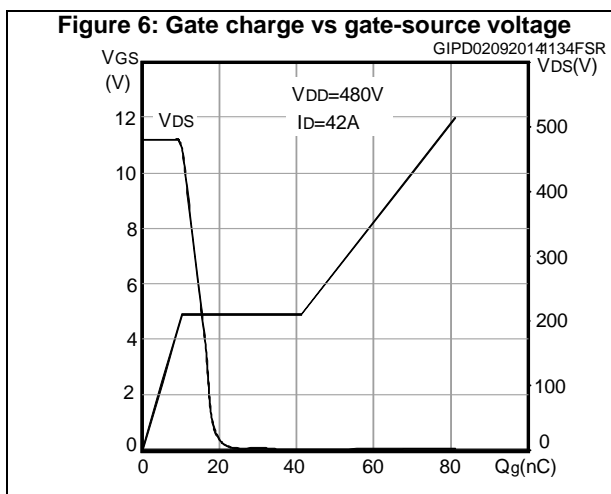
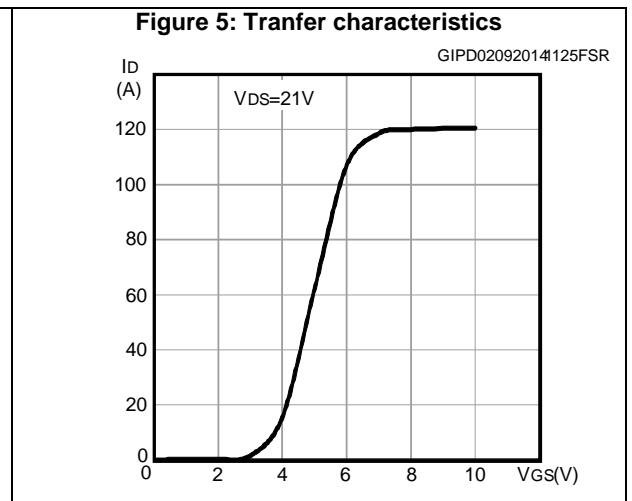
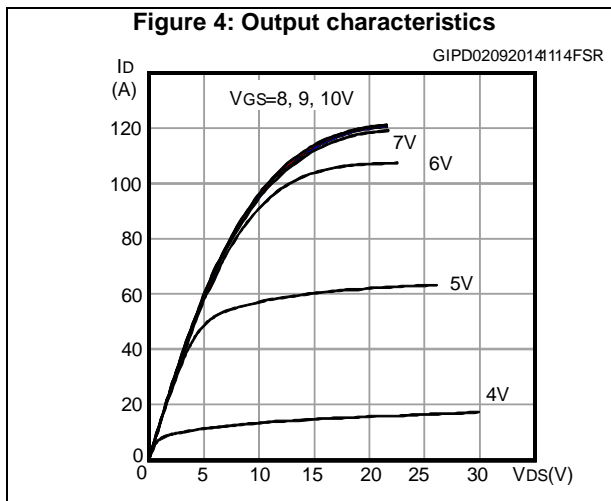
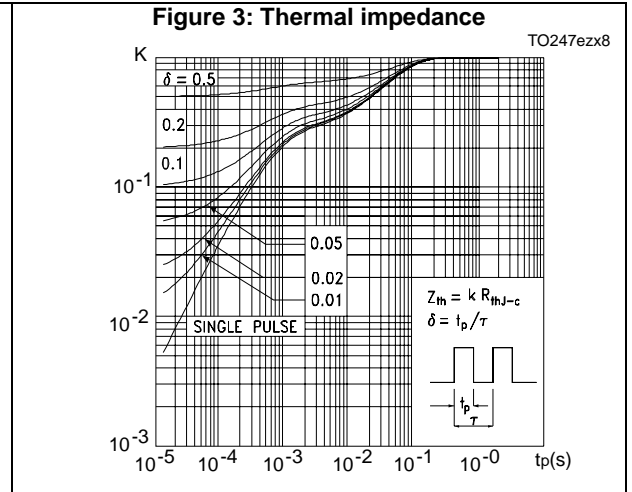
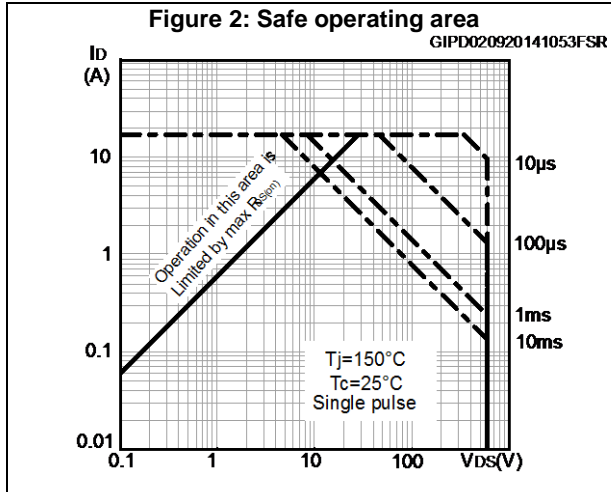
(1)Pulse width limited by safe operating area.

(2)Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Electrical characteristics

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2.1 Electrical characteristics (curves)



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Electrical characteristics

Figure 8: Capacitance variations

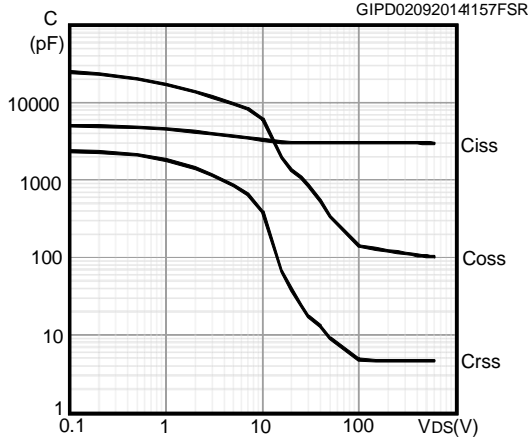


Figure 9: Output capacitance stored energy

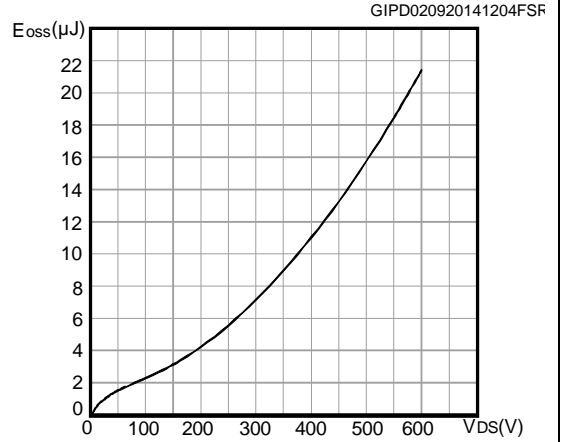


Figure 10: Normalized gate threshold voltage vs temperature

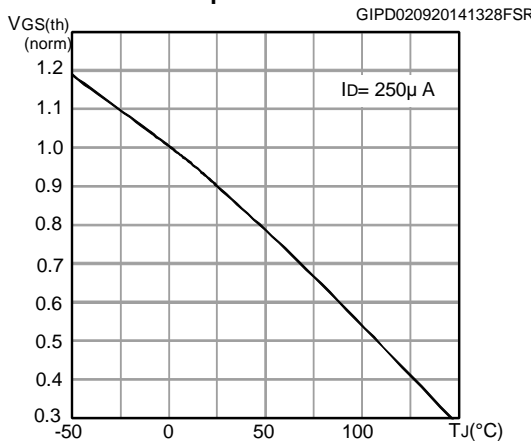


Figure 11: Normalized on-resistance vs temperature

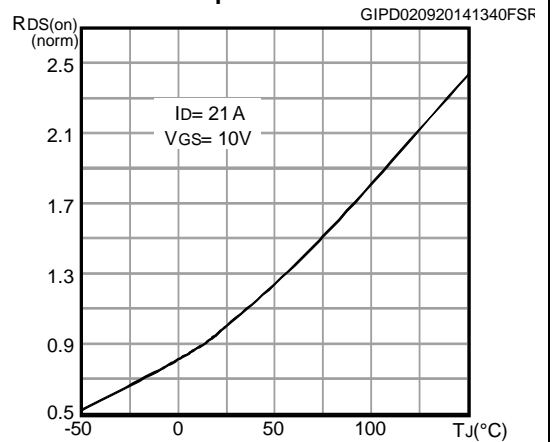


Figure 12: Normalized V(BR)DSS vs temperature

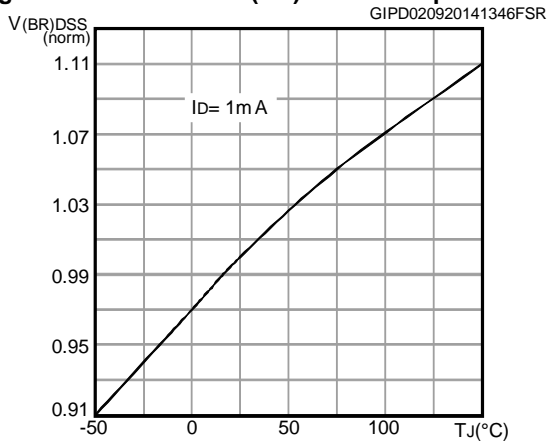
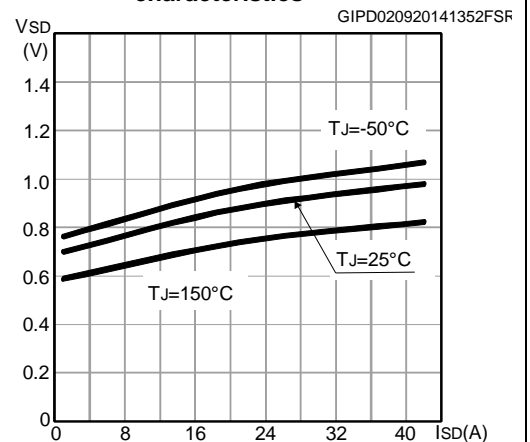


Figure 13: Source-drain diode forward characteristics

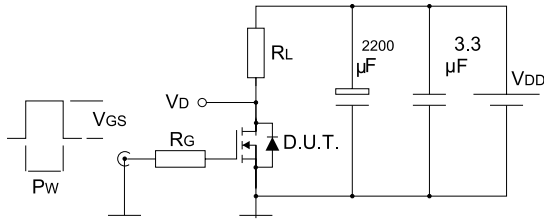


Test circuits

STW48N60M2

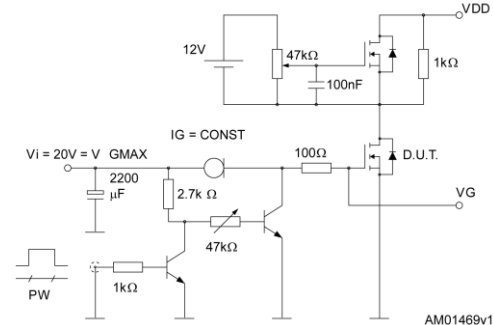
3 Test circuits

Figure 14: Switching times test circuit for resistive load



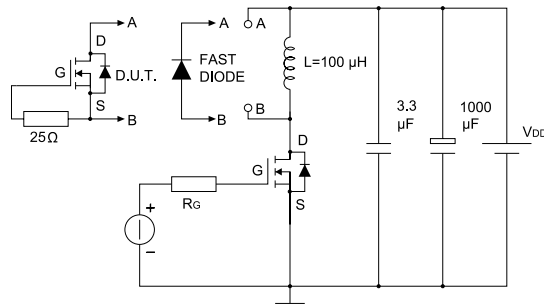
AM01468v1

Figure 15: Gate charge test circuit



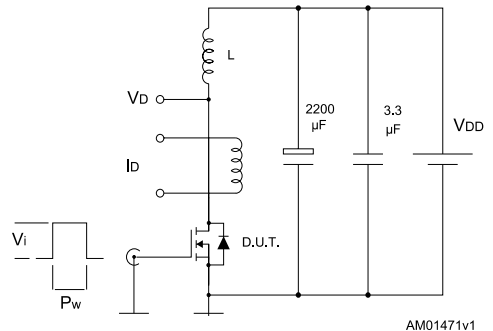
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Figure 16: Test circuit for inductive load switching and diode recovery times



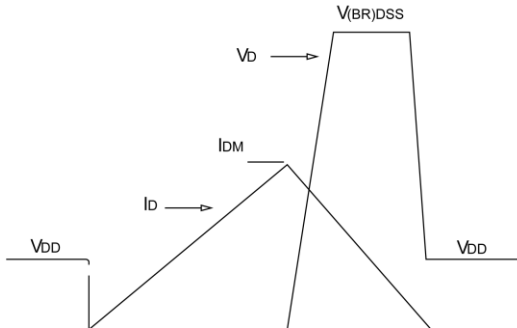
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Figure 17: Unclamped inductive load test circuit



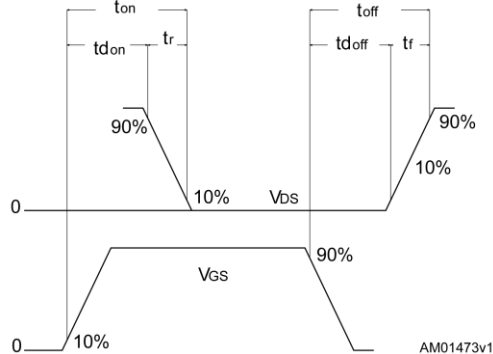
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Figure 18: Unclamped inductive waveform



AM01472v1

Figure 19: Switching time waveform



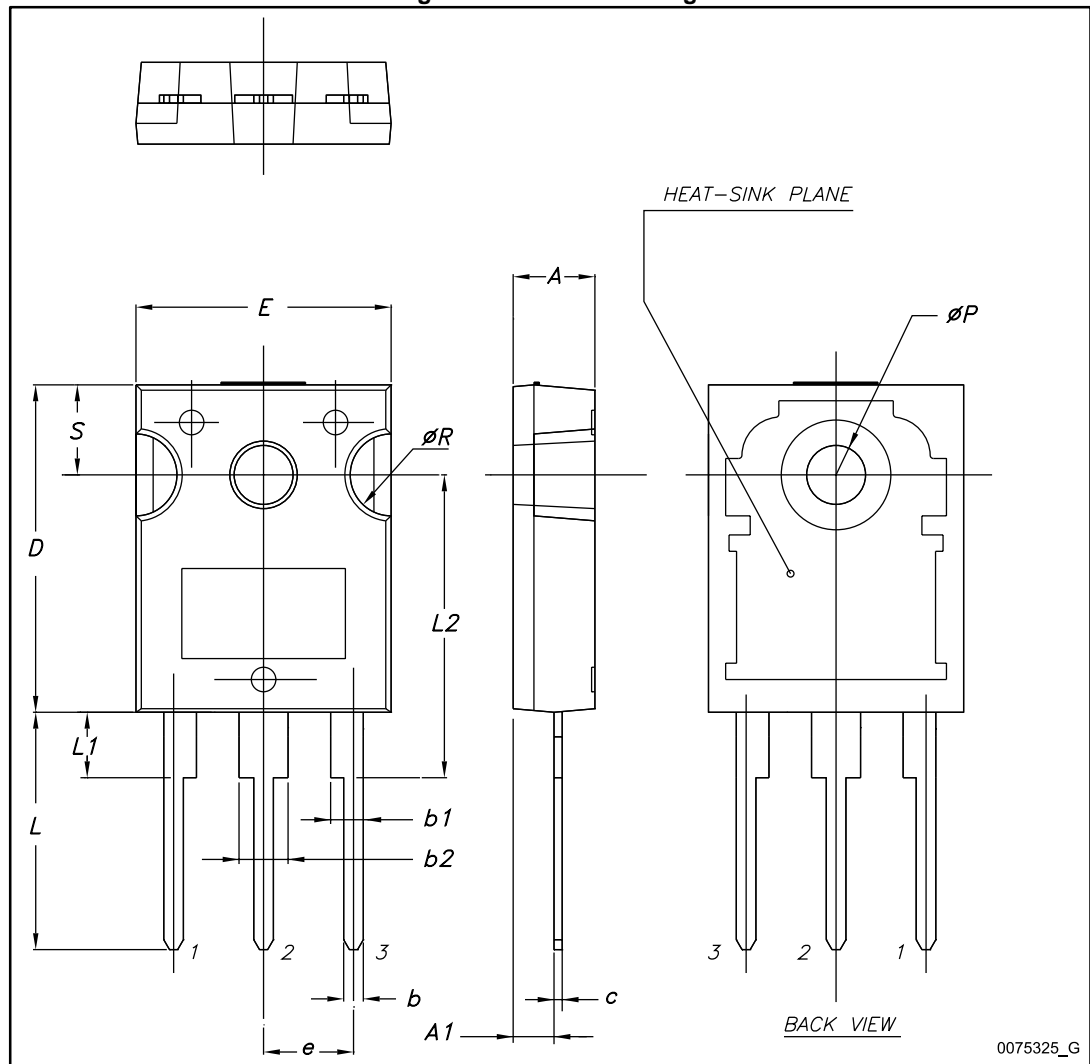
AM01473v1

4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-247

Figure 20: TO-247 drawing



Package mechanical data

STW48N60M2

Table 9: TO-247 mechanical data

| Dim. | mm. | | |
|------|-------|-------|-------|
| | Min. | Typ. | Max. |
| A | 4.85 | | 5.15 |
| A1 | 2.20 | | 2.60 |
| b | 1.0 | | 1.40 |
| b1 | 2.0 | | 2.40 |
| b2 | 3.0 | | 3.40 |
| c | 0.40 | | 0.80 |
| D | 19.85 | | 20.15 |
| E | 15.45 | | 15.75 |
| e | 5.30 | 5.45 | 5.60 |
| L | 14.20 | | 14.80 |
| L1 | 3.70 | | 4.30 |
| L2 | | 18.50 | |
| ØP | 3.55 | | 3.65 |
| ØR | 4.50 | | 5.50 |
| S | 5.30 | 5.50 | 5.70 |

5 Revision history

Table 10: Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 09-Jun-2014 | 1 | First release. |
| 01-Sep-2014 | 2 | Document status promoted from preliminary to production data. Added Section 2.1: "Electrical characteristics (curves)" . Minor text changes. |

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