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[Alpha & Omega Semiconductor Inc.](#)
[AO6424A](#)

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ALPHA & OMEGA
SEMICONDUCTOR

AO6424A

30V N-Channel MOSFET

General Description

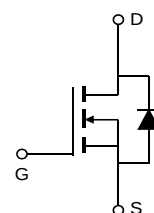
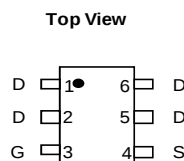
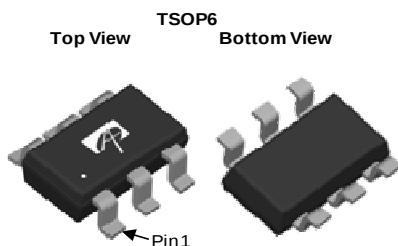
- Latest Trench Power MOSFET technology
- Very Low $R_{DS(ON)}$ at 4.5V V_{GS}
- Low Gate Charge
- High Current Capability
- RoHS and Halogen-Free Compliant

Application

- System/Load Switch

Product Summary

V_{DS}	30V
I_D (at $V_{GS}=10V$)	6.5A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 35mΩ
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	< 48mΩ



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AO6424A	TSOP-6	Tape & Reel	3000

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	6.5	A
Current		5	
Pulsed Drain Current ^C	I_{DM}	27	
Power Dissipation ^B	P_D	2.5	W
		1.5	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	42	50	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^{A, D}		68	85	$^\circ\text{C/W}$
Maximum Junction-to-Lead	$R_{\theta JL}$	23	30	$^\circ\text{C/W}$



Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	ID=250μA, VGS=0V	30			V
IDSS	Zero Gate Voltage Drain Current	VDS=30V, VGS=0V TJ=55°C			1 5	μA
IGSS	Gate-Body leakage current	VDS=0V, VGS=±20V			±100	nA
VGS(th)	Gate Threshold Voltage	VDS=VGS, ID=250μA	1.2	1.8	2.4	V
RDS(on)	Static Drain-Source On-Resistance	VGS=10V, ID=5A TJ=125°C		29 44	35 53	mΩ
		VGS=4.5V, ID=4A		38	48	mΩ
gFS	Forward Transconductance	VDS=5V, ID=5A		8		S
VSD	Diode Forward Voltage	IS=1A, VGS=0V		0.76	1	V
IS	Maximum Body-Diode Continuous Current				3	A
DYNAMIC PARAMETERS						
Ciss	Input Capacitance	VGS=0V, VDS=15V, f=1MHz		270		pF
Coss	Output Capacitance			50		pF
Crss	Reverse Transfer Capacitance			35		pF
Rg	Gate resistance	f=1MHz	1.4	2.8	4.2	Ω
SWITCHING PARAMETERS						
Qg(10V)	Total Gate Charge	VGS=10V, VDS=15V, ID=5A		6.3	12	nC
Qg(4.5V)	Total Gate Charge			3.2	8	nC
Qgs	Gate Source Charge			0.65		nC
Qgd	Gate Drain Charge			1.75		nC
tD(on)	Turn-On DelayTime	VGS=10V, VDS=15V, RL=3Ω, RGEN=3Ω		3		ns
tr	Turn-On Rise Time			2.5		ns
tD(off)	Turn-Off DelayTime			17.5		ns
tf	Turn-Off Fall Time			2.5		ns
trr	Body Diode Reverse Recovery Time	IF=5A, dI/dt=100A/μs		10		ns
Qrr	Body Diode Reverse Recovery Charge	IF=5A, dI/dt=100A/μs		2.3		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

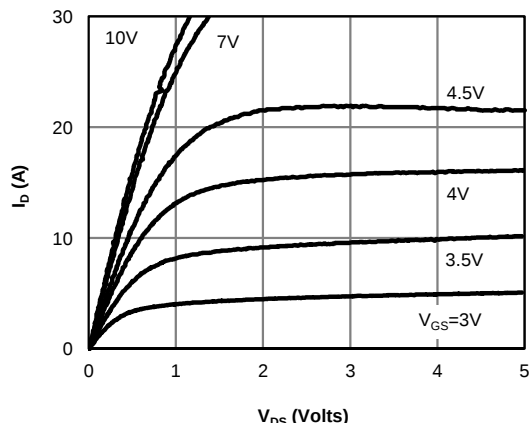


Figure 1: On-Region Characteristics (Note E)

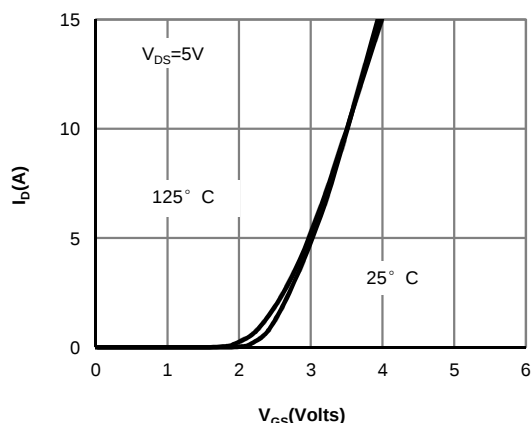


Figure 2: Transfer Characteristics (Note E)

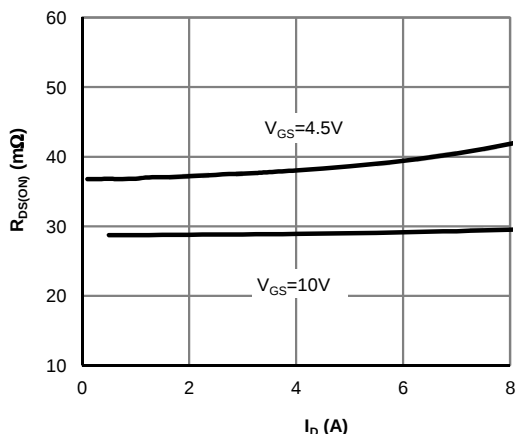


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

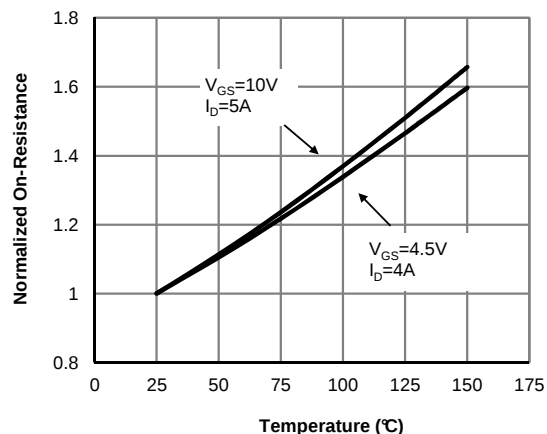


Figure 4: On-Resistance vs. Junction Temperature (Note E)

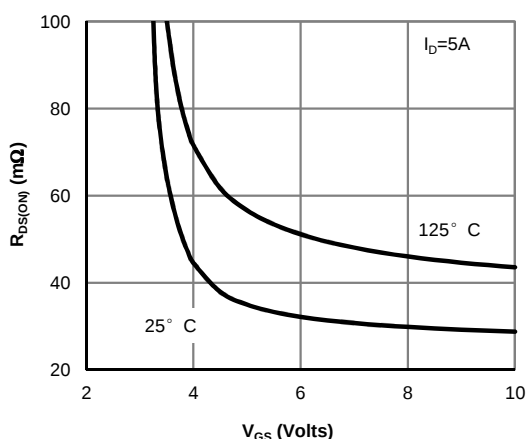


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

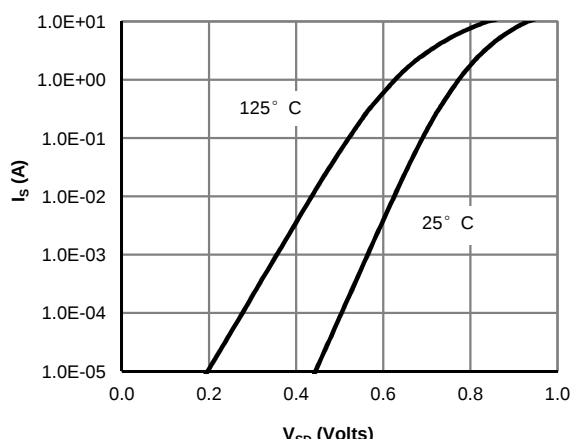


Figure 6: Body-Diode Characteristics (Note E)



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

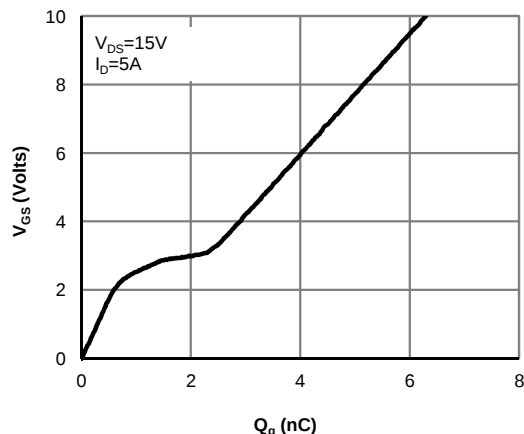


Figure 7: Gate-Charge Characteristics

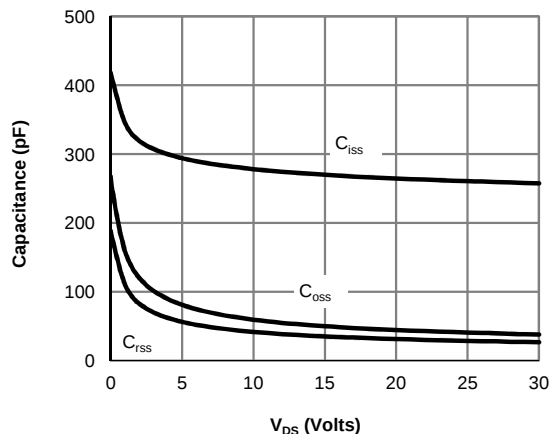


Figure 8: Capacitance Characteristics

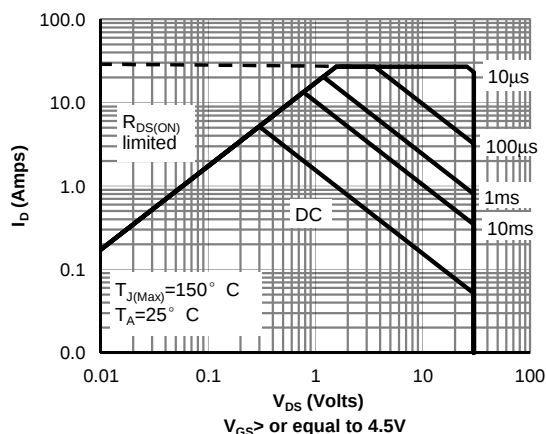


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

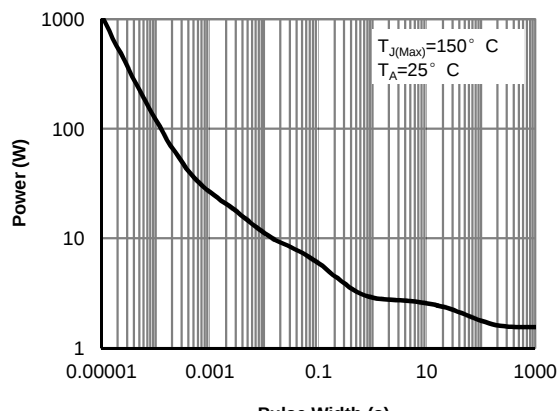


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

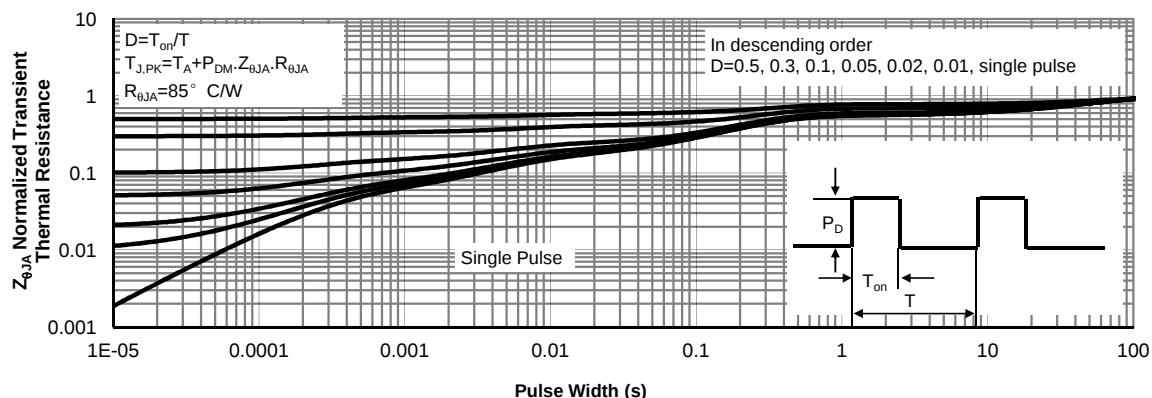
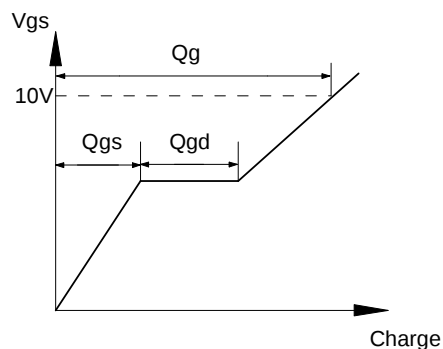
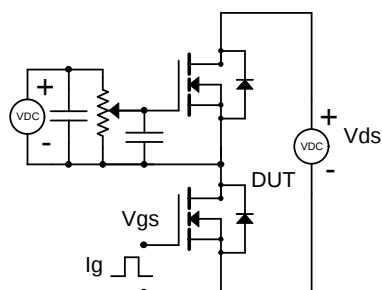


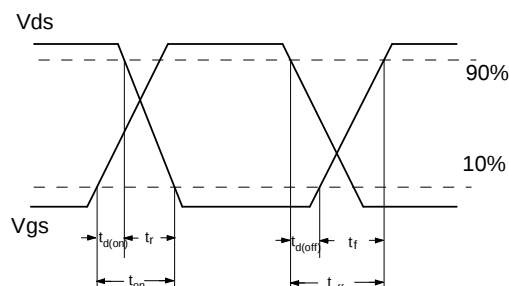
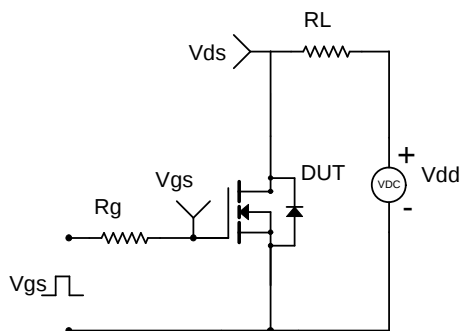
Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)



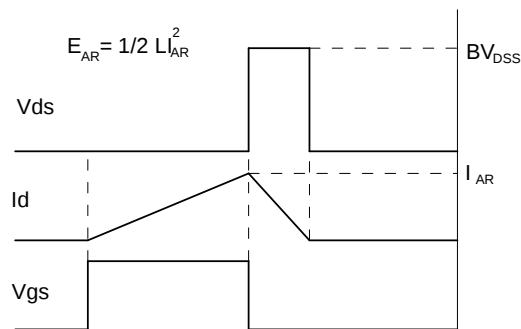
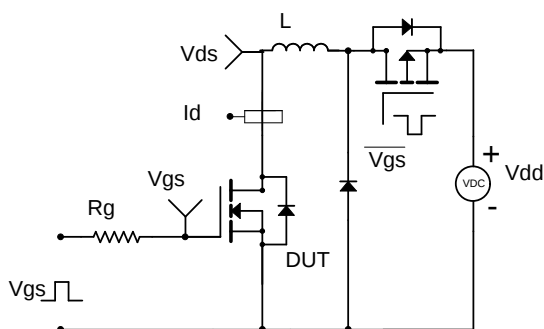
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

