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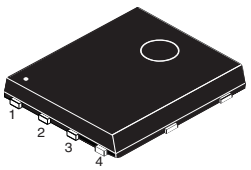
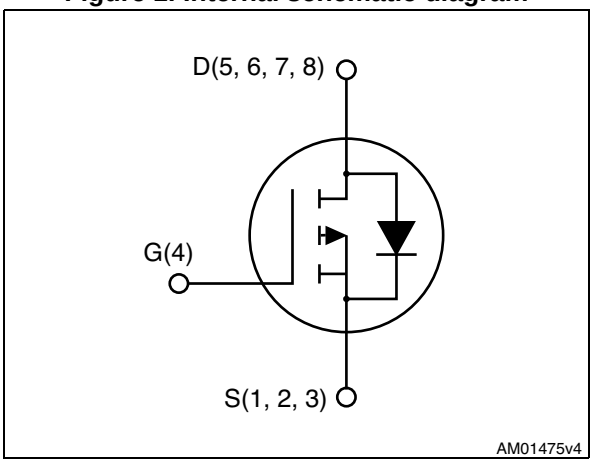
P-channel 30 V, 0.024 Ω typ., 9 A STripFET™ VI DeepGATE™ Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet – preliminary data



PowerFLAT™ 5x6

Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max	I_D	P_{TOT}
STL30P3LLH6	30 V	0.03 Ω	9 A	4.8 W

- $R_{DS(on)}$ * Q_g industry benchmark
- Extremely low on-resistance $R_{DS(on)}$
- High avalanche ruggedness
- Low gate drive power losses

Applications

- Switching applications

Description

This device is a P-channel Power MOSFET developed using the 6th generation of STripFET™ DeepGATE™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest $R_{DS(on)}$ in all packages.

Table 1. Device summary

Order code	Marking	Package	Packaging
STL30P3LLH6	30P3L	PowerFLAT™ 5x6	Tape and reel

Note: For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	30	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	18.75	A
I_D (2)	Drain current (continuous) at T_{pcb} = 25 °C	9	A
I_D (2)	Drain current (continuous) at T_{pcb} = 100 °C	6.4	A
I_{DM} (2)(3)	Drain current (pulsed)	36	A
P_{TOT} (1)	Total dissipation at T_C = 25 °C	75	W
P_{TOT} (2)	Total dissipation at T_{pcb} = 25 °C	4.8	W
	Derating factor (2)	0.03	W/°C
T_{stg}	Storage temperature	- 55 to 175	°C
T_j	Max. operating junction temperature	175	°C

1. The value is rated according to $R_{thj\text{-}c}$
2. This value is rated according to $R_{thj\text{-}pcb}$
3. Pulse width is limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	2.00	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb, single operation	31.3	°C/W

1. When mounted on FR-4 board of 1inch², 2oz Cu, steady state

Note: For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0, I_D = 250 µA	30			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0, V_{DS} = 30 V			1	µA
		V_{GS} = 0, V_{DS} = 30 V, T_C=125 °C			10	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0, V_{GS} = ± 20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1			V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 4.5 A		0.024	0.03	Ω
		V_{GS} = 4.5 V, I_D = 4.5 A		0.032	0.040	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	1450	-	pF
C_{oss}	Output capacitance		-	178	-	pF
C_{rss}	Reverse transfer capacitance		-	120	-	pF
Q_g	Total gate charge	V_{DD} = 24 V, I_D = 9 A, V_{GS} = 4.5 V	-	12	-	nC
Q_{gs}	Gate-source charge		-	4.4	-	nC
Q_{gd}	Gate-drain charge		-	5	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 24 V, I_D = 4.5 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	15	-	ns
t_r	Rise time		-	15	-	ns
$t_{d(off)}$	Turn-off delay time		-	24	-	ns
t_f	Fall time		-	21	-	ns

Note: For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		9	A
I_{SDM} (1)	Source-drain current (pulsed)		-		36	A
V_{SD} (2)	Forward on voltage	I_{SD} = 4.5 A, V_{GS} = 0	-		1.1	V
t_{rr}	Reverse recovery time	I_{SD} = 4.5 A, di/dt = 100 A/µs V_{DD} = 16 V, T_j=150 °C	-	15		ns
Q_{rr}	Reverse recovery charge		-	6.5		nC
I_{RRM}	Reverse recovery current		-	0.9		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

Note: For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

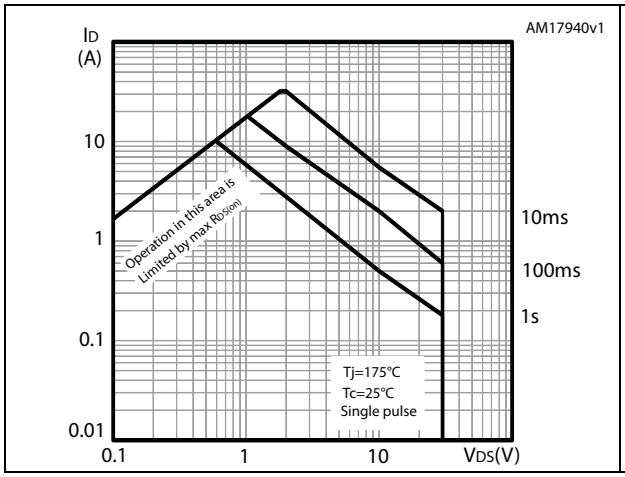


Figure 3. Thermal impedance

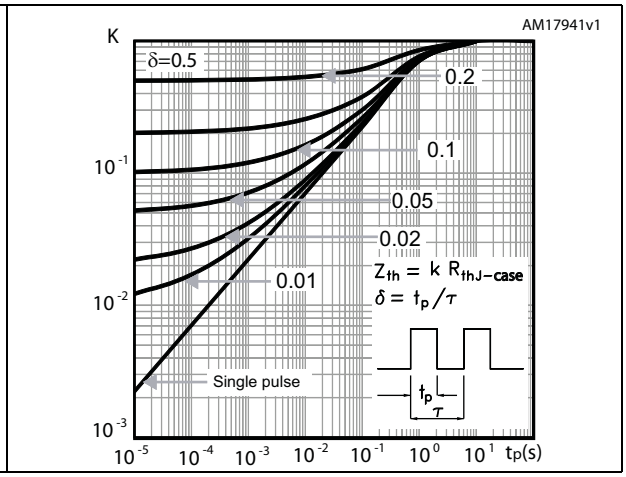


Figure 4. Output characteristics

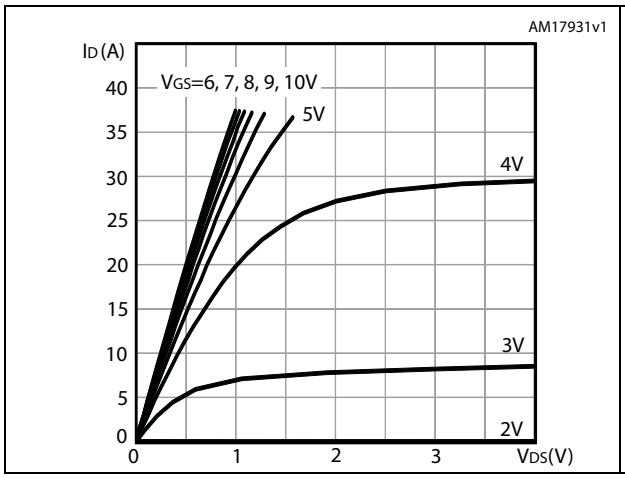


Figure 5. Transfer characteristics

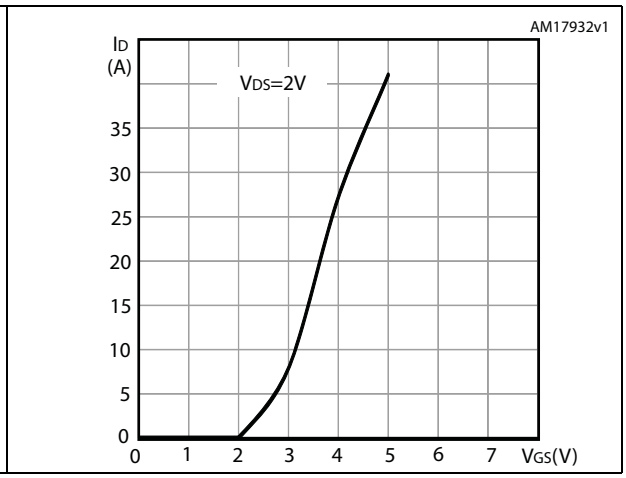


Figure 6. Gate charge vs gate-source voltage

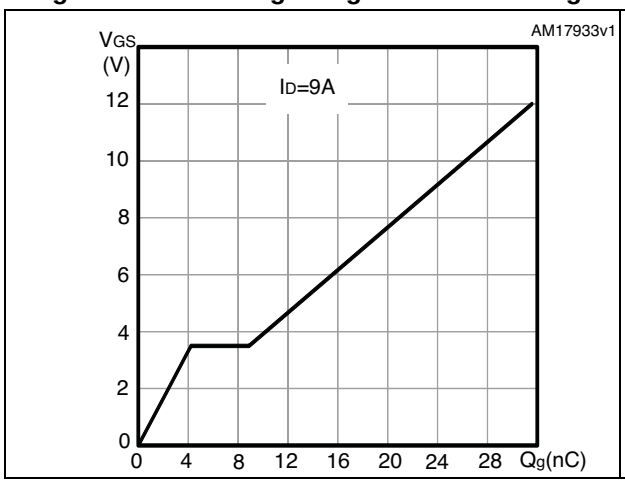


Figure 7. Static drain-source on-resistance

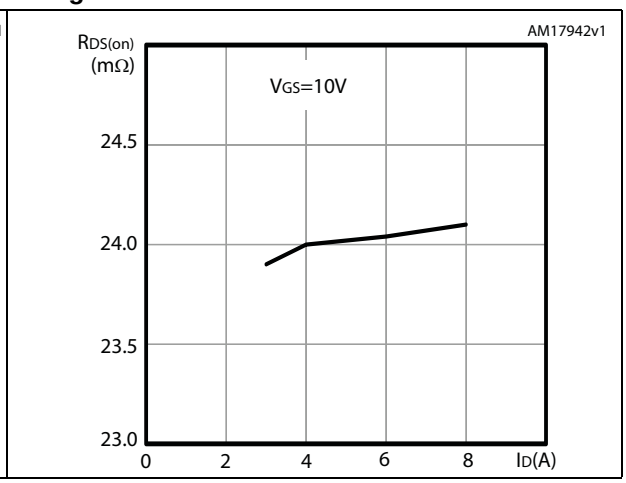


Figure 8. Capacitance variations

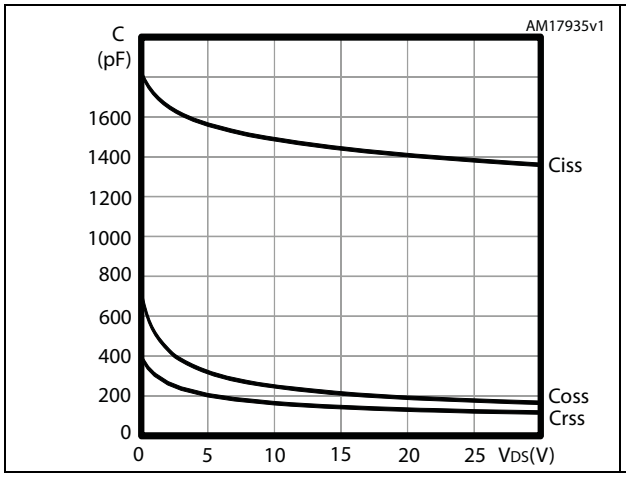


Figure 9. Normalized gate threshold voltage vs temperature

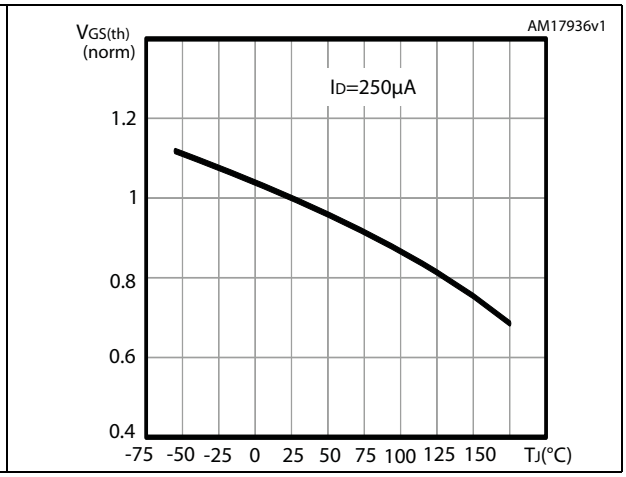


Figure 10. Normalized on-resistance vs temperature

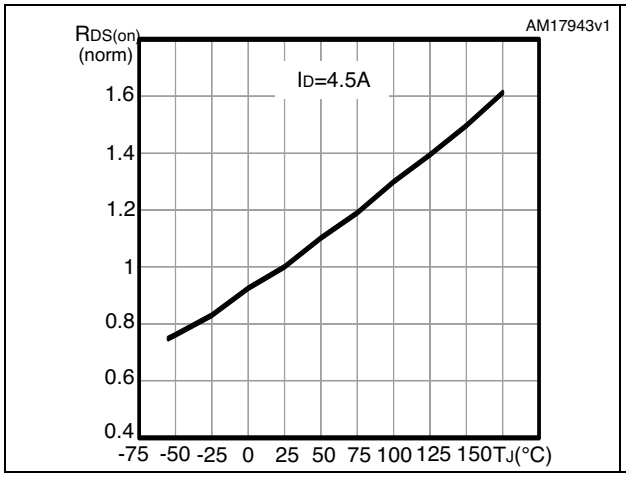


Figure 11. Normalized V_{DS} vs temperature

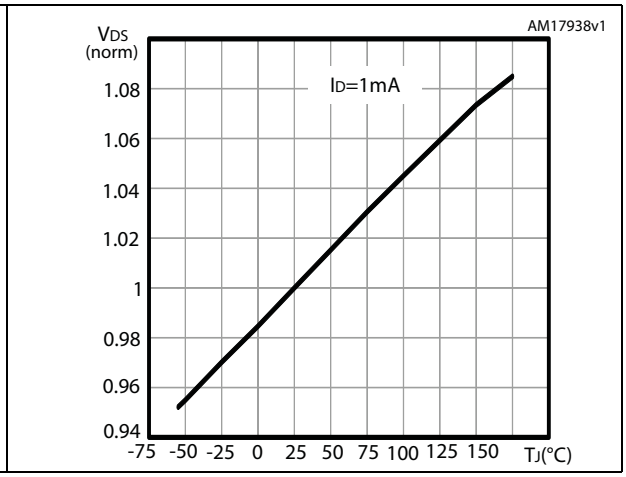
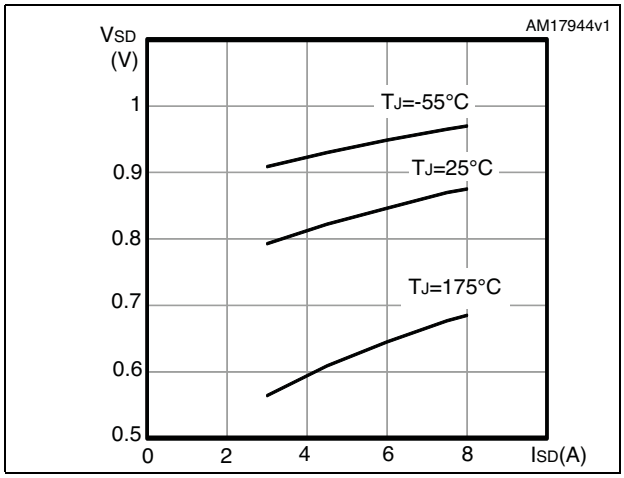


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

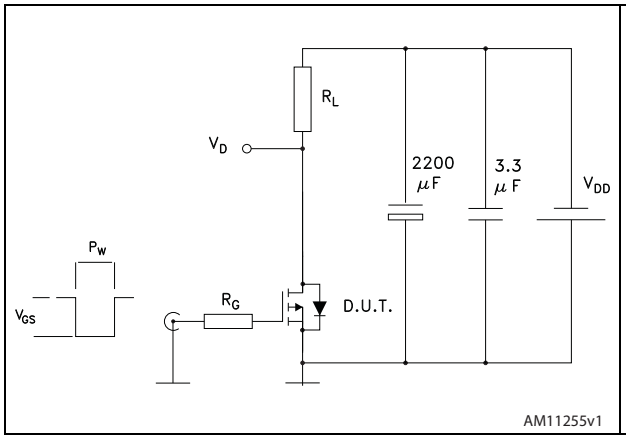


Figure 14. Gate charge test circuit

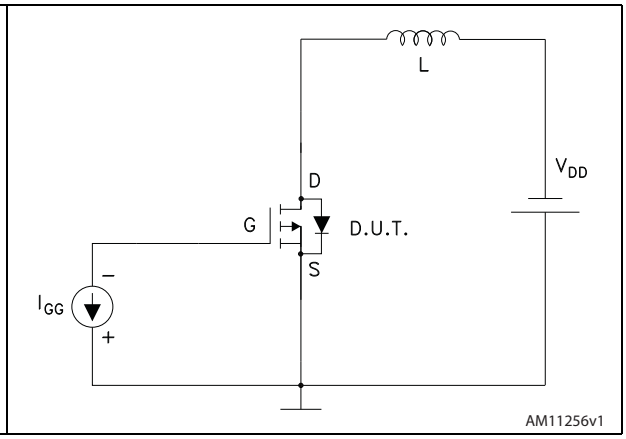
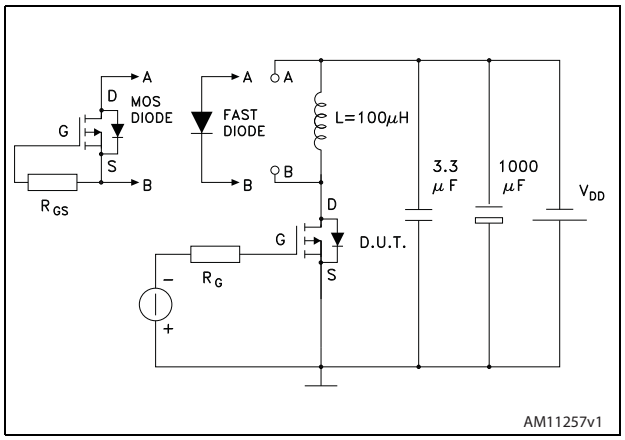


Figure 15. Test circuit for diode recovery behavior



4 Package mechanical data

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Figure 16. PowerFLAT™ 5x6 type S-R drawing

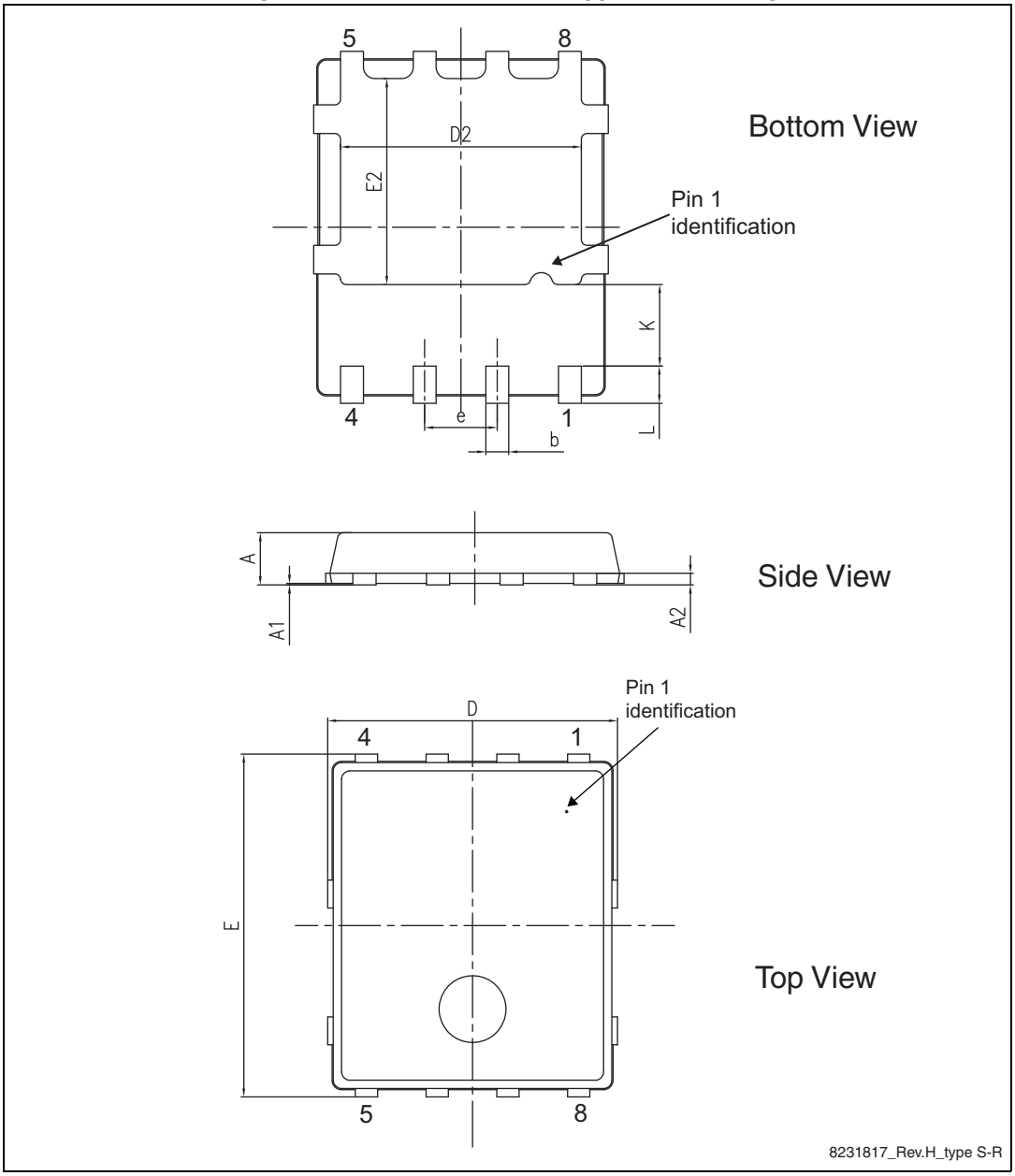
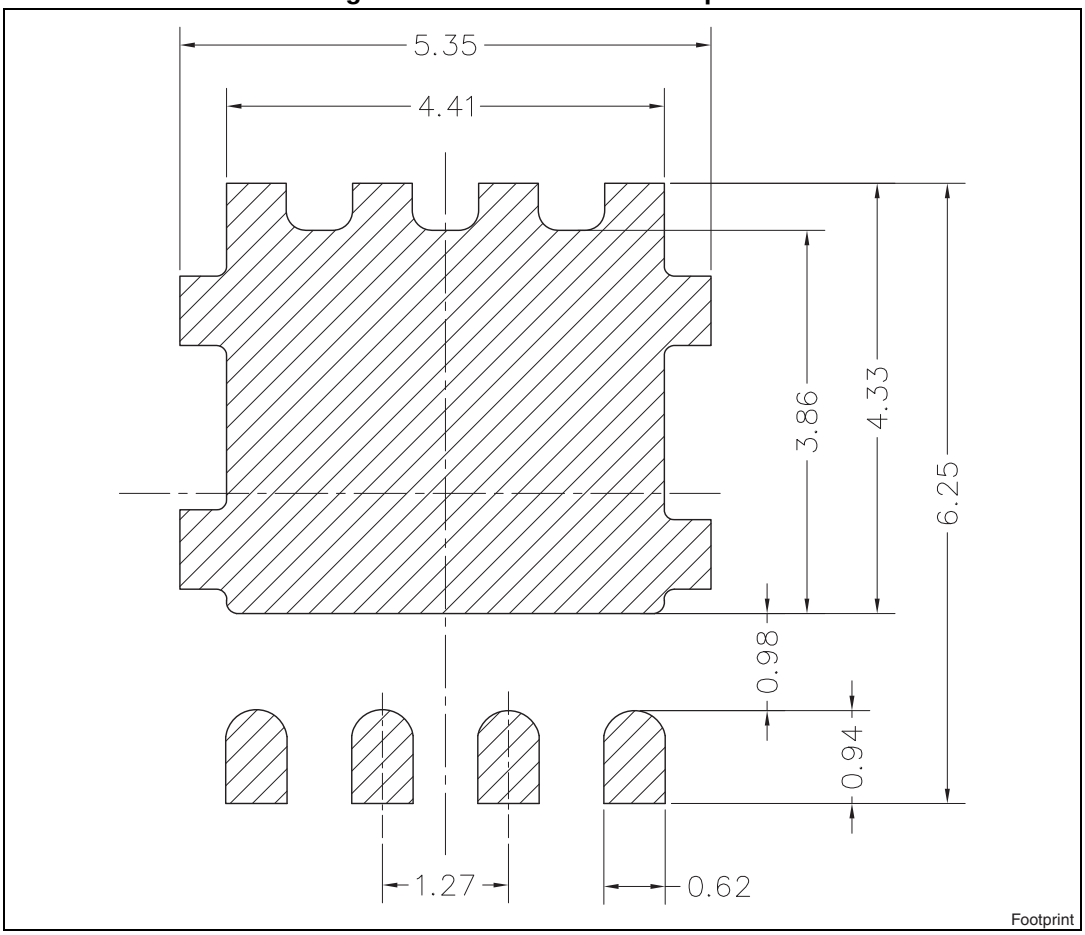


Table 8. PowerFLAT 5x6 type S-R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
E	5.95	6.15	6.35
D2	4.11		4.31
E2	3.50		3.70
e		1.27	
L	0.60		0.80
K	1.275		1.575

Figure 17. Recommended footprint



5 Packaging mechanical data

Figure 18. PowerFLAT™ 5x6 tape(a)

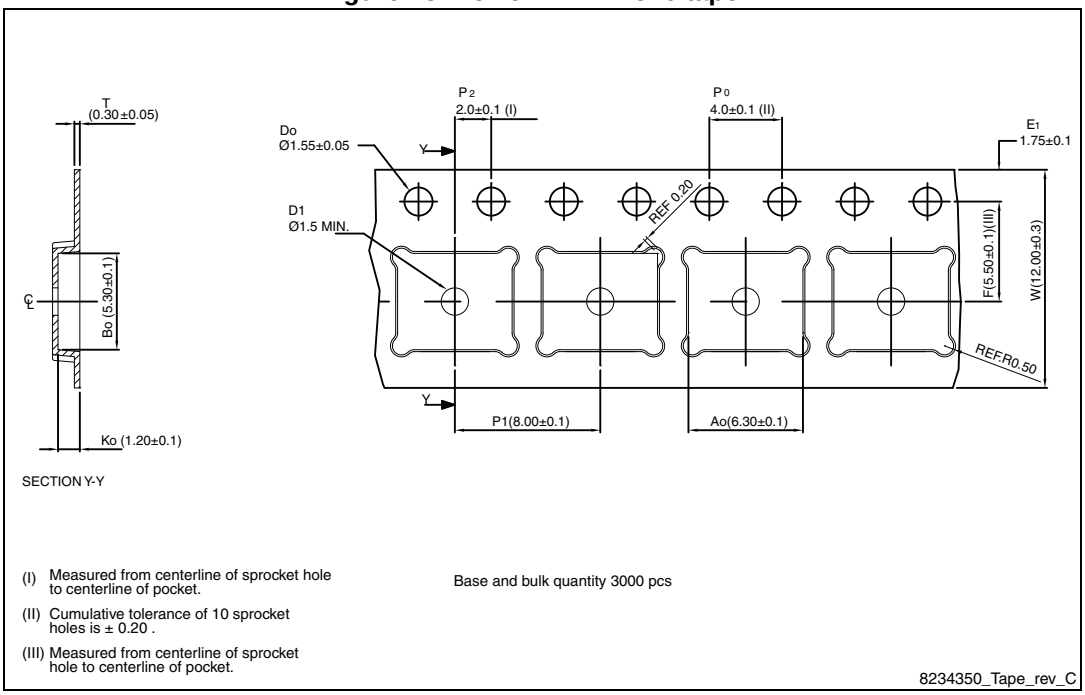
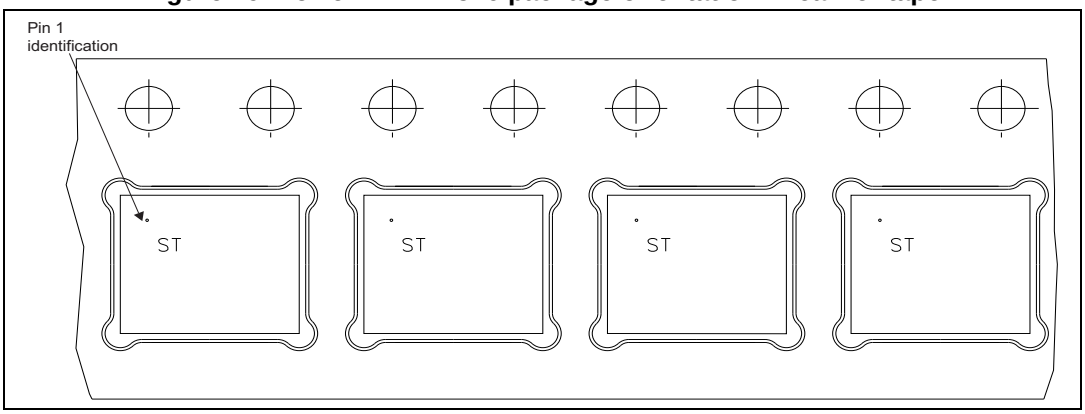
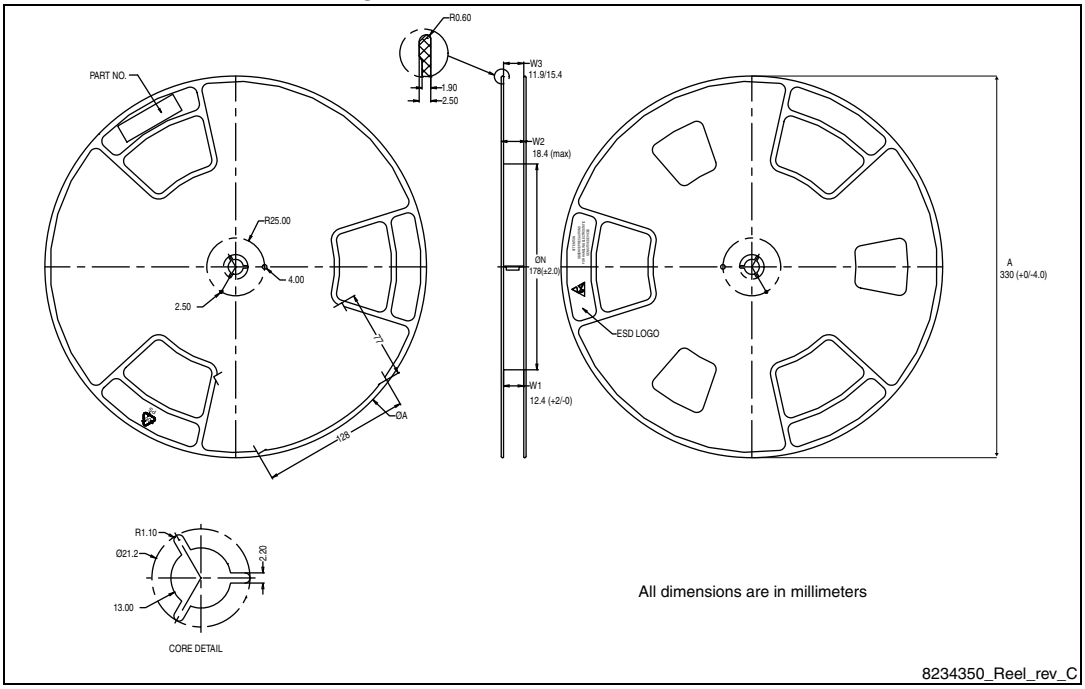


Figure 19. PowerFLAT™ 5x6 package orientation in carrier tape



a. All dimensions are in millimeters.

Figure 20. PowerFLAT™ 5x6 reel



6 Revision history

Table 9. Document revision history

Date	Revision	Changes
20-Mar-2013	1	First release.
28-Nov-2013	2	– Modified: title – Modified: I_D, P_{TOT} values and *Figure 1* in cover page – Modified: V_{GS}, I_D (at T_{pcb}=125 °C and T_{pcb}=100 °C), I_{DM}, P_{TOT} (at T_c=25 °C and T_{pcb}=25 °C) and T_{stg} in *Table 2* – Modified: $R_{thj\text{-}pcb}$ value in *Table 3* – Modified: I_{GSS} (V_{GS} - test condition) value and I_D (for $R_{DS(on)}$) in *Table 4* – Modified: Q_g value in *Table 5* – Modified: I_D value in *Table 6* – Modified: I_{SD} and I_{SDM} in *Table 7* – Added:*Section 2.1: Electrical characteristics (curves)* – Minor text changes
08-Jan-2014	3	– Modified: T_j value in *Table 2* – Modified: *Figure 6* – Updated: *Section 4: Package mechanical data* – Minor text changes

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