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[EQ0321](#)

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	EQ0321 Programmable linear Hall IC for 1 axis
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1. General Description

The EQ0321 is a programmable linear Hall IC which has two Hall elements and a processing circuit. The output of the EQ0321 is an analog voltage and proportional with the displacement of the magnet that placed above the EQ0321. The EQ0321 is suitable for precise position sensing to optical image stabilization, auto focus, zoom lenses of digital steel camera.

2. Features

- | | |
|--|-----------------------------------|
| □ Sensing stroke | ; 1~3mm |
| □ Accuracy | ; 0.1 % of sensing stroke (Ideal) |
| □ 4-line SPI interface | |
| □ Consumption current | |
| Power down mode | ; 5 μ A (Max.) |
| Active mode | ; 5.5 mA (Typ.), 7.5 mA (Max.) |
| □ Power supply | ; 2.7 ~ 5.5 V |
| □ Package size | ; 10 pin, SON (2.9×3.2×0.6mm) |
| □ Operating Temperature | ; -30°C ~ 85°C |
| □ Compensating the temperature characteristic of the magnet and Hall elements. | |

3. Table of Contents

1. Genaral Description	1
2. Features	1
3. Table of Contents.....	2
4. Block Diagram and Functions	3
5. Pin Configurations and Functions.....	4
6. Absolute Maximum Ratings	5
7. Recommended Operating Conditions	5
8. Electrical Characteristics	5
9. Non-volatile Memory Characteristics.....	10
10. Functional Descriptions	10
11. Recommended External Circuits	15
12. Package	16
13. Taping	18
14. Soldering Conditions	19
IMPORTANT NOTICE	20

4. Block Diagram and Functions

4.1 Block Diagram

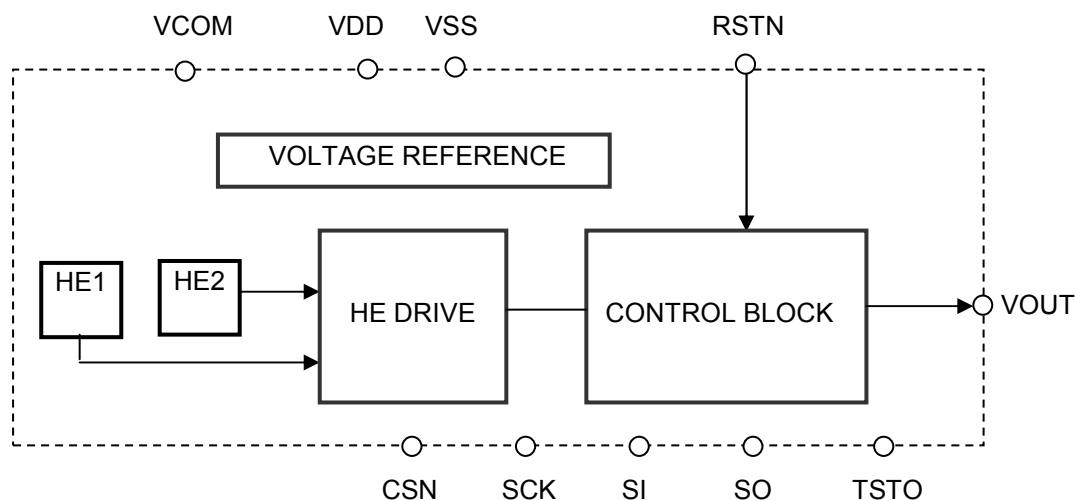


Figure 1. Block diagram of the EQ0321

4.2 Block Function

Table 1. Explanation of circuit block

Name	Description
HE1, HE2	Hall elements
CONTROL BLOCK	It calculates $(B1-B2) / (B1+B2)$, adjusts gain and offset voltage, controls HE DRIVE.
HE DRIVE	It supplies the driving voltage to Hall elements.
VOLTAGE REFERENCE	It generates reference voltage.

5. Pin Configurations and Functions

5.1 Pin Configurations

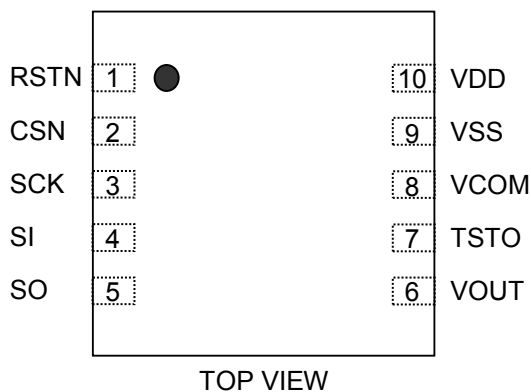


Figure 2. Bump down view

5.2 Pin Function

Table 2. Pin configurations and functions of the EQ0321

Pin No.	Pin Name	Type (Note 1)	I/O (Note 2)	Description
1	RSTN	D	I	When the input signal is “Low”, the power down mode is active. Please make the input “Low” before power on.
2	CSN	D	I	The chip select pin for serial interface.
3	SCK	D	I	The clock input pin for serial interface.
4	SI	D	I	The data input pin for serial interface.
5	SO	D	O	The data output pin for serial interface.
6	VOUT	A	O	This pin outputs the voltage which is proportional to the position of the magnet. Maximum capacity load = 20pF. Minimum resistance load = 100kΩ.
7	TSTO	A	O	This is a test pin. This pin should be connected to V _{SS} .
8	VCOM	A	O	This pin outputs the internal reference voltage (V _{DD} /2). Please connect 0.01μF to ground. No resistance load.
9	VSS	GND	—	Ground
10	VDD	PWR	—	Power supply

(Note 1) A(analog pin), D(digital pin), GND(ground pin), PWR(power pin)

(Note 2) I(input pin), O(output pin).

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[EQ0321]

6. Absolute Maximum Ratings

If the device is used in conditions exceeding below values, the device may be destroyed. Normal operations are not guaranteed in such exceeding conditions.

Table 3. Absolute Maximum Ratings

Ta = 25 °C, unless otherwise specified.

Parameter	Symbol	Min.	Max.	Pin	Units
Supply Voltage	V _{DD}	-0.3	6.0		V
Input Voltage	V _{IN}	-0.3	V _{DD} +0.3		V
Storage Temperature	T _{stg}	-40	125		°C

7. Recommended Operating Conditions

Table 4. Recommended operating conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V _{DD}		2.7		5.5	V
Operating Temperature Range	Ta		-30		85	°C
Input M.F.D. Range	Bin	(Note 1)	15		150	mT
“B1-B2” Range	Bsub	(Note 2)	-120		120	mT
“B1+B2” Range	Badd	(Note 2)	70		250	mT
“(B1-B2) / (B1+B2)” Range	Bdiv	(Note 2)	-0.7		0.7	-

(Note 1) Magnetic Flux Density (M.F.D.) applied into one Hall element.

(Note 2) B1, B2 = the applied magnetic flux density of each Hall elements of the EQ0321.

8. Electrical Characteristics

8.1 Analog Electrical Characteristics

Table 5. Analog Electrical Characteristics

V_{DD} = 2.7 ~ 5.5 V, Ta = 25 °C, GAIN = 2.4 and OFFSET=0mV, unless otherwise specified.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Standby Current	SIDD	RSTN=V _{SS} , Bsub=0mT, Badd=80mT			5	μA
Consumption Current	DIDD	RSTN=V _{DD} , Bsub=0mT, Badd=80mT		5.5	7.5	mA
Output Sensitivity	Vh	(Note 1) Bsub=±8mT, Badd=80mT	28.5	30.0	31.5	mV/mT
Offset Voltage	VOU0	Bsub=0mT, Badd=80mT	V _{DD} /2 -0.15	V _{DD} /2	V _{DD} /2 +0.15	V
Output High Saturation Voltage	Vsath	100kΩ load against VSS	V _{DD} -0.3		V _{DD}	V
Output Low Saturation Voltage	Vsatl	100kΩ load against VDD	0		0.3	V
Power On Time	tpon	(Note 2) Bsub=0mT, Badd=80mT			1	ms
Reset Release Time	tRST	(Note 2)	0.5			ms

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Temperature Drift of Output Sensitivity	Vhd	(Note 3)(Note 4) Ta=-30~85°C, 25°C standard		±2		%
Temperature Drift of Offset Voltage	Vofd	(Note 3)(Note 5) Ta=-30~85°C, 25°C standard		±30		mV
Output Noise Voltage		(Note 3) (Note 6) Badd=150mT		0.2		mVrms
Bandwidth	fT	(Note 3)		10		kHz

(Note 1) The Slope of a line that calculated by least-square method by Vout1 (Bsub=0, Badd=80), Vout2 (Bsub=8, Badd=80) and Vout3 (Bsub=-8, Badd=80) is equal Vh.

$V_{out} = \{ B_{sub} / B_{add} \} \times GAIN \times 1000 + V_{OUT0} [mV]$

(Note 2) Figure 3 is a timing chart about power on. "tpon" is a time to reach less than ±1% of the offset voltage after a reset release. "tRST" is a reset release time after VDD is stable.

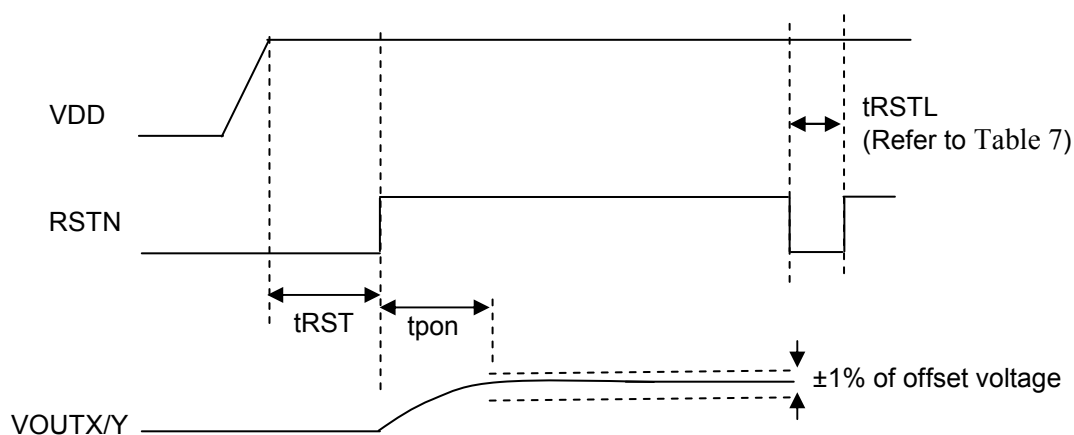


Figure 3. Operation when the device is powered up

(Note 3) These parameters are not tested in mass production.

(Note 4) $V_{hd} = \{ (V_h(T_a) - V_h(25^\circ C)) / V_h(25^\circ C) \} \times 100 [\%]$

(Note 5) $V_{ofd} = V_{OUT0}(T_a) - V_{OUT0}(25^\circ C) [mV]$

(Note 6) The external LPF circuit ($f_c = 2kHz$)

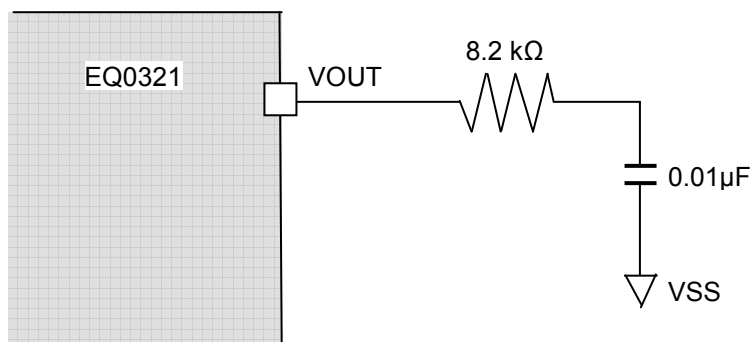


Figure 4. LPF circuit

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8.2 Digital DC Specification

Table 6. Digital DC Specification

$V_{DD} = 2.7 \sim 5.5 \text{ V}$, $T_a = -30 \sim 85 \text{ }^{\circ}\text{C}$, unless otherwise specified.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input High Voltage	V_{IH}	RSTN, CSN, SCK, SI	$0.8V_{DD}$		V_{DD}	V
Input Low Voltage	V_{IL}	RSTN, CSN, SCK, SI	0		$0.2V_{DD}$	V
Output High Voltage	V_{OH}	SI, $I_{OH} = -400\mu\text{A}$	$V_{DD}-0.4$			V
Output Low Voltage	V_{OL}	SI, $I_{OL} = +400\mu\text{A}$			0.4	V
Input Leakage	I_{LI}	RSTN, CSN, SCK, SI	-10		10	μA
Output Leakage	I_{HL}	SO	-10		10	μA

8.3 Digital AC Specification

Table 7. Digital AC Specification

$V_{DD} = 2.7 \sim 5.5 \text{ V}$, $T_a = -30 \sim 85 \text{ }^{\circ}\text{C}$, Load capacitance = 30 pF, unless otherwise specified.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCK Frequency	fSK				10	MHz
SCK Setup time	tSKSH		20			ns
CSN Setup time	tCSS		40			ns
SCK Pulse Width	tSKW		40			ns
SCK Rise Time	tRC	(Note 1)			10	ns
SCK Fall Time	tFC	(Note 1)			10	ns
Data Setup Time	tDIS		15			ns
Data Hold Time	tDIH		15			ns
Data Rise Time	tRD	(Note 1)			10	ns
Data Fall Time	tFD	(Note 1)			10	ns
SO pin Output Delay	tPD				25	ns
SO pin Hi-Z Time	tOZ	(Note 1)			40	ns
SO pin Output Hold Time	tOHD		0			ns
CSN Hold Time	tCSH		40			ns
SCK Hold Time	tSKH		20			ns
CSN High Time	tCS		40			ns
EEPROM Program Time	tWR		10		20	ms
Reset Time	tRSTL	(Note 2)	10			μs

(Note 1) These parameters are not tested in mass production.

(Note 2) See Figure 3.

8.4 Synchronous Data Timing

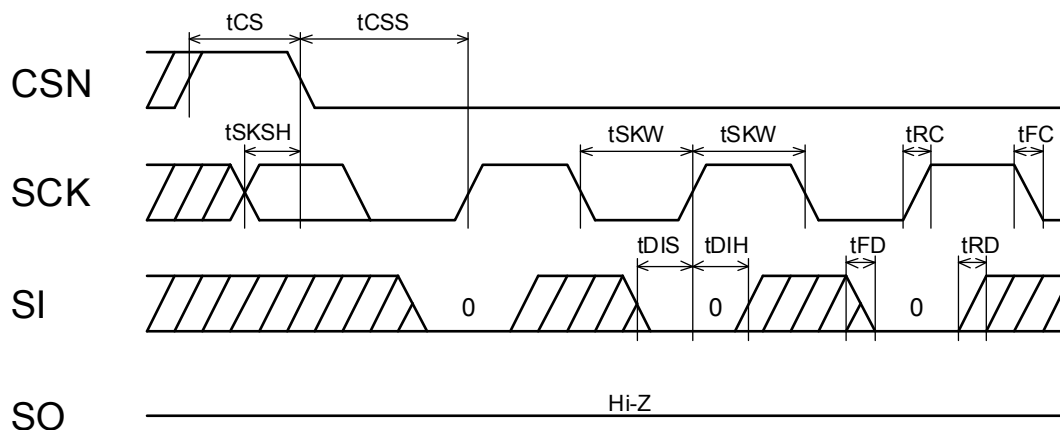


Figure 5. Instruction Input

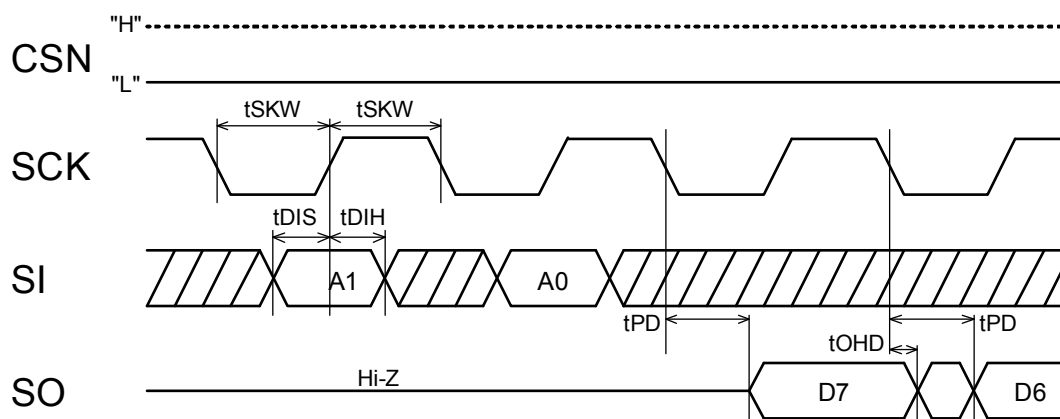


Figure 6. Data Output (READ)

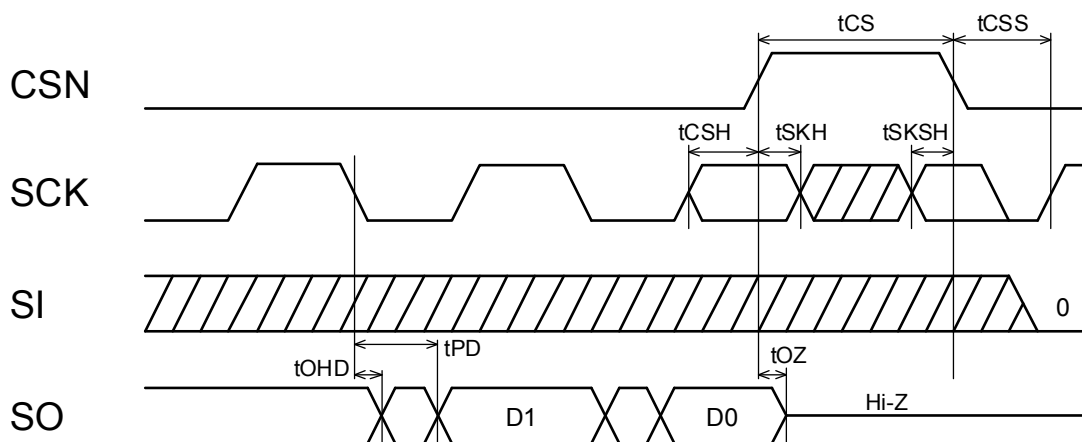


Figure 7. Data Output (READ) at end of command

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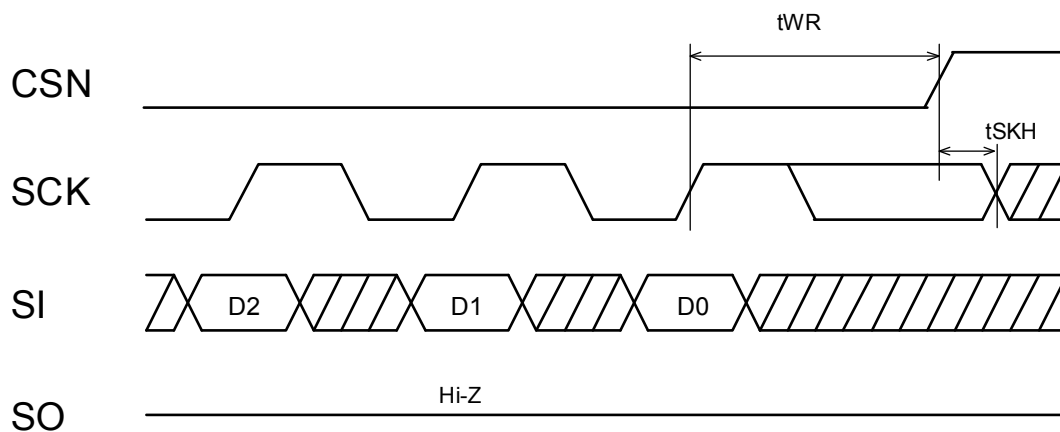


Figure 8. Data Input (WRITE)

9. Non-volatile Memory Characteristics

Table 8. Non-volatile Memory Characteristics

$V_{DD} = 2.7 \sim 5.5 \text{ V}$, $T_a = -30 \sim 85 \text{ }^{\circ}\text{C}$, unless otherwise specified.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
EEPROM Endurance	EEN				1000	Cycles
EEPROM Data Retention	ERE	(Note 1)	10			Years

(Note 1) Data retention is not guaranteed after rewritten over 1000 cycles

10. Functional Descriptions

10.1 Positional relation of the magnet and the EQ0321

The EQ0321 and a magnet should be placed as Figure 9.

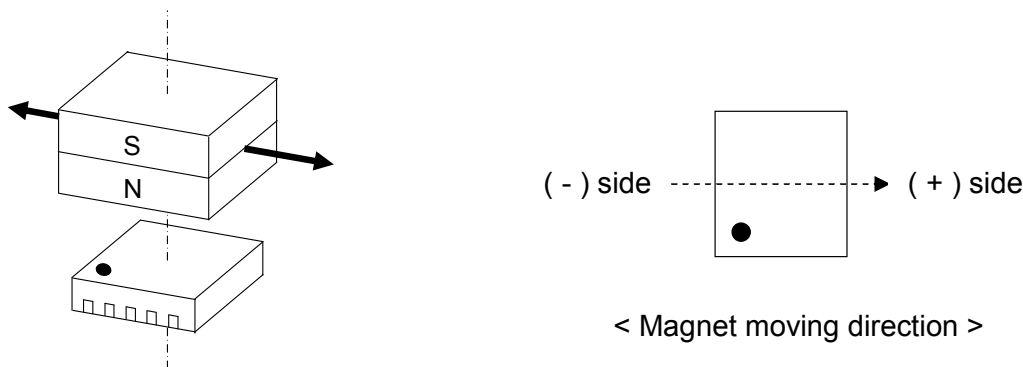


Figure 9. Positional relation of magnet and the EQ0321

When the magnet moves from “(-) side” to “(+) side”, the output voltage increases with magnet position as Figure 10.

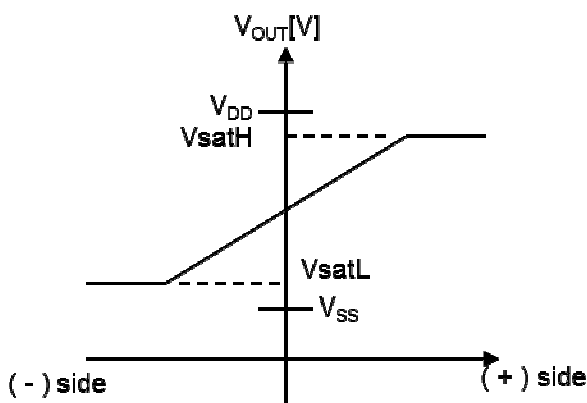


Figure 10. The output voltage with magnet position

10.2 Output voltage, Gain, Offset

The EQ0321 has two Hall elements. The EQ0321 outputs the voltage in proportion to following equations which operated Magnetic Flux Density (= M.F.D.) applied on each Hall element.

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$$V_{OUT} [mV] = \{ B_{sub} / B_{add} \} \times GAIN + OFFSET + VOUT0$$

Where, $B_{sub} [mT] = B1 - B2$

$B_{add} [mT] = B1 + B2$

B1 and B2 are the applied magnetic flux density of each Hall elements of the EQ0321.

GAIN and OFFSET are defined in Section 10.4 and 10.5. These are adjustable.

10.3 Serial interface

Users can read and write the setting data to EEPROM by 4-wire synchronous serial interface. Each command has original operation code, address and data (8bit). Input and output data are synchronized with SCK. The data are entered with a time when SCK rises, and outputted with a time when SCK falls.

Table 9. Command Table

Command	Operation code	Address	Data	Note
WRITE	0000 x010	A7-A0	D7-D0 (in)	Write EEPROM
READ	0000 x011	A7-A0	D7-D0 (out)	Read EEPROM
WREN	0000 x110			EEPROM write enable
WRDI	0000 x100			EEPROM write disable

x : Don't care

Table 10. Memory Map

Memory Name	Address	D7	D6	D5	D4	D3	D2	D1	D0
GAIN	00h	0	0	GA5	GA4	GA3	GA2	GA1	GA0
OFFSET	01h	0	0	0	0	OF3	OF2	OF1	OF0

(Note) Writing to address other than "00h" ~ "01h" is inhibited.

- 10.3.1 WREN (WRITE ENABLE) / WRDI (WRITE DISABLE)

EEPROM has two states, "write enable state" and "write disable state". When WREN command is entered the mode of EEPROM goes to "write enable state". When the EQ0321 is powered on, the state is "write disable state".

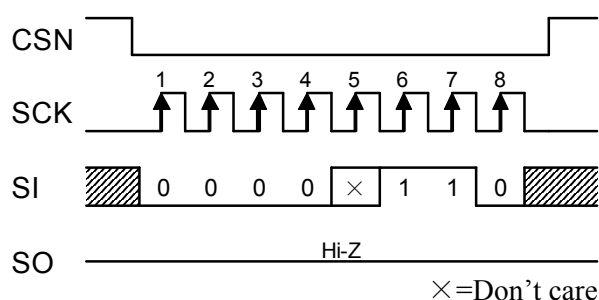


Figure 11. WREN command

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[EQ0321]

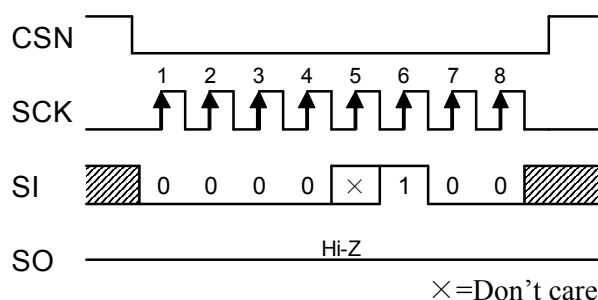


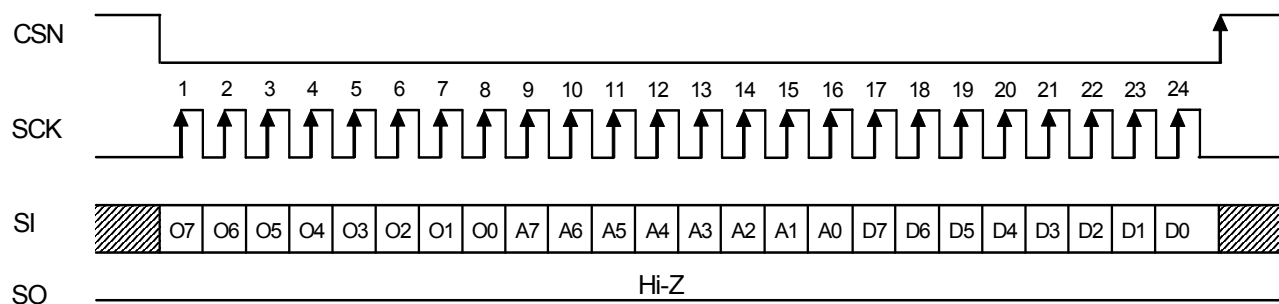
Figure 12. WRDI command

- 10.3.2 WRITE command

WRITE instruction can start the WRITE function to EEPROM.

After CSN pin changes high to low, operation code, address and data are entered from SI pin. After the instruction input, the internal programming cycle starts when CSN pin changes low to high. After the instructions are entered, CSN pin should change low to high after waiting EEPROM Program Time “tWR” and before next SCK clock rises.

After WRITE instruction, the EQ0321 changes to Write Disable status automatically. theEQ0321 needs WREN instruction before every WRITE instruction. When WRITE instruction is done while the EQ0321 is in Write Disable status, WRITE instructions are ignored and the EQ0321 becomes standby status after CSN changes to high. The EQ0321 can accept the next instruction after CSN becomes low.

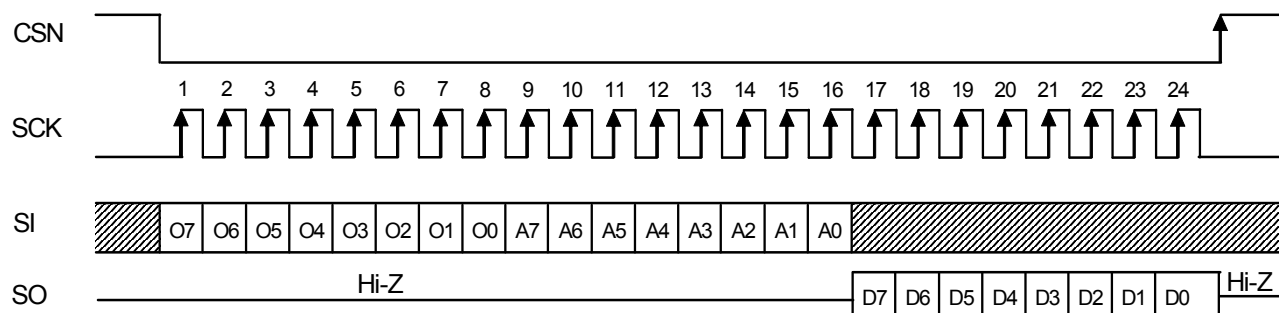


O7-O0: Operation Code, A7-A0 : Address, D7-D0 : Data

Figure 13. WRITE sequence

- 10.3.3 READ command

After CSN changes high to low, the operation code and address are sent on SI pin and the data (D7-D0) outs from SO pin. SI signal is ignored after a final bit (A0) is entered.



O7-O0: Operation Code, A7-A0 : Address, D7-D0 : Data

Figure 14. READ command

10.4 Gain Adjustment Function (Memory Name: GAIN)

Users can change the gain of Vout by writing a setting value to EEPROM by using the serial interface. A factory default setting value of gain is 2.4.

Table 11. GAIN Table

Setting value GA[5]~GA[0]	Gain [times]	Setting value GA[5]~GA[0]	Gain [times]
000000	1.4	010000	3.0
000001	1.5	010001	3.1
000010	1.6	010010	3.2
000011	1.7	010011	3.3
000100	1.8	010100	3.4
000101	1.9	010101	3.5
000110	2.0	010110	3.6
000111	2.1	010111	3.7
001000	2.2	011000	3.8
001001	2.3	011001	3.9
001010	2.4(default)	011010	4.0
001011	2.5	011011	4.1
001100	2.6	011100	4.2
001101	2.7	011101	4.3
001110	2.8	011110	4.4
001111	2.9	011111	4.5

Setting value GA[5]~GA[0]	Gain [times]	Setting value GA[5]~GA[0]	Gain [times]
100000	4.6	110000	6.2
100001	4.7	110001	6.3
100010	4.8	110010	6.4
100011	4.9	110011	6.5
100100	5.0	110100	6.6
100101	5.1	110101	6.7
100110	5.2	110110	6.8
100111	5.3	110111	6.9
101000	5.4	111000	7.0
101001	5.5	111001	7.1
101010	5.6	111010	7.2
101011	5.7	111011	7.3
101100	5.8	111100	7.4
101101	5.9	111101	7.5
101110	6.0	111110	7.6
101111	6.1	111111	7.7

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[EQ0321]

10.5 Offset Adjustment Function (Memory Name: OFFSET)

Users can change DC level of Vout by writing a setting value to EEPROM by using the serial interface. A factory default setting value of DC level is 0mV.

Table 12. OFFSET Table

Setting value OF[3]~OF[0]	DC level [mV]	Setting value OF[3]~OF[0]	DC level [mV]
0000	0(default)	1000	0
0001	+100	1001	-100
0010	+200	1010	-200
0011	+300	1011	-300
0100	+400	1100	-400
0101	+500	1101	-500
0110	+600	1110	-600
0111	+700	1111	-700

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[EQ0321]

11. Recommended External Circuits

11.1 Circuit example

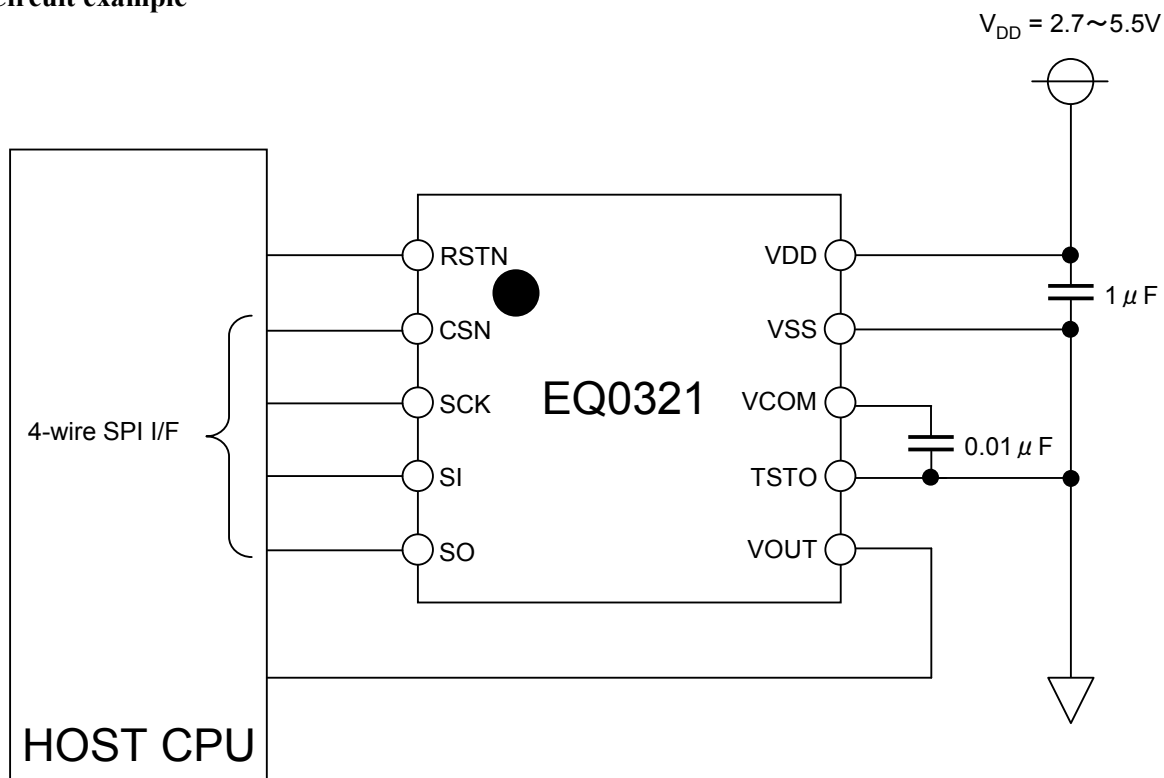


Figure 15. Recommended circuit

12. Package

12.1 Outline Dimensions and Pad Dimensions

10 pin SON package

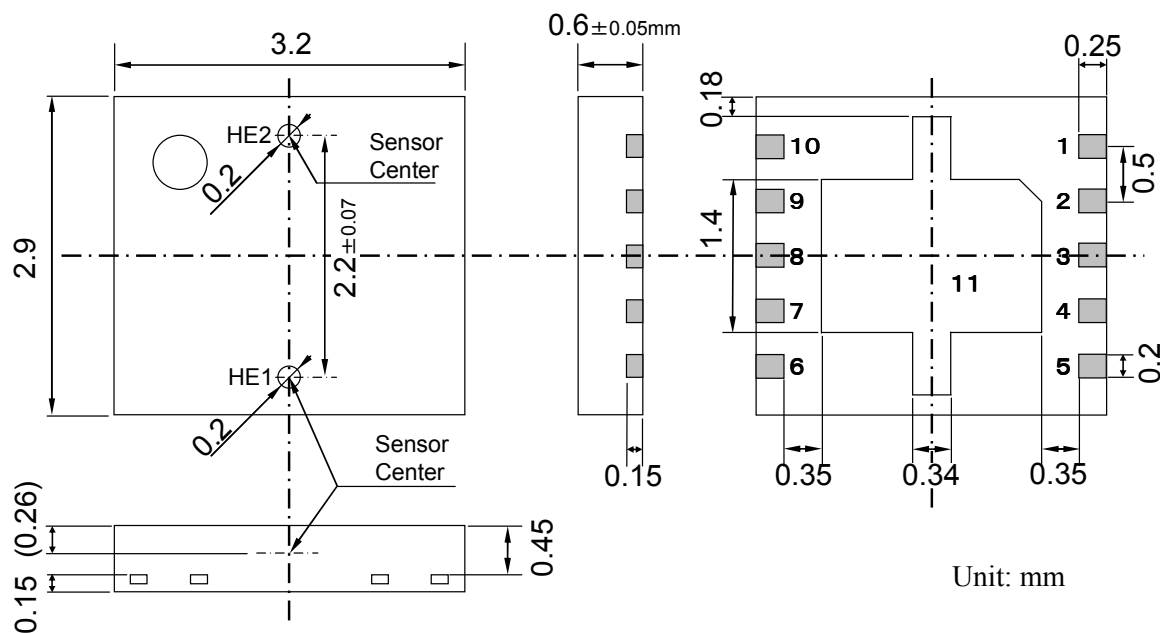


Figure 16. Dimensional drawing of the EQ0321

- 1: RSTN
- 2: CSN
- 3: SCK
- 4: SI
- 5: SO
- 6: VOUT
- 7: TSTO
- 8: VCOM
- 9: VSS
- 10: VDD
- 11: N.C. (OPEN)

- (Note 1) The center of the sensor is located within the $\phi 0.2\text{mm}$ circle.
 (Note 2) Sensor plate is located in 0.26mm depth from the package surface.
 (Note 3) The tolerances of dimensions with no mention is $\pm 0.1\text{mm}$
 (Note 4) There is no plating on cut surface of the terminals.

Package Type: SON

Material of Terminals: Cu

Material of Plating for Terminals: Sn 100%

Plating Thickness: 10 μm (typ.)

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12.2 Recommended Land Pattern

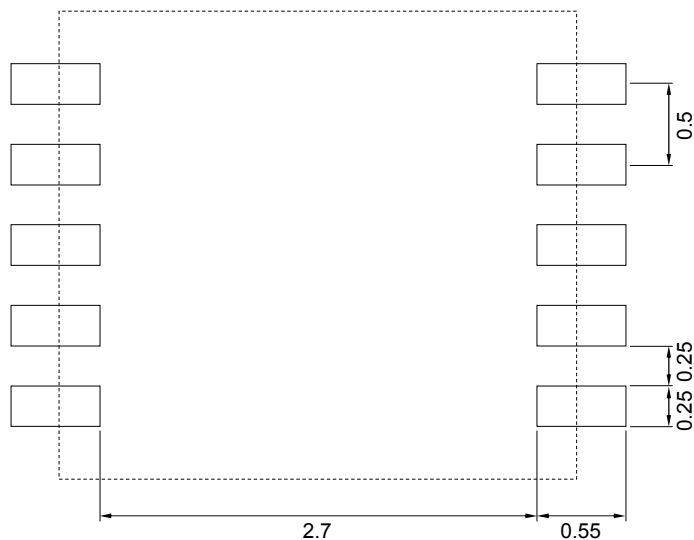


Figure 17. Recommended land pattern

12.3 Marking

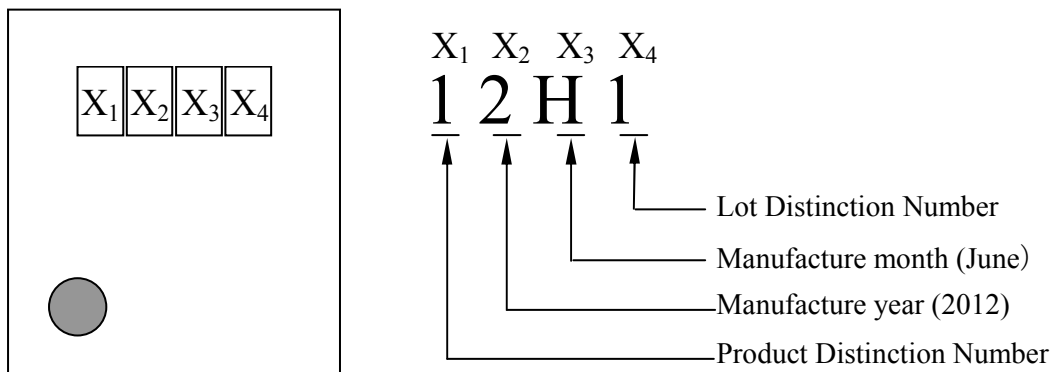


Figure 18. Marking of the EQ0321

Table 13. Marking information

Product Distinction Number		Manufacture Year		Manufacture month	
Mark	Product ID	Mark	Corresponding Year	Mark	Corresponding Month
1	EQ0321	0	2020	C	January
2		1	2011	D	February
3		2	2012	E	March
4		3	2013	F	April
5		4	2014	G	May
6		5	2015	H	June
7		6	2016	J	July
8		7	2017	K	August
9		8	2018	L	September
0		9	2019	M	October
				N	November
				P	December

13. Taping

13.1 Carrier Tape

Products are supplied in the reeled tape which contains 3,000 units per reel.

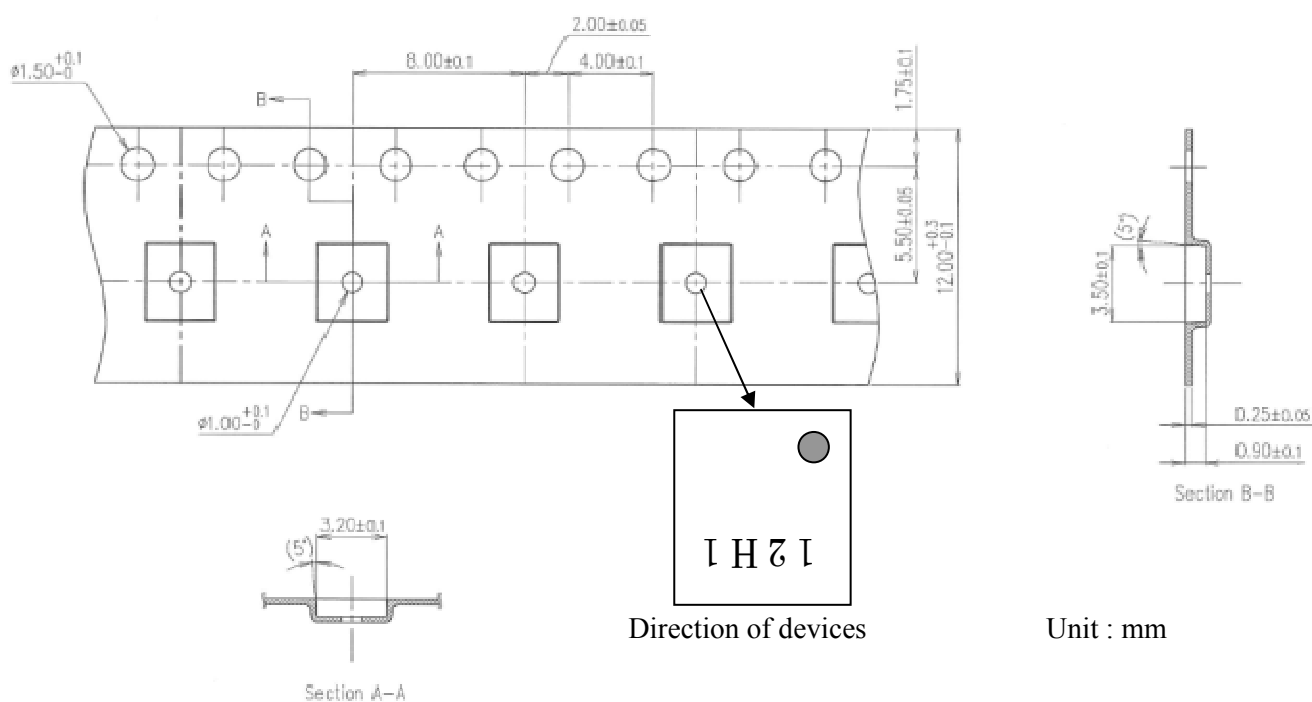


Figure 19. Dimensional drawing of carrier tape

13.2 Reel Dimensions

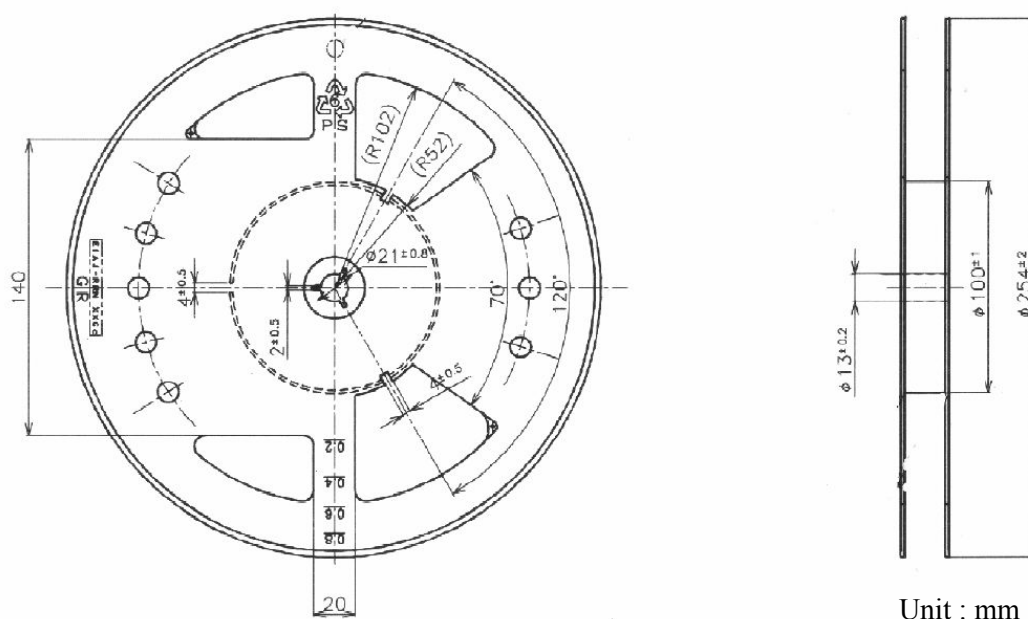


Figure 20. Dimensional drawing of reel

14. Soldering Conditions

14.1 Soldering Conditions

Reflow soldering should be performed under the following conditions.

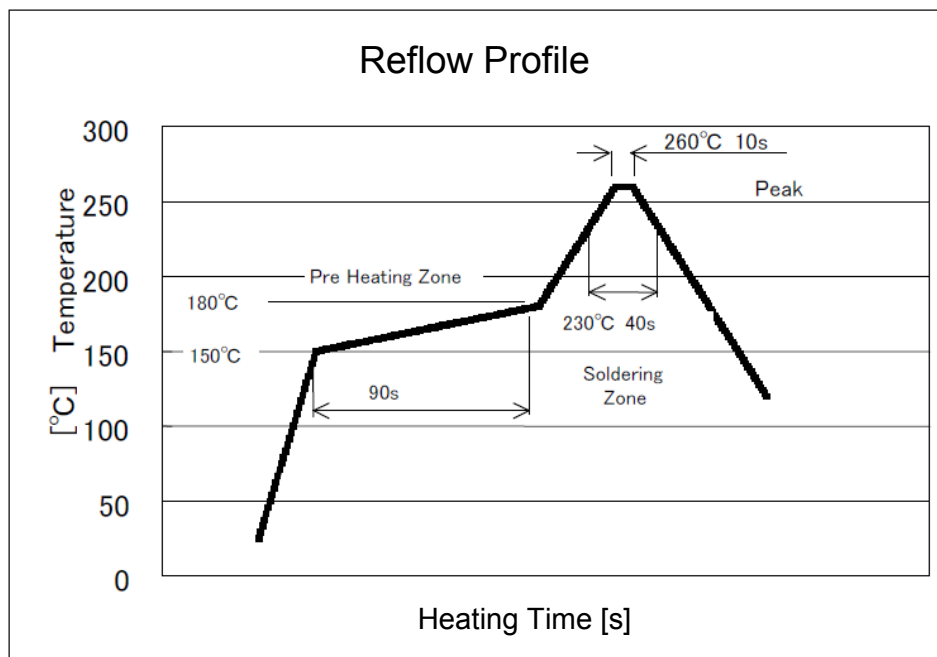


Figure 21. Reflow profile

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