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STF40N65M2

N-channel 650 V, 0.087 Ω typ., 32 A MDmesh™ M2
Power MOSFET in a TO-220FP package

Datasheet - production data

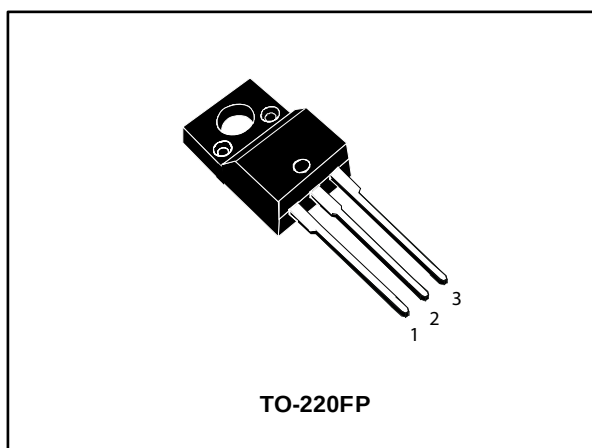
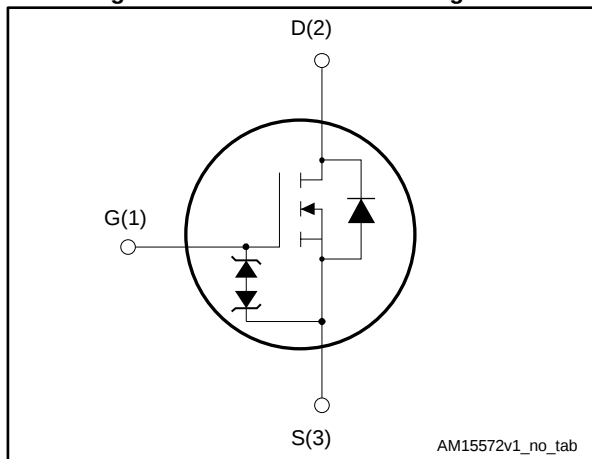


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STF40N65M2	650 V	0.099 Ω	32 A

- Extremely low gate charge
- Excellent output capacitance (C_{oss}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

Table 1: Device summary

Order code	Marking	Package	Packaging
STF40N65M2	40N65M2	TO-220FP	Tube

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Electrical ratings

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	32	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	20	A
$I_{DM}^{(2)}$	Drain current (pulsed)	128	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	25	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(4)}$	MOSFET dv/dt ruggedness	50	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$; $T_C = 25\text{ }^\circ\text{C}$)	2500	V
T_{stg}	Storage temperature	- 55 to 150	$^\circ\text{C}$
T_j	Max. operating junction temperature	150	

Notes:

⁽¹⁾Limited by maximum junction temperature.

⁽²⁾Pulse width limited by safe operating area.

⁽³⁾ $I_{SD} \leq 32\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$; $V_{DS\text{ peak}} < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$

⁽⁴⁾ $V_{DS} \leq 520\text{ V}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	3.13	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.50	$^\circ\text{C}/\text{W}$

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	3	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	820	mJ

Electrical characteristics

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2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V, I _D = 1 mA	650			V
I _{DSS}	Zero gate voltage Drain current	V _{GS} = 0 V, V _{DS} = 650 V			1	μA
		V _{GS} = 0 V, V _{DS} = 650 V, T _C = 125 °C			100	μA
I _{GSS}	Gate-body leakage current	V _{DS} = 0 V, V _{GS} = ± 25 V			±10	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2	3	4	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 16 A		0.087	0.099	Ω

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 100 V, f = 1 MHz, V _{GS} = 0 V	-	2355	-	pF
C _{oss}	Output capacitance		-	102	-	pF
C _{rss}	Reverse transfer capacitance		-	2.7	-	pF
C _{oss eq.} ⁽¹⁾	Equivalent output capacitance	V _{DS} = 0 V to 520 V, V _{GS} = 0 V	-	380	-	pF
R _G	Intrinsic gate resistance	f = 1 MHz open drain	-	4.5	-	Ω
Q _g	Total gate charge	V _{DD} = 520 V, I _D = 32 A, V _{GS} = 10 V (see Figure 15: "Gate charge test circuit")	-	56.5	-	nC
Q _{gs}	Gate-source charge		-	8	-	nC
Q _{gd}	Gate-drain charge		-	24	-	nC

Notes:

⁽¹⁾C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

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Electrical characteristics

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 325\text{ V}$, $I_D = 16\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 14: "Switching times test circuit for resistive load" and Figure 19: "Switching time waveform")	-	15	-	ns
t_r	Rise time		-	10	-	ns
$t_{d(off)}$	Turn-off-delay time		-	96.5	-	ns
t_f	Fall time		-	12	-	ns

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		32	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		128	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 32\text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 32\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times")	-	468		ns
Q_{rr}	Reverse recovery charge		-	8.7		μC
I_{RRM}	Reverse recovery current		-	37.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 32\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times")	-	610		ns
Q_{rr}	Reverse recovery charge		-	11.7		μC
I_{RRM}	Reverse recovery current		-	39		A

Notes:

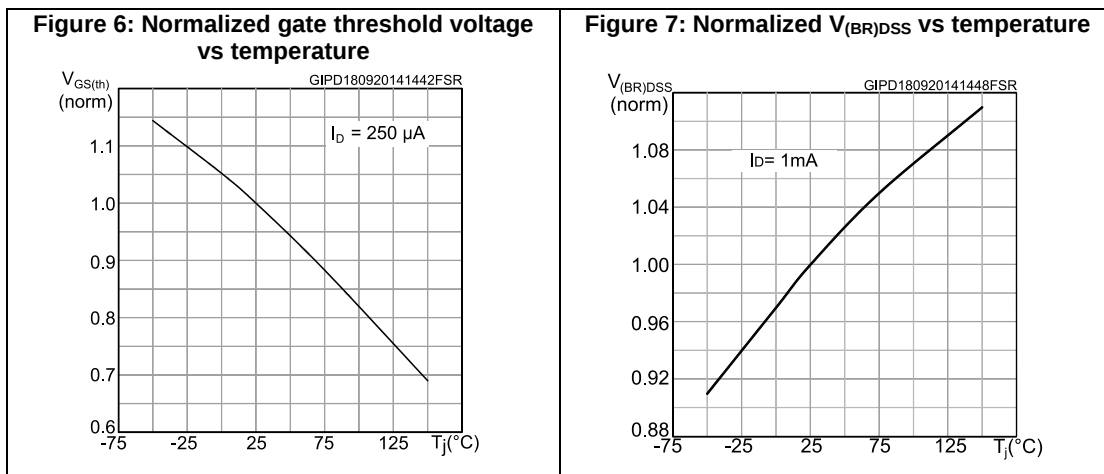
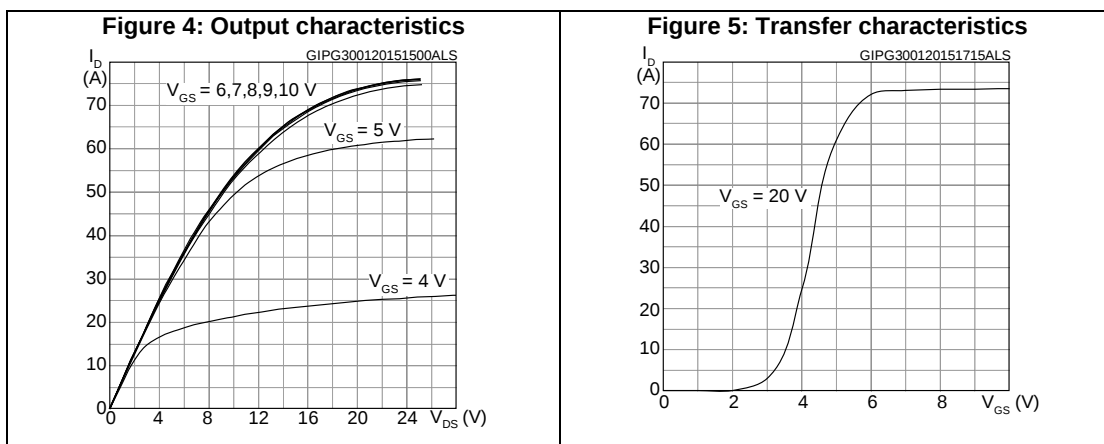
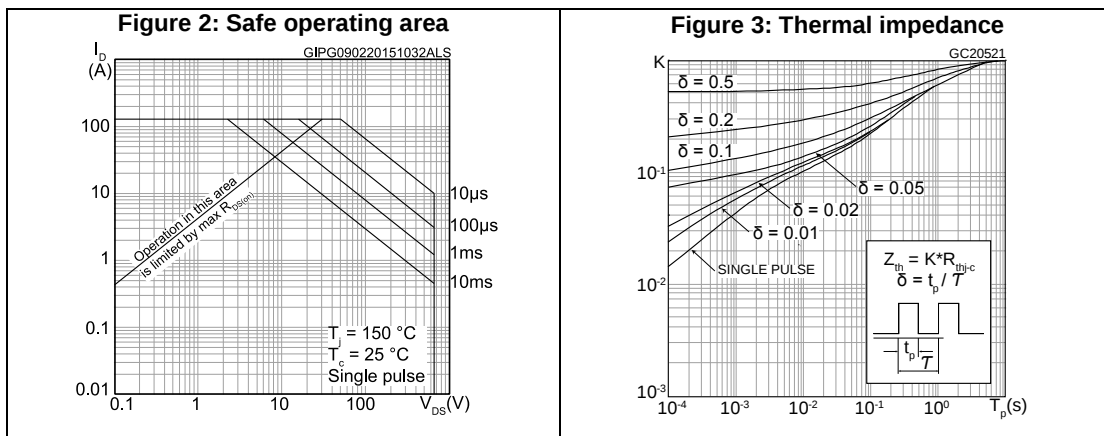
⁽¹⁾ Pulse width is limited by safe operating area

⁽²⁾ Pulse test: pulse duration = 300 μs , duty cycle 1.5%

Electrical characteristics

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2.2 Electrical characteristics (curves)



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Electrical characteristics

Figure 8: Static drain-source on-resistance

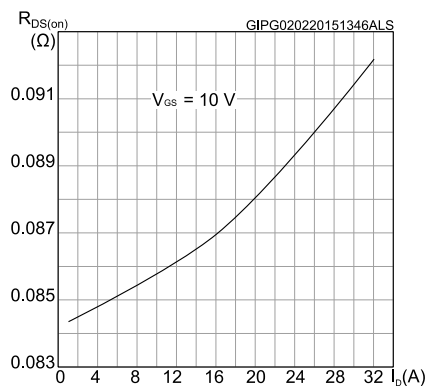


Figure 9: Normalized on-resistance vs. temperature

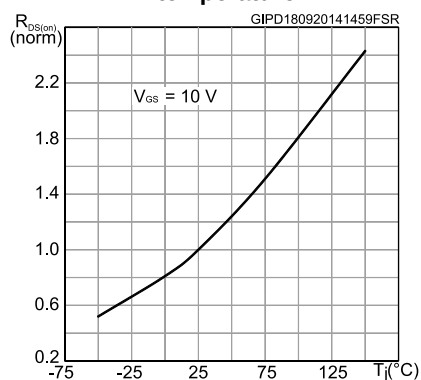


Figure 10: Gate charge vs. gate-source voltage

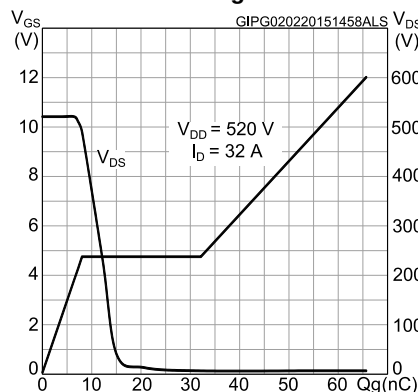


Figure 11: Capacitance variations

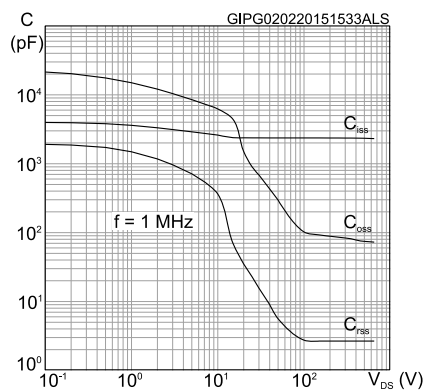


Figure 12: Output capacitance stored energy

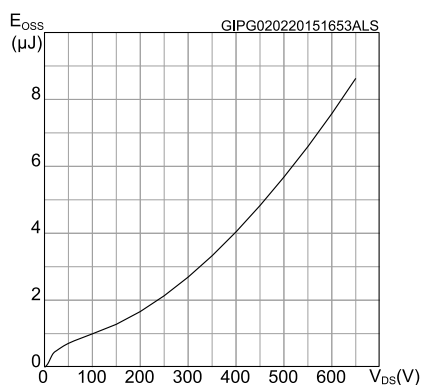
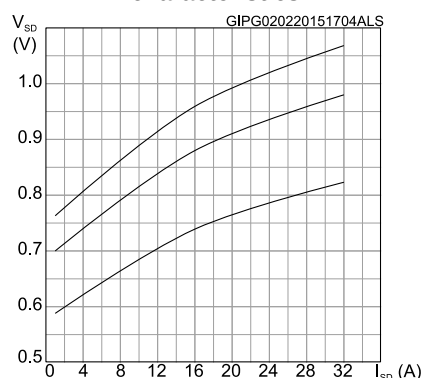


Figure 13: Source-drain diode forward characteristics



Test circuits

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3 Test circuits

Figure 14: Switching times test circuit for resistive load

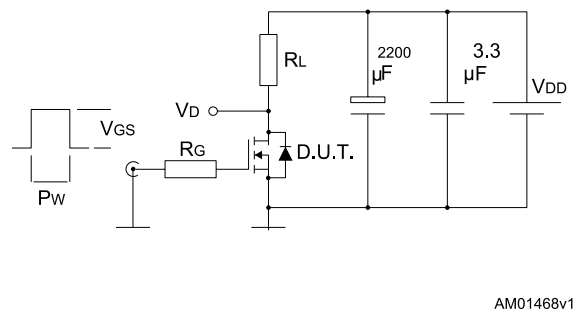


Figure 15: Gate charge test circuit

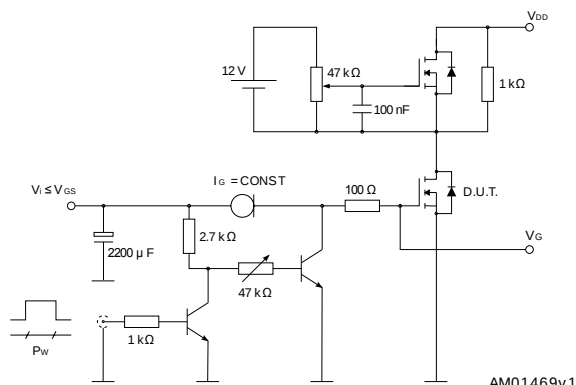


Figure 16: Test circuit for inductive load switching and diode recovery times

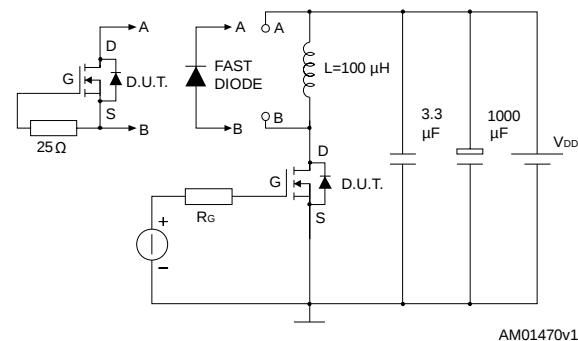


Figure 17: Unclamped inductive load test circuit

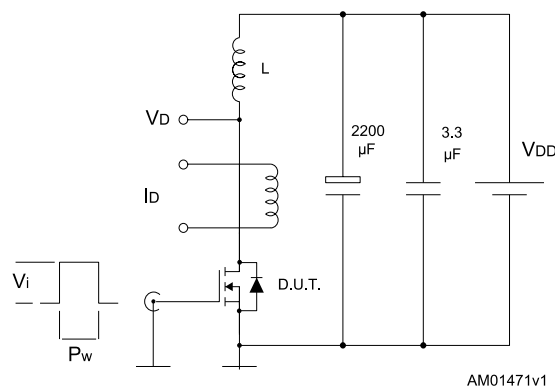


Figure 18: Unclamped inductive waveform

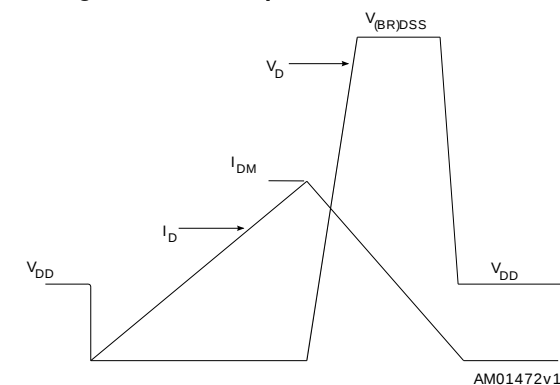
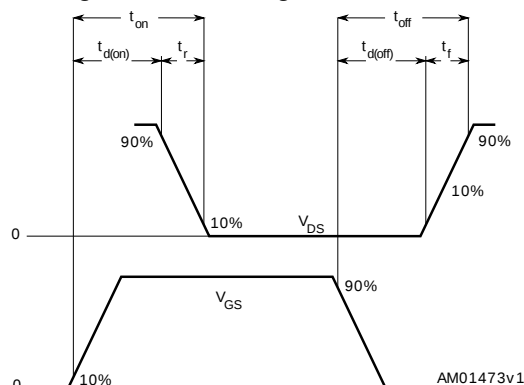


Figure 19: Switching time waveform

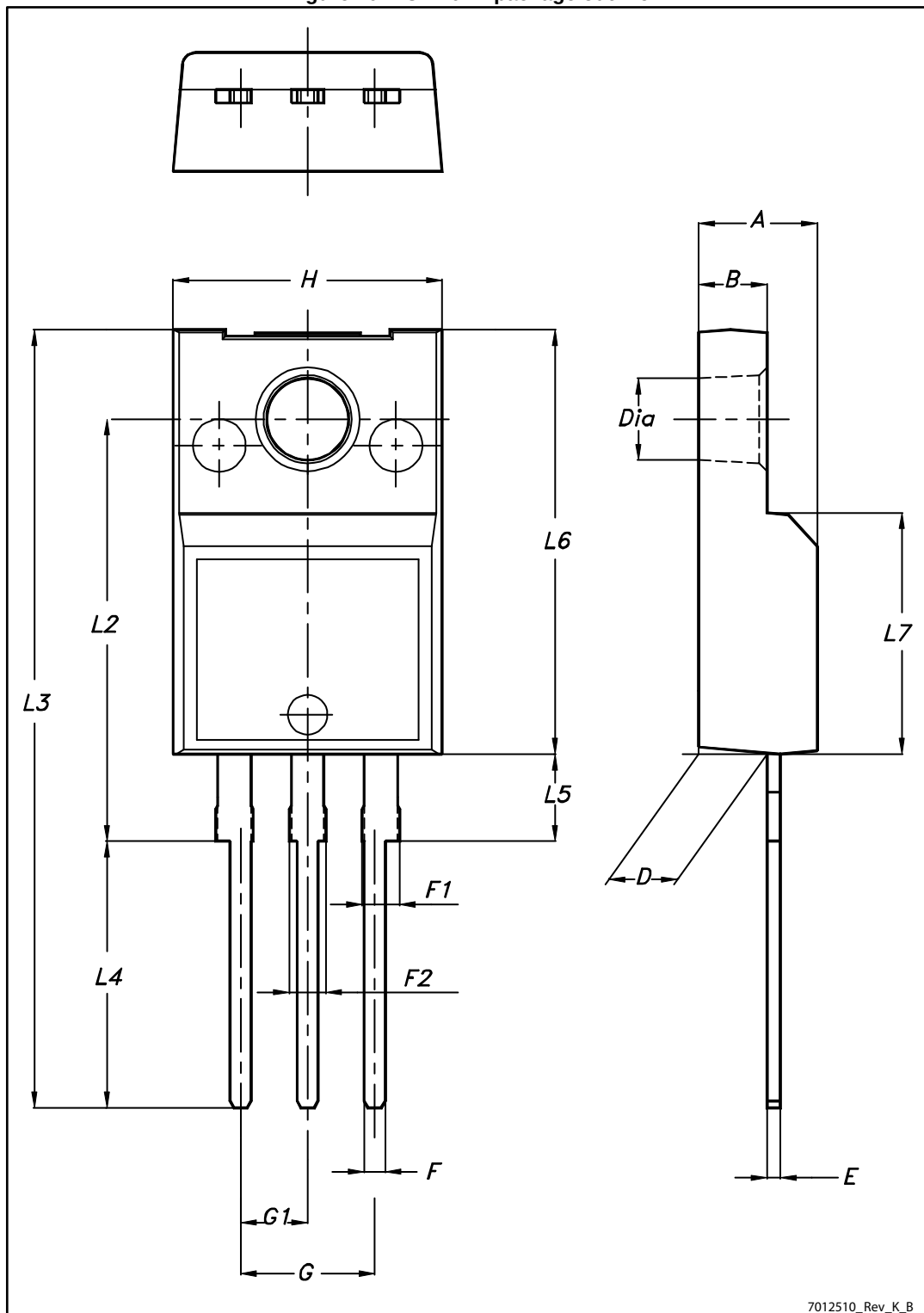


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK[®] is an ST trademark.

4.1 TO-220FP package information

Figure 20: TO-220FP package outline



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Package information

Table 9: TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
09-Feb-2014	1	First release.

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