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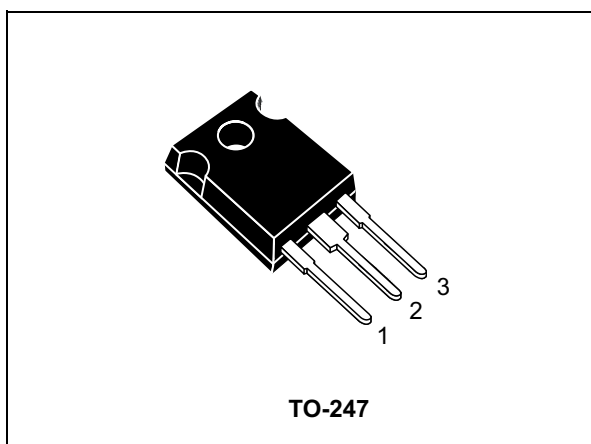
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STW56N65M2

N-channel 650 V, 0.049 Ω typ., 49 A MDmesh™ M2
 Power MOSFET in a TO-247 package

Datasheet - production data



Features

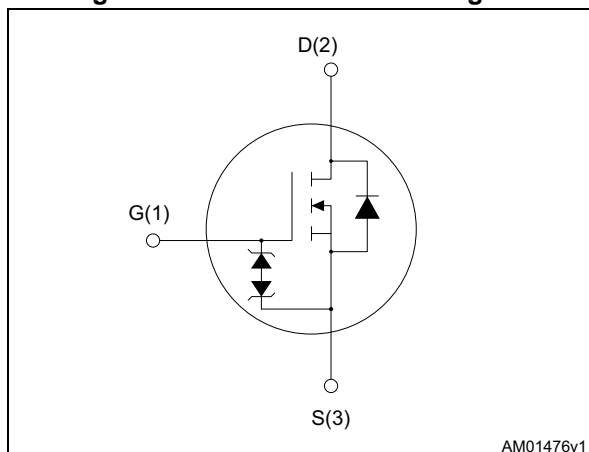
Order code	V _{DS}	R _{DS(on)} max	I _D
STW56N65M2	650 V	0.062 Ω	49 A

- Extremely low gate charge
- Excellent output capacitance (C_{oss}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Figure 1. Internal schematic diagram



Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order code	Marking	Package	Packaging
STW56N65M2	56N65M2	TO-247	Tube

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
2.1	Electrical characteristics (curves)	6
3	Test circuits	8
4	Package mechanical data	9
4.1	TO-247, STW56N65M2	9
5	Revision history	11

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{GS}	Gate- source voltage	±25	V
I _D	Drain current (continuous) at T _C = 25 °C	49	A
I _D	Drain current (continuous) at T _C = 100 °C	31	A
I _{DM} ⁽¹⁾	Drain current (pulsed)	196	A
P _{TOT}	Total dissipation at T _C = 25 °C	358	W
dv/dt ⁽²⁾	Peak diode recovery voltage slope	15	V/ns
dv/dt ⁽³⁾	MOSFET dv/dt ruggedness	50	V/ns
T _{stg}	Storage temperature	- 55 to 150	°C
T _j	Max. operating junction temperature	150	°C

1. Pulse width limited by safe operating area
2. I_{SD} ≤ 49 A, di/dt = 400 A/μs, peak V_{DS} < V_{(BR)DSS}, V_{DD} = 400 V
3. V_{DS} ≤ 520 V

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R _{thj-amb}	Thermal resistance junction-ambient max	50	°C/W
R _{thj-case}	Thermal resistance junction-case max	0.35	°C/W

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T _{JMAX})	3.5	A
E _{AS}	Single pulse avalanche energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	1300	mJ

Electrical characteristics

STW56N65M2

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0	650			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = 650 V V _{DS} = 650 V, T _C = 125 °C			1 100	μA μA
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	V _{GS} = ± 25 V			± 10	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2	3	4	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 24.5 A		0.049	0.062	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 100 V, f = 1 MHz, V _{GS} = 0	-	3900	-	pF
C _{oss}	Output capacitance		-	160	-	pF
C _{rss}	Reverse transfer capacitance		-	2.8	-	pF
C _{o(er)} ⁽¹⁾	Equivalent Output Capacitance	V _{GS} = 0, V _{DS} = 0 to 520 V	-	838	-	pF
R _G	Intrinsic gate resistance	f = 1 MHz open drain	-	4.6	-	Ω
Q _g	Total gate charge	V _{DD} = 520 V, I _D = 49 A, V _{GS} = 10 V, (see Figure 15)	-	93	-	nC
Q _{gs}	Gate-source charge		-	16	-	nC
Q _{gd}	Gate-drain charge		-	40	-	nC

1. C_{oss} eq. is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

STW56N65M2
Electrical characteristics
Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 325\text{ V}$, $I_D = 24.5\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 16 and Figure 19)	-	19	-	ns
t_r	Rise time		-	27.5	-	ns
$t_{d(off)}$	Turn-off delay time		-	146	-	ns
t_f	Fall time		-	13	-	ns

Table 8. Source drain diode

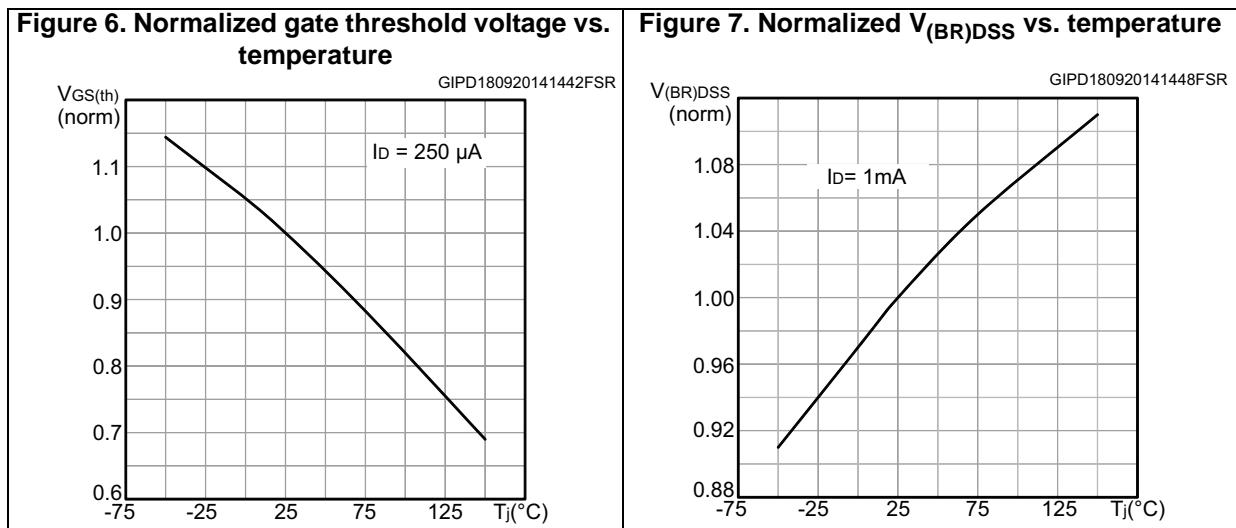
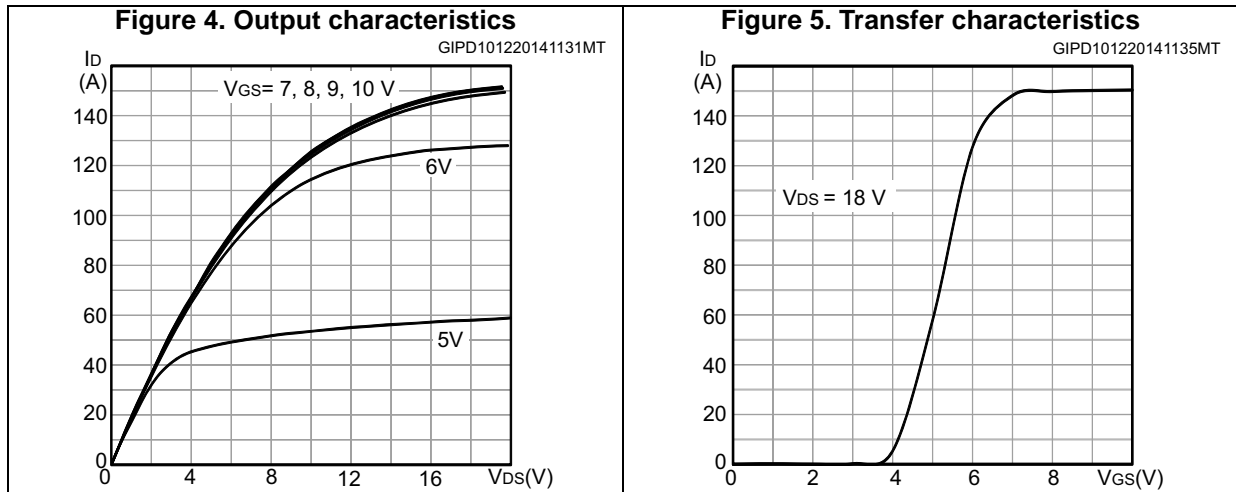
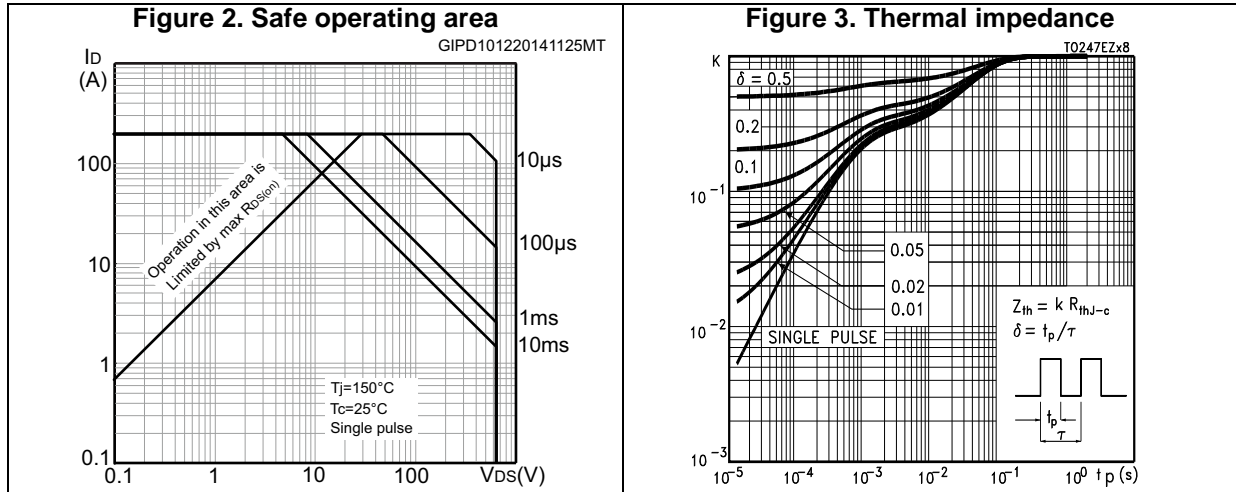
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		49	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		196	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 49\text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 49\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	-	554		ns
Q_{rr}	Reverse recovery charge		-	13.5		μC
I_{RRM}	Reverse recovery current	$V_{DD} = 60\text{ V}$ (see Figure 16)	-	49.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 49\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 19)	-	688		ns
Q_{rr}	Reverse recovery charge		-	18		μC
I_{RRM}	Reverse recovery current		-	52		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Electrical characteristics

STW56N65M2

2.1 Electrical characteristics (curves)



STW56N65M2

Electrical characteristics

Figure 8. Static drain-source on-resistance

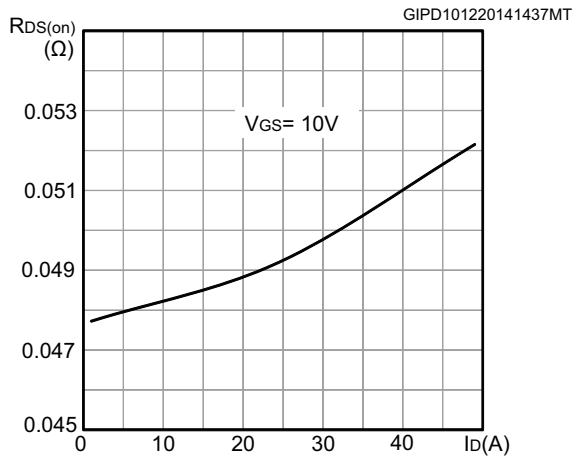


Figure 9. Normalized on-resistance vs. temperature

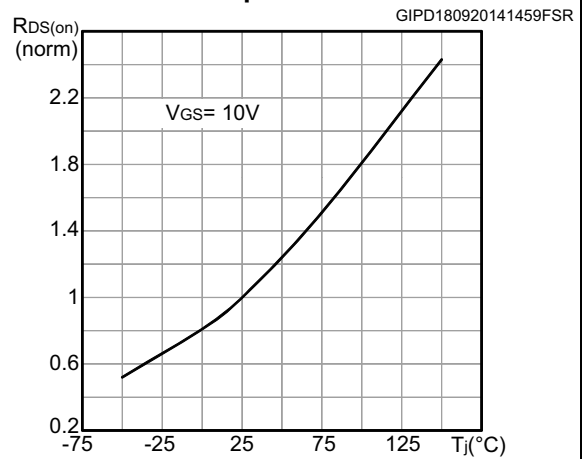


Figure 10. Gate charge vs. gate-source voltage

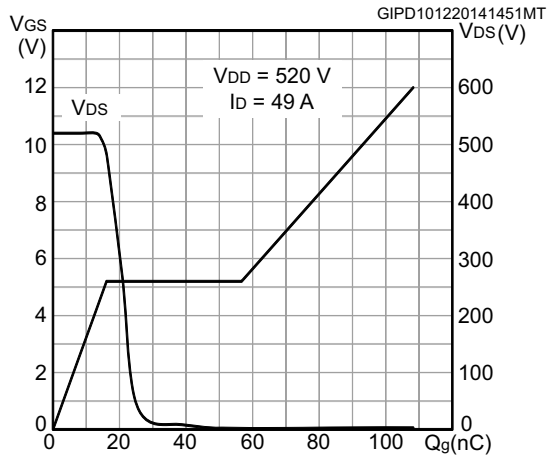


Figure 11. Capacitance variations

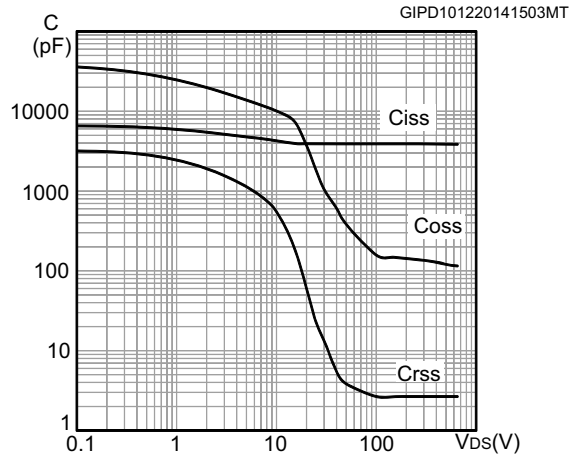


Figure 12. Output capacitance stored energy

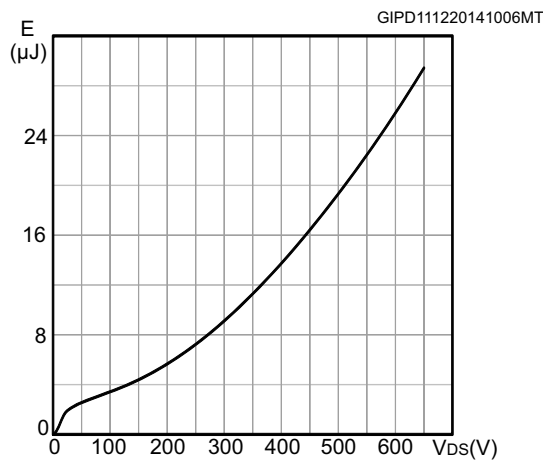
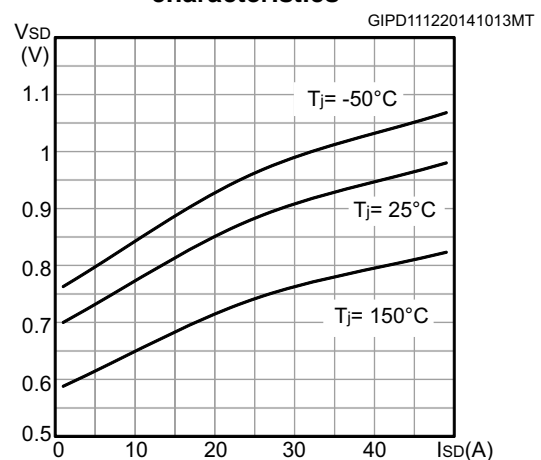
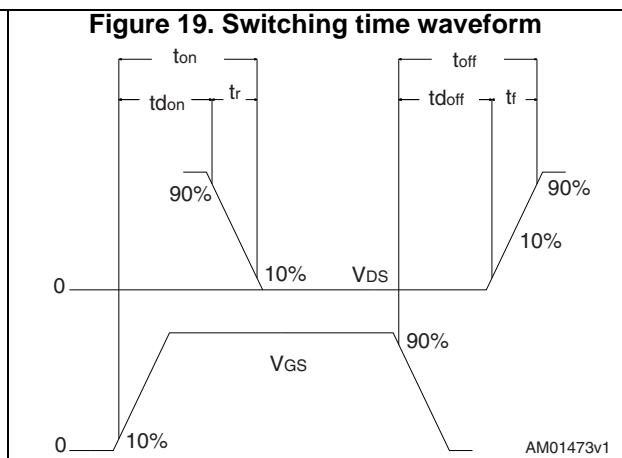
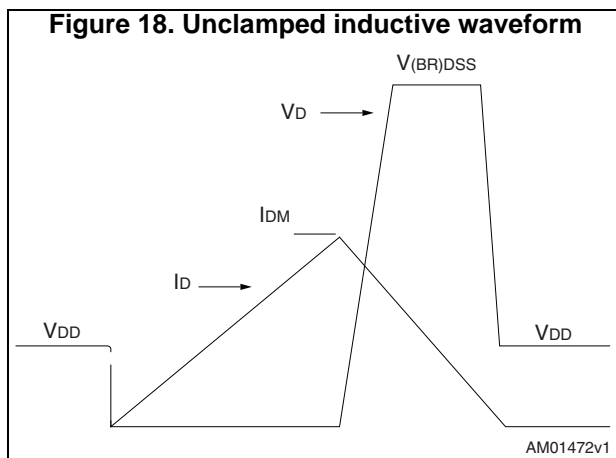
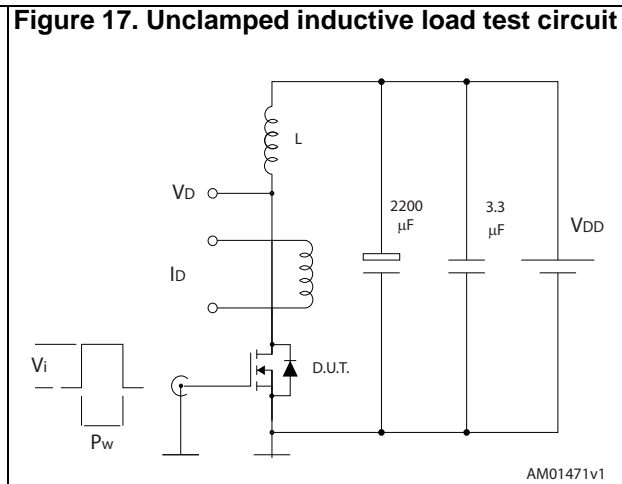
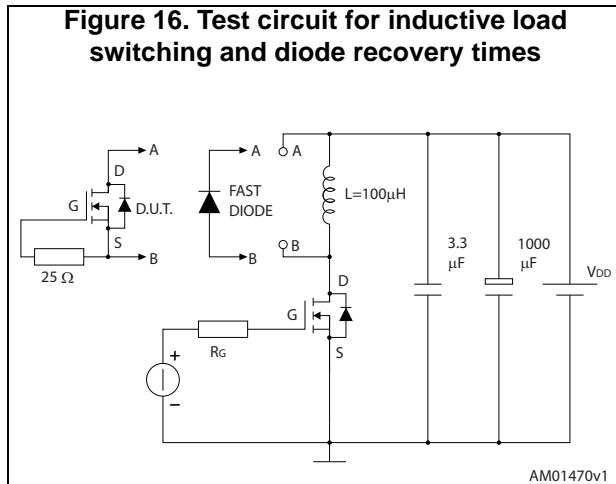
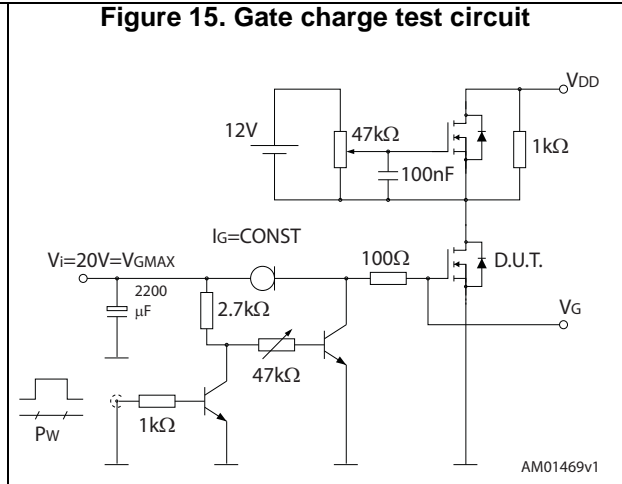
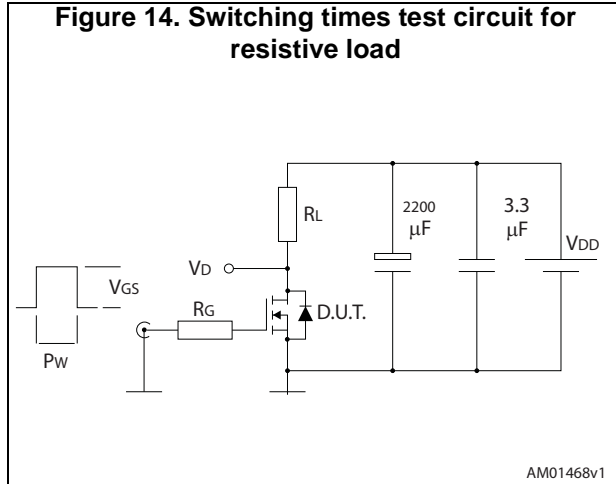


Figure 13. Source-drain diode forward characteristics



3 Test circuits

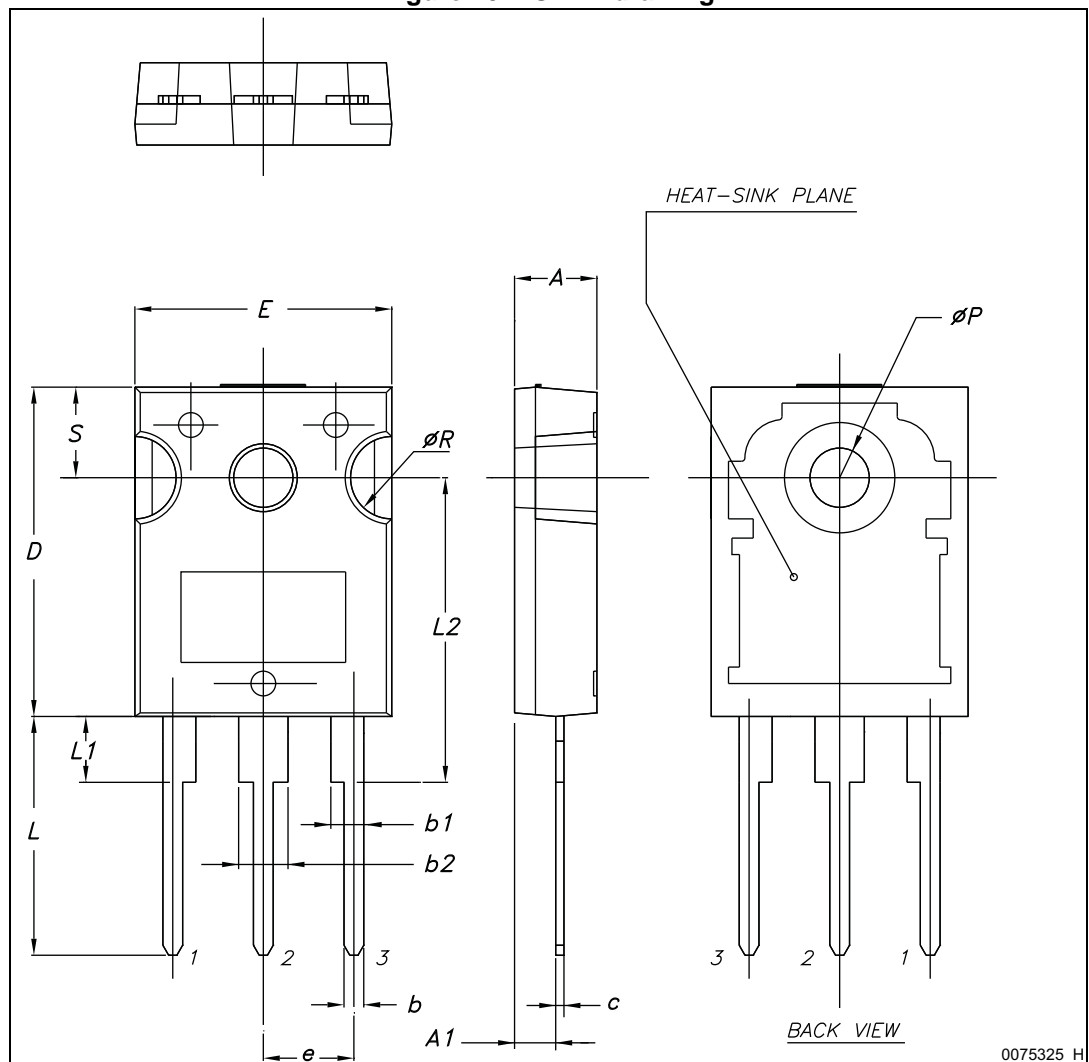


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

4.1 TO-247, STW56N65M2

Figure 20. TO-247 drawing



Package mechanical data

STW56N65M2

Table 9. TO-247 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

5 Revision history

Table 10. Document revision history

Date	Revision	Changes
10-Dec-2014	1	Initial release.

STW56N65M2

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