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VL-7709a
VL-7709b
VL-77CT09a
VL-77CT09b

64/256K Memory Card
for the STD Bus

Model VL-7709

64/256K Memory Card for the STD Bus

REFERENCE MANUAL

VL-7709a	Rev. 1.00
VL-7709b	Rev. 1.01
VL-77CT09a	Rev. 1.00
VL-77CT09b	Rev. 1.01
Doc. Rev.	9/10/93

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M7709

Model VL-7709
64/256K Memory Card

REFERENCE MANUAL

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5. Reference

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Section 1
OVERVIEW

INTRODUCTION

This manual details the installation and operation of VersaLogic's VL-7709 memory card. The VL-7709 card accepts 8K or 32K RAM and ROM devices, and is available with battery backup option for totally non-volatile operation. It features 16 and 20 bit addressing, and is compatible with all common STD Bus processor types. It is fully compatible with the Pro-Log 7709 memory board.

The "B" versions of the board (VL-7709B, VL-77CT09B) include an on-board backup battery and related support circuitry.

Throughout this manual "VL-7709" will be used to refer to all versions of the board, unless specifically noted otherwise.

OVERVIEW

The VL-7709 memory card includes eight 28-pin JEDEC sockets which can be jumpered to accept 8K or 32K memory chips. This provides a capacity of 64K (with 8K chips) or 256K (with 32K chips) of memory. RAM and ROM chips (of a similar size) can be mixed on the same board.

The board provides both 16-bit addressing (for Z80, 8085, etc.) and extended 20-bit addressing for use with STD 8088 systems. In addition, a programmable bank select port allows selection of multiple memory boards in 16-bit systems (in either 32K or 64K blocks). Multiple VL-7709 boards (up to 1M byte) can be directly addressed in 20-bit systems.

The MEMEX signal is decoded for use with bootstrap applications, or for further extending the number of boards that can be addressed.

The battery backup option provides a completely self-contained data retention system for use in nonvolatile memory applications. The long life lithium battery, and complete power monitoring circuitry allow the on-board data to be retained for 5-10 years (depending on the chips used) with or without the presence of system power.

Write inhibit switches allow on-board RAM to be protected (to act as ROM) to simplify testing during software development.

FEATURES

- 64K to 256K byte capacity.
- Eight 28-pin JEDEC memory sockets.
- Accepts 8K and 32K byte RAMs and ROMs.
- 16-bit and 20-bit address decoding.
- Bank select and MEMEX decoding.
- Optional lithium battery backup.
- Write inhibit switches.
- Extended temperature version available.
- Universal STD Bus processor compatible.
- Three year warranty.

DESCRIPTION

Addressing

Both 16 and 20-bit addressing are supported. The 20-bit mode is STD 8088 Bus compatible. It extends the system addressing capability by strobing and latching A16-A19 from the D0-D3 bus lines when operation with an 8088 CPU card. The 20-bit addressing mode allows large amounts of memory (1M bytes) to be directly addressed by the CPU.

The 16-bit addressing mode is compatible with most 8 bit CPUs (Z80, 8085, 6809, etc.). It includes a programmable memory bank control that allows these systems to address more than 64K of memory. 64 banks of 32K or 64K bytes of memory can be selected by the processor for up to 4M bytes of system memory. The Bank Control port can be addressed at any I/O location (00-FF).

Both 16 and 20-bit addressing can be extended (capacity doubled) using the MEMEX signal which is also decoded by the VL-7709.

Memory Sockets

Eight 28-pin JEDEC compatible memory sockets accept either 8K or 32K byte RAM and ROMs. Each pair of sockets can be jumper configured for RAM/ZRAM/EEROM or ROM/PROM use, and whether or not they will be powered by the on-board battery (optional) when system power is not available. Each socket can be individually disabled to remove it from the memory map. The VL-7709 board has a capacity of 64K (8K chips) or 256K bytes (32K chips) depending on the memory chips used.

Memory Chips

Memory chips used with the VL-7709 should be selected according to the capacity required (8K or 32K per socket), speed of the system CPU, and power required in standby mode (if the chip will be battery backed-up). The tables below detail these parameters.

	8085 6.25 MHz	Z80 4 MHz	Z80 6 MHz	8088 5 MHz	8088 8 MHz
Access Time (min.)	415	200	110	325	180 ns

Minimum RAM/ROM Access Times

8K RAM
Hitachi HM6264LP* (2uA)#
Toshiba TC5564PL* (.01uA)#

32K RAM
Hitachi HM62256LP* (2uA)#
Toshiba TC55257PL* (2uA)#

8K PROM
Intel 2764A
Intel 27C64*
Hitachi HN482764
Hitachi HN27C64*
AMD AM2764A
TI TMS2764

32K PROM
Intel 27256
Intel 27C256*
Hitachi HN27256
Hitachi HN27C6256*
AMD AM27256

* CMOS part. # Standby current rating.

Typical Memory Devices

Memory Mapping

With 20-bit addressing the board can be located at any 64K (with 8K chips) or 256K (with 32K chips) boundary. With 16-bit addressing the board can be configured as 64K of memory, 64K of bank selectable memory, or two overlapping 32K blocks of bank selectable memory.

Battery Backup

The battery backup option provides automatic backup power for on-board RAMs. The high capacity lithium battery assures data retention for short or long term outages (5-10 years). The backup circuitry also monitors the system power level and protects on-board RAM from spurious writes during power up and power down. A board-edge LED indicator, and Battery Low output signal allow the condition of the battery to be monitored if desired.

SPECIFICATIONS

Size: Meets all STD Bus mechanical specifications.

Storage Temperature:
- VL-7709: -40° to +75° C.
- VL-77CT09: -40° to +85° C.

Free Air Operating Temperature:
- VL-7709: 0° to +65° C.
- VL-77CT09: -40° to +85° C.

Memory Sockets: Eight 28 pin JEDEC compatible.

Power Requirements:
- VL-7709: 5V ±5% at 150 ma typ. (without on-board memory).
  5V ±5% at 175 ma typ. (with 8 low power RAMs).
- VL-77CT09: 5V ±10% at 25 ma typ. (without on-board memory).
  5V ±10% at 70 ma typ. (with 8 low power RAMs).

Battery Type: Lithium.

Battery Voltage: 3.5V nominal (2.5V min.)

Battery Capacity: 750 mAH

Data Retention Time/ Battery Life (at 25·C):
- 64K bytes (8x8K chips) @ 2uA/chip: 4 years.
- 64K bytes (8x8K chips) @ .01uA/chip: 10 years min.
- 256K bytes (8x32K chips) @ 2uA/chip: 4 years.

Section 2
OPERATION

INTRODUCTION

Since the function of the VL-7709 board is simply to hold RAM or ROM for use by the system CPU, there is very little attention needed to the board once it is installed. However, since there are several ways that the board can be configured, careful thought should be given to the board's operation before it is installed in the system.

This section briefly discusses the various options that are available with this board including 16 and 20-bit addressing, bank selection, battery backup, and the write protection switches.

Details of configuring the board for these options can be found in Section 4 of this manual.

SELECTING AN ADDRESS MODE

Address Bus

The VL-7709 operates in two address modes, 16-bit (for Z80, 8085, 6800, 6500, etc. systems) and 20-bit (for STD 8088 systems).

Most non-8088 users will select the 16-bit bit addressing mode. In this mode up to 64K bytes of memory can be directly addressed. The bank selection feature can be used to allow software selection of additional 32K or 64K blocks of memory.

In the 20-bit mode, data lines D0-D3 act as address lines A16-A19 during part of the read/write cycle and are automatically latched by the VL-7709 board. Up to 1M byte of memory can be directly addressed in this mode. Bank selection is not available.

Both addressing modes support the MEMEX control. This signal, which is usually controlled by the system CPU, allows a "main" and "secondary" memory area to be selected. It can be used for startup/bootstrap operation, or to double the amount of accessible memory in a system. See Using MEMEX in this section for further information.

Memory Chip Selection

Before the board can be configured for the desired addressing and mapping options, the type of memory chips to be used must be known. The VL-7709 supports both 8K and 32K byte types.

Only one size can be used on the board. 8K and 32K chips can not be mixed.

The selection of memory chips will normally be based on current chip pricing. An exception to this is in systems that will use larger amounts of memory. 32K chips will usually be appropriate in these cases since 256K of memory can reside on a single board, versus only 64K bytes per board using 8K chips. The extra expense of 32K chips (if any) is usually outweighed by the expense of additional memory boards, bus slots, etc.

Bank Selection

In the 16-bit addressing mode the VL-7709 supports bank selection. This method of memory expansion allows the processor to switch a number of blocks (banks) of memory in and out of its basic 64K addressing space. When a bank is selected it takes its place in the addressing space and may be read and written in normal fashion. When a different bank is selected the memory on the old bank is no longer accessible by the CPU. The data is simply retained in the bank until it is once again selected by the CPU.

The VL-7709 allows a bank size of either 32K or 64K bytes. Depending on the bank size, and the type of chips used, each bank may be physically located on the same or different VL-7709 boards.

The process of selecting a bank involves simply writing a bank number to the Bank Control port (see example below). The desired bank is immediately selected and the previously selected bank is de-selected. The VL-7709 board always selects bank 00 at power-up, or whenever the system is reset.

Note that for proper bank select operation the Bank Control port address (normally EE) must be the same on all memory cards in the system.

```
                    ; Bank selection example for Z80 CPU
                    ;
                    BankCntl  equ  EEH
                    ;
                    ;
0417 3E 02          LD A,02H            ;Select memory bank #2
0419 D3 EE          OUT (BankCntl),A
                    ;
                    ;(Continuation of program)
```

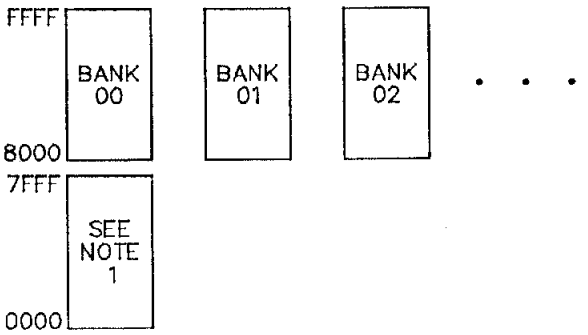
Figure 2-1. Bank Selection Example.

When using bank switching there are several special programming considerations. Most important is maintaining software continuity when switching banks. If the currently executing program is located in a bank that is being switched out of use, identical or "mating" code must be available in the new bank for the CPU to continue execution. The CPU is not aware that it is in a new memory area; it simply increments the

program counter and expects to read the next program instruction.

This software problem can be dealt with in several ways. First, by selecting a 32K bank size, only half of the memory map is switched in/out at a time. This allows the routine that does the bank switching to be located in a portion of the address space that is not being switched. A typical example is shown in Figure 2-2.

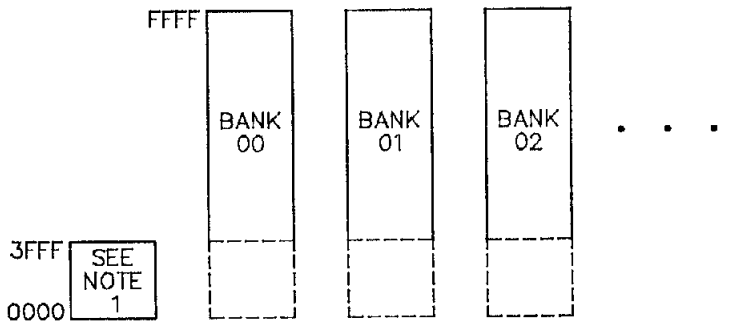
In this example the lower 32K of memory is fixed (not bank selectable). It holds the program code for bank switching so that the upper half of the map can be switched without concern for program continuity. Note that the lower 32K block must be configured for no bank selection so that it will not be switched out when the upper 32K banks are selected.



(1) Primary RAM or ROM. Contains bank switching routine.

Figure 2-2. Typical 32K Bank Switching.

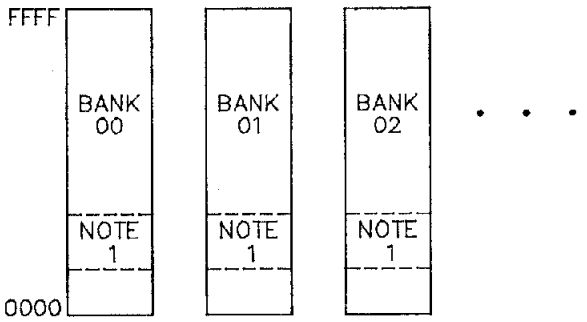
When 8K chips are used, a similar scheme can be employed by using 64K banks and de-selecting one or more chips at the bottom of each bank. This empty space in each bank can then be used for some non-bank selected memory (on a VL-7709 or the system CPU board) that can reside at the bottom of the map. The figure below illustrates this approach.



(1) Primary RAM or ROM. Appears in all banks.

Figure 2-3. 64K Banks With Chip De-Selection.

Finally, full 64K banks can be used by placing a small section of identical code (the bank switching routine) in each bank. Figure 2-4 illustrates this scheme.



(1) Bank switching routine (a copy in each bank).

Figure 2-4. 64K Bank Switching

Using MEMEX

The MEMEX (memory expansion) signal on the STD Bus can be used to select between two different memory banks or maps. It is simply another way to enable/disable certain memory board(s) in the system. It can be used to double the available memory (similar to selecting between two banks), or to control a bootstrap PROM (that disappears from the map after power-up). The MEMEX signal is usually controlled by (or jumpered to ground on) the system CPU card.

The VL-7709 decodes MEMEX in both the 16 and 20-bit addressing modes. MEMEX is usually low (default) to select the standard or normal memory map. MEMEX high typically selects a secondary or alternate memory map. Boards that ignore the state of MEMEX will appear in both memory maps.

As shipped the MEMEX jumper (V2h) is set to ignore the MEMEX signal. The VL-7709 board will be addressed whether MEMEX is high or low. Refer to MEMEX Options in the Configuration section for further information.

Since the MEMEX signal causes program memory to be switched in and out of the CPU's address space, the same software cautions apply to using MEMEX as to bank switching in general (see Bank Selection above).

BATTERY BACKUP

The "B" versions of the VL-7709 feature an on-board backup battery and associated support circuitry. The battery can backup some or all of the on-board RAM chips so that data is not lost when the system power fails.

The backup battery used on the VL-7709 is a long life lithium type. It does not require charging or setup prior to being placed in service.

The data retention (battery life) time for the battery depends primarily on the type of RAM chip used. Typical unpowered backup time is 4-10 years. Some examples are listed in Specifications in the Overview section. Note that with extremely low power RAMs, the data retention calculation must be artificially limited since the shelf life of the battery is not guaranteed past 10 years.

The power backup of on-board chips is jumper selectable for each socket pair. Each chip pair may use standard (non-backed-up) system power, or automatically backed-up power. Be certain that only sockets using RAM chips are jumpered for backup power. Jumpering PROM chips for backup power will result in unnecessary battery drain and shortened battery life.

A low battery signal and on-board LED indicator are available to indicate that the on-board battery is getting weak. The LED indicator, which is located at the edge of the board, will light whenever the battery is low and the system power is on (the LED is powered by the system, not by the battery).

The low battery signal is available at connector J1 (see Figure 3-2). It is normally used for connection to an I/O card in the system for automatic monitoring of the battery condition. This signal goes low when the battery is getting weak. The low battery signal is valid only when the system power is on.

The low battery signal occurs when the battery output falls below 2.5 volts.

For special applications the power backup circuit may be connected to an external backup battery (instead of the on-board lithium cell). The external battery must be between 3.3 and 4.5 volts. If required the VL-7709 can supply a charging current for this battery by installing the R-OPT resistor on the board.

WRITE PROTECTION SWITCHES

The VL-7709 provides four on-board switches that can write protect on-board RAM chips. The switches located at the board edge are accessible while the board is inserted in a card cage.

When the switch is up (off, open) the current contents of associated RAM chips can not be altered (written to) by the system CPU. This is useful during software development for simulating ROM based software, or for debugging software that overwrites itself in error. The switch can be set to the down (on) position at any time to allow writing to RAM.

Each write protect switch is associated with a pair of memory sockets. As shown below these pairs are identical to those controlled by the configuration jumpers (A-D).

Write Switch	Controlled Sockets
A	M0, M1
B	M2, M3
C	M4, M5
D	M6, M7

Figure 2-5. Write Protect Switch Function

Section 3
INSTALLATION

HANDLING

**** CAUTION **** The VL-7709 card uses chips which are sensitive to static electricity discharges. Normal precautions, such as discharging yourself, work stations, and tools to ground before touching the board should be taken whenever the board is handled.

The board should also be protected during shipment or storage by placing it in a conductive bag (such as the one it was received in) or by wrapping it in metal foil.

INSTALLATION

The VL-7709 card can be installed in any slot of an STD Bus card cage.

The VL-7709 does not use the STD Bus priority interrupt chain. However, the priority IN and OUT pins on this board are connected together so that the priority chain will not be broken. This board may be inserted between other boards that are using the priority chain.

**** CAUTION **** When cards are installed in an STD Bus card cage they must be oriented correctly (usually with the card ejector toward the top of the cage). Refer to the card cage documentation for the correct way to insert the STD Bus cards.

**** CAUTION **** Cards should be inserted or removed from the STD Bus card cage only when the system power is off.

Note: VL-7709B versions (with battery backup) utilize a long life lithium battery for the backup power source. This battery does not require charging or other maintenance during installation.

EXTERNAL CONNECTIONS

Connection to the low battery indicator signal (J1) on the VL-7709B board can be made with the mating connector listed below. Connector J1 is a two-pin right angle header which is accessible at the outside edge of the board. Pin one, marked with a dot, is oriented nearest to the card ejector.

VL-7709B Connector	Mating Connector
J1	AMP #530554-1 + (2) #530553-5 or equiv. two-pin connector.

Figure 3-1. VL-7709B I/O Connector.

J1 Pin	Signal Name	Output Drive (Sink ma)
1	GND	-
2	LOW BATTERY*	5 ma

Figure 3-2. Low Battery Connector (J1) Pinout.

Section 4
CONFIGURATION

JUMPER SUMMARY

Various options available on the VL-7709 card are selected using removable jumper plugs (shorting plugs). Features are selected or deselected by installing or removing the jumper plugs as noted. The terms "IN" or "JUMPED" are used to indicate an installed plug. "OUT" or "OPEN" indicates the absence of a jumper plug.

Figure 4-1 shows the jumper block locations on the VL-7709 board. It indicates the position of the jumper plugs as shipped from the factory. The function of each jumper block is detailed in Figure 4-2.

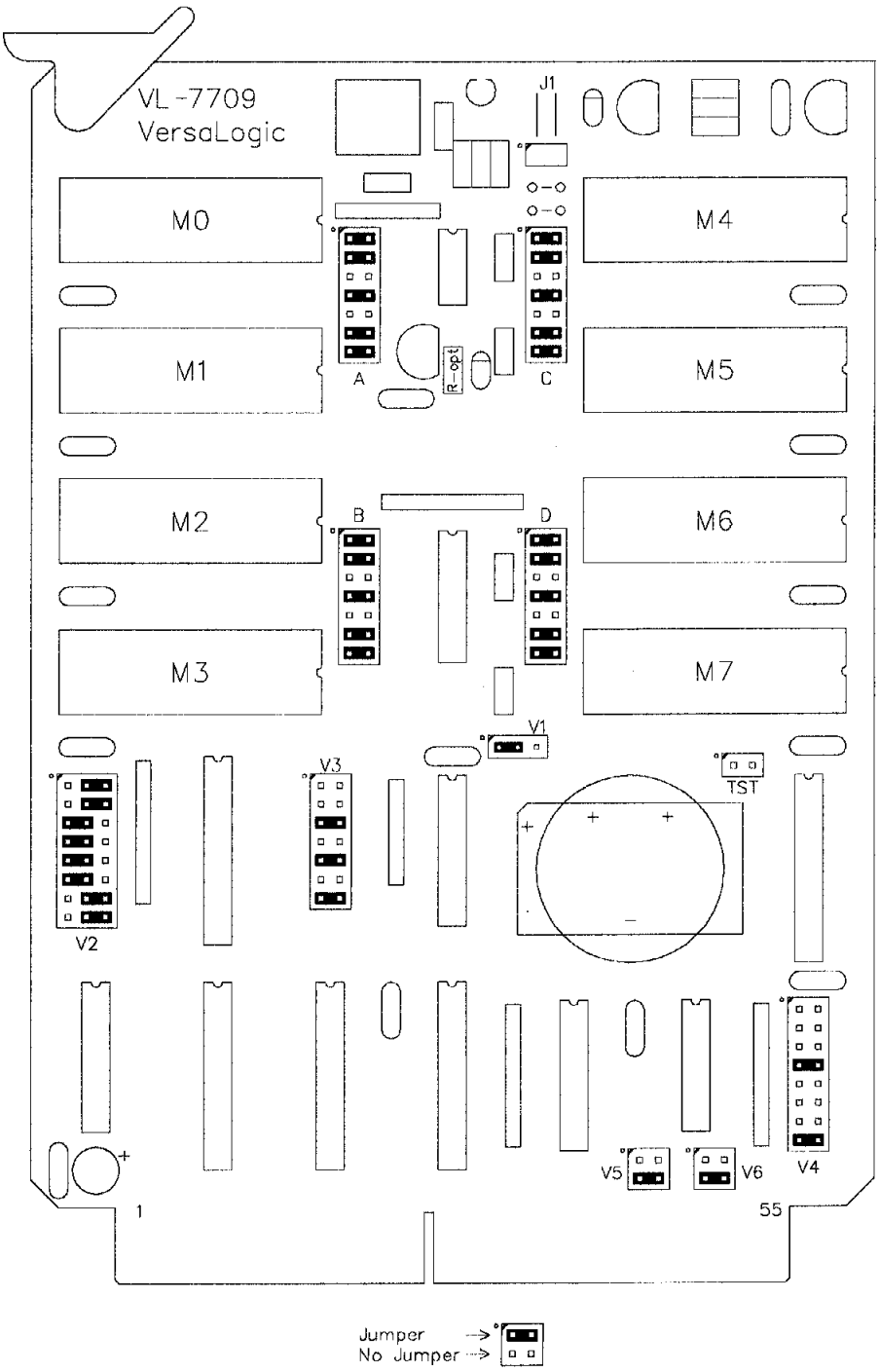


Figure 4-1. Jumper Block Locations

Jumper Block	Description	As Shipped
A-D	Memory socket options. See Memory Socket Configuration section.	All 8K RAMs
V1	Battery backup source. (VL-7709B version) a - Off-board (STD pin 5). b - On-board battery	 a - IN b - out
V2	Board Address. See addressing sections.	
V3	Memory map selection. a, d, f - 32K parts in a 256K block. b, e, g - 8K parts, 32K blocks, bank sel. c, e, g - 8K parts in a 64K block.	 out out IN
V4	Bank Control port I/O address. See Bank Control Port Address section.	Hex EE
V5	IOEXP select (for Bank Control port). a - Active high. b - Active low. - - Don't care (both jumpers out).	 a - out b - IN
V6	Addressing mode. a - 20-bit (8088) b - 16-bit with bank select. - - 16-bit without bank select (no jumpers).	 a - out b - IN

Figure 4-2. Jumper Functions

MEMORY CONFIGURATION

The VL-7709 has eight on-board memory sockets which can accommodate 8K or 32K byte RAM and ROM devices. RAMs and ROMs of the same size can be mixed on the board. Individual memory sockets can be disabled to remove them from the memory map.

The board can be addressed with 16 or 20-bit addressing with bank selection available in the 16-bit mode.

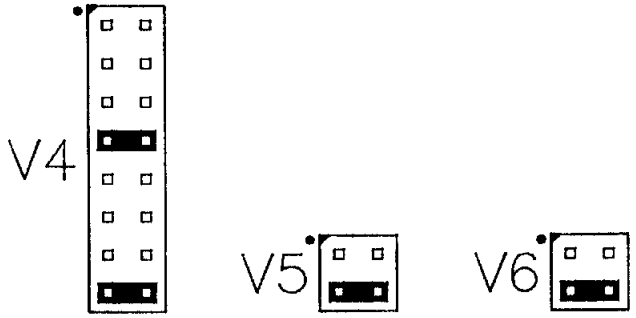
The jumpers needed to make these selections are detailed below. See the Operation section for more information on selecting and using these address modes.

When selecting the desired memory map, note that the addressing jumpers determine only the memory space that is reserved for each memory socket. Whether or not the socket is enabled, and whether a socket holds RAM or ROM, is determined by the memory socket jumpers (jumper blocks A-D) which are discussed later in this section.

16-BIT ADDRESS

The 16-bit addressing mode is available for use with most STD Bus systems with 8-bit CPU cards including Z80, 8085, 6800, and 6500 types. In this mode up to 64K of memory can be directly addressed by the processor. Bank selection, provided by the VL-7709 card, allows multiple banks of memory to be switched in and out of the CPU's address space. A new memory bank is enabled by writing to the Bank Control port. Up to 4M bytes of memory can be accessed by the CPU using this method.

To jumper the board for the 16-bit addressing mode set jumpers V4-V6 as shown below.



Jumper Block	Description	Setting
V2	Board Address and MEMEX.	Refer To Text
V3	Memory map selection. a, d, f - 32K parts, 256K block b, e, g - 8K parts, 32K blocks, bank sel. c, e, g - 8K parts, 64K block.	Refer To Text
V4	Bank Control port I/O address. See Bank Control Port Address for special configurations.	(Port EE) a-c - out d - IN e-g - out h - IN
V5	IOEXP select (for Bank Control port). a - Active high. b - Active low. - - Either (both jumpers out).	a - out b - IN
V6	Addressing mode. a - 20-bit (8088) b - 16-bit with bank select. - - 16-bit without bank select (no jumpers).	a - out b - IN

Figure 4-3. 16-bit Address Mode Selection

16-bit Address With 8K Chips

When 16-bit addressing and 8K chips are used the board can hold up to 64K bytes of memory. This can be arranged as one 64K block (with or without bank selection), or two 32K blocks (at the same address) with bank selection. These options are discussed separately below.

64K Bank

When 16-bit addressing with 8K chips will be used in a single 64K block (the most standard configuration) set jumper blocks V2 and V3 as shown below.

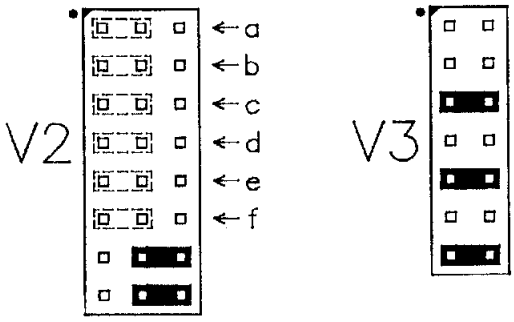
If bank switching is not needed jumpers V2a-f should all be installed (bank zero). Otherwise jumpers V2a-f should be set to select the board for the desired bank number as shown in Figure 4-5. Figure 4-4 details the address of each memory socket on the board.

The Bank Control port is initialized to bank zero when power is applied to the system. This will change only if data is written to the Bank Control port (I/O port EE as shipped). If desired the Bank Control port can be disabled completely. Refer to the Bank Control Port Address section for further details.

This jumper configuration ignores the state of the MEMEX signal in addressing the board. For systems that will use MEMEX, refer to the MEMEX Options section.

Memory Socket							
0	1	2	3	4	5	6	7
0000-1FFF	2000-3FFF	4000-5FFF	6000-7FFF	8000-9FFF	A000-BFFF	C000-DFFF	E000-FFFF

Figure 4-4. 8K Chip / 64K Bank Memory Map



V2 a	V2 b	V2 c	V2 d	V2 e	V2 f	Memory Bank	V2 a	V2 b	V2 c	V2 d	V2 e	V2 f	Memory Bank
X	X	X	X	X	X	00*	-	X	X	X	X	X	20
X	X	X	X	X	-	01	-	X	X	X	X	-	21
X	X	X	X	-	X	02	-	X	X	X	-	X	22
X	X	X	X	-	-	03	-	X	X	X	-	-	23
X	X	X	-	X	X	04	-	X	X	-	X	X	24
X	X	X	-	X	-	05	-	X	X	-	X	-	25
X	X	X	-	-	X	06	-	X	X	-	-	X	26
X	X	X	-	-	-	07	-	X	X	-	-	-	27
X	X	-	X	X	X	08	-	X	-	X	X	X	28
X	X	-	X	X	-	09	-	X	-	X	X	-	29
X	X	-	X	-	X	0A	-	X	-	X	-	X	2A
X	X	-	X	-	-	0B	-	X	-	X	-	-	2B
X	X	-	-	X	X	0C	-	X	-	-	X	X	2C
X	X	-	-	X	-	0D	-	X	-	-	X	-	2D
X	X	-	-	-	X	0E	-	X	-	-	-	X	2E
X	X	-	-	-	-	0F	-	X	-	-	-	-	2F
X	-	X	X	X	X	10	-	-	X	X	X	X	30
X	-	X	X	X	-	11	-	-	X	X	X	-	31
X	-	X	X	-	X	12	-	-	X	X	-	X	32
X	-	X	X	-	-	13	-	-	X	X	-	-	33
X	-	X	-	X	X	14	-	-	X	-	X	X	34
X	-	X	-	X	-	15	-	-	X	-	X	-	35
X	-	X	-	-	X	16	-	-	X	-	-	X	36
X	-	X	-	-	-	17	-	-	X	-	-	-	37
X	-	-	X	X	X	18	-	-	-	X	X	X	38
X	-	-	X	X	-	19	-	-	-	X	X	-	39
X	-	-	X	-	X	1A	-	-	-	X	-	X	3A
X	-	-	X	-	-	1B	-	-	-	X	-	-	3B
X	-	-	-	X	X	1C	-	-	-	-	X	X	3C
X	-	-	-	X	-	1D	-	-	-	-	X	-	3D
X	-	-	-	-	X	1E	-	-	-	-	-	X	3E
X	-	-	-	-	-	1F	-	-	-	-	-	-	3F

* Use bank 00 if bank switching will not be used.
X = Install jumper in location shown
- = Remove jumper

Figure 4-5. 8K Chip / 64K Bank Addressing

32K Banks

16-bit addressing with 8K chips can also be configured as two 32K memory banks. In this mode both 32K blocks occupy the same memory space, and switching between them is accomplished with the Bank Control port. To select this mode set jumper blocks V2 and V3 as shown below.

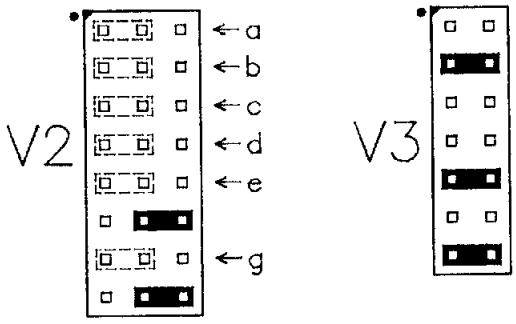
Jumpers V2a-e are used to select the board for the desired banks as shown in Figure 4-6. Jumper V2g is used to select one of the two memory maps detailed in Figure 4-6.

This jumper configuration ignores the state of the MEMEX signal in addressing the board. For systems that will use MEMEX, refer to the MEMEX Options section.

Map#	Memory Socket							
	0	1	2	3	4	5	6	7
	Odd Bank				Even Bank			
0*	0000-1FFF	2000-3FFF	4000-5FFF	6000-7FFF	0000-1FFF	2000-3FFF	4000-5FFF	6000-7FFF
1*	8000-9FFF	A000-BFFF	C000-DFFF	E000-FFFF	8000-9FFF	A000-BFFF	C000-DFFF	E000-FFFF

* Map 0 - V2g installed as shown below.
Map 1 - V2g removed.

Figure 4-6. 8K Chip / 32K Bank Memory Map



V2					32K BANK Memory Socket	
a	b	c	d	e	0-3	4-7
X	X	X	X	X	01	00
X	X	X	X	-	03	02
X	X	X	-	X	05	04
X	X	X	-	-	07	06
X	X	-	X	X	09	08
X	X	-	X	-	0B	0A
X	X	-	-	X	0D	0C
X	X	-	-	-	0F	0E
X	-	X	X	X	11	10
X	-	X	X	-	13	12
X	-	X	-	X	15	14
X	-	X	-	-	17	16
X	-	-	X	X	19	18
X	-	-	X	-	1B	1A
X	-	-	-	X	1D	1C
X	-	-	-	-	1F	1E
-	X	X	X	X	21	20
-	X	X	X	-	23	22
-	X	X	-	X	25	24
-	X	X	-	-	27	26
-	X	-	X	X	29	28
-	X	-	X	-	2B	2A
-	X	-	-	X	2D	2C
-	X	-	-	-	2F	2E
-	-	X	X	X	31	30
-	-	X	X	-	33	32
-	-	X	-	X	35	34
-	-	X	-	-	37	36
-	-	-	X	X	39	38
-	-	-	X	-	3B	3A
-	-	-	-	X	3D	3C
-	-	-	-	-	3F	3E

X = Install jumper in location shown
- = Remove jumper

Figure 4-7. 8K Chip / 32K Bank Addressing

16-Bit Address With 32K Chips

When 16-bit addressing and 32K chips are used, up to four 64K banks of memory can be addressed on the board. Each pair of sockets is addressed as a different memory bank. Multiple boards can be used to address additional 64K banks of memory. By disabling every other socket, this same mode can be used to address 32K banks of memory (four per board).

64K Banks

To use 16-bit addressing with 32K chips set jumper blocks V2 and V3 as shown below.

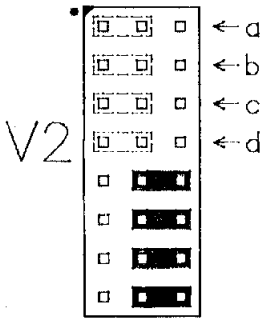
If bank switching is not needed jumpers V2a-d should all be installed (map 0) and only sockets 0 and 1 should be used. Otherwise jumpers V2a-d should be set to select the board for the desired bank number as shown in Figure 4-9. Figure 4-8 details the address and bank of each memory socket (example shown is for Map 0).

The Bank Control port is initialized to bank zero when power is applied to the system. This will change only if data is written to the Bank Control port (I/O port EE as shipped). If desired the Bank Control port can be disabled completely. Refer to the Bank Control Port Address section for further details.

This jumper configuration ignores the state of the MEMEX signal in addressing the board. For systems that will use MEMEX, refer to the MEMEX Options section.

Memory Socket							
0	1	2	3	4	5	6	7
--Bank 00--		--Bank 01--		--Bank 02--		--Bank 03--	
0000-7FFF	8000-FFFF	0000-7FFF	8000-FFFF	0000-7FFF	8000-FFFF	0000-7FFF	8000-FFFF

Figure 4-8. 32K Chip / 64K Bank Memory Map



V2				Map#	MEMORY BANKS —Memory Sockets—			
a	b	c	d		0–1	2–3	4–5	6–7
X	X	X	X	0*	00	01	02	03
X	X	X	–	1	04	05	06	07
X	X	–	X	2	08	09	0A	0B
X	X	–	–	3	0C	0D	0E	0F
X	–	X	X	4	10	11	12	13
X	–	X	–	5	14	15	16	17
X	–	–	X	6	18	19	1A	1B
X	–	–	–	7	1C	1D	1E	1F
–	X	X	X	8	20	21	22	23
–	X	X	–	9	24	25	26	27
–	X	–	X	A	28	29	2A	2B
–	X	–	–	B	2C	2D	2E	2F
–	–	X	X	C	30	31	32	33
–	–	X	–	D	34	35	36	37
–	–	–	X	E	38	39	3A	3B
–	–	–	–	F	3C	3D	3E	3F

* Use Map 0 if bank switching will not be used.
X = Install jumper in location shown
– = Remove jumper

Figure 4-9. 32K Chip / 64K Bank Addressing

32K Banks

The use of 32K chips in 32K banks is not specifically supported by the VL-7709. However, it can be easily accomplished by jumpering the board for 64K banks (see section above) and disabling every other socket (see Disabling Unused Sockets).

See the Operation section for general information on using bank selection.

20-BIT ADDRESS

The 20-bit addressing mode is available for systems using STD 8088 type processor boards. In this mode either 8K or 32K byte chips can be used on board for a maximum capacity of 64K or 256K respectively.

20-bit addressing allows multiple VL-7709 boards to be used in a system, with the CPU directly addressing of up to 1M bytes of memory.

To jumper the board for the 20-bit addressing mode set jumpers V6 as shown below.

Jumper Block	Description	Setting
V2	Board Address and MEMEX.	REFER TO TEXT
V3	Memory map selection. a, d, f - 32K parts, 256K block b, e, g - 8K parts, 32K blocks, bank sel. c, e, g - 8K parts, 64K block.	Depends on chips used REFER TO TEXT
V4	Bank Control port I/O address. Ignored. Any jumpers are acceptable.	ANY
V5	IOEXP select (for Bank Control port). Ignored. Any jumpers are acceptable.	ANY
V6	Addressing mode. a - 20-bit (8088) b - 16-bit with bank select. - - 16-bit without bank select (no jumpers).	a - IN b - out

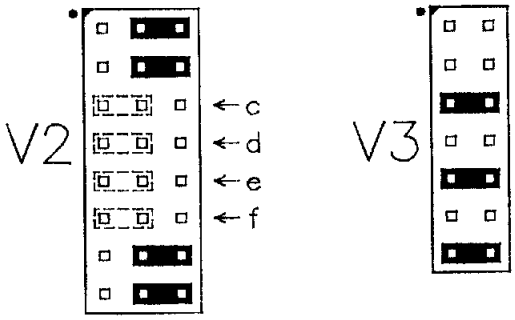
Figure 4-10. 20-Bit Address Mode Selection

20-Bit Address With 8K Chips

To use 8K chips with 20-bit addressing, set jumper blocks V2 and V3 as shown below.

Jumpers V2c-f should be set for the desired board address as shown in Figure 4-11. Figure 4-12 details the resulting address of each memory socket in the selected memory map.

This jumper configuration ignores the state of the MEMEX signal in addressing the board. For systems that will use MEMEX, refer to the MEMEX Options section.



V2					
c	**d**	**e**	**f**	**Map#**	**Address Range**
X	X	X	X	0	00000-0FFFF
X	X	X	-	1	10000-1FFFF
X	X	-	X	2	20000-2FFFF
X	X	-	-	3	30000-3FFFF
X	-	X	X	4	40000-4FFFF
X	-	X	-	5	50000-5FFFF
X	-	-	X	6	60000-6FFFF
X	-	-	-	7	70000-7FFFF
-	X	X	X	8	80000-8FFFF
-	X	X	-	9	90000-9FFFF
-	X	-	X	A	A0000-AFFFF
-	X	-	-	B	B0000-BFFFF
-	-	X	X	C	C0000-CFFFF
-	-	X	-	D	D0000-DFFFF
-	-	-	X	E	E0000-EFFFF
-	-	-	-	F	F0000-FFFFF

X = Install jumper in location shown
- = Remove jumper

Figure 4-11. 20-Bit / 8K Chip Addressing

	Memory Socket							
Map#	0	1	2	3	4	5	6	7
0	00000-01FFF	02000-03FFF	04000-05FFF	06000-07FFF	08000-09FFF	0A000-0BFFF	0C000-0DFFF	0E000-0FFFF
1	10000-11FFF	12000-13FFF	14000-15FFF	16000-17FFF	18000-19FFF	1A000-1BFFF	1C000-1DFFF	1E000-1FFFF
2	20000-21FFF	22000-23FFF	24000-25FFF	26000-27FFF	28000-29FFF	2A000-2BFFF	2C000-2DFFF	2E000-2FFFF
3	30000-31FFF	32000-33FFF	34000-35FFF	36000-37FFF	38000-39FFF	3A000-3BFFF	3C000-3DFFF	3E000-3FFFF
4	40000-41FFF	42000-43FFF	44000-45FFF	46000-47FFF	48000-49FFF	4A000-4BFFF	4C000-4DFFF	4E000-4FFFF
5	50000-51FFF	52000-53FFF	54000-55FFF	56000-57FFF	58000-59FFF	5A000-5BFFF	5C000-5DFFF	5E000-5FFFF
6	60000-61FFF	62000-63FFF	64000-65FFF	66000-67FFF	68000-69FFF	6A000-6BFFF	6C000-6DFFF	6E000-6FFFF
7	70000-71FFF	72000-73FFF	74000-75FFF	76000-77FFF	78000-79FFF	7A000-7BFFF	7C000-7DFFF	7E000-7FFFF
8	80000-81FFF	82000-83FFF	84000-85FFF	86000-87FFF	88000-89FFF	8A000-8BFFF	8C000-8DFFF	8E000-8FFFF
9	90000-91FFF	92000-93FFF	94000-95FFF	96000-97FFF	98000-99FFF	9A000-9BFFF	9C000-9DFFF	9E000-9FFFF
A	A0000-A1FFF	A2000-A3FFF	A4000-A5FFF	A6000-A7FFF	A8000-A9FFF	AA000-ABFFF	AC000-ADFFF	AE000-AFFFF
B	B0000-B1FFF	B2000-B3FFF	B4000-B5FFF	B6000-B7FFF	B8000-B9FFF	BA000-BBFFF	BC000-BDFFF	BE000-BFFFF
C	C0000-C1FFF	C2000-C3FFF	C4000-C5FFF	C6000-C7FFF	C8000-C9FFF	CA000-CBFFF	CC000-CDFFF	CE000-CFFFF
D	D0000-D1FFF	D2000-D3FFF	D4000-D5FFF	D6000-D7FFF	D8000-D9FFF	DA000-DBFFF	DC000-DDFFF	DE000-DFFFF
E	E0000-E1FFF	E2000-E3FFF	E4000-E5FFF	E6000-E7FFF	E8000-E9FFF	EA000-EBFFF	EC000-EDFFF	EE000-EFFFF
F	F0000-F1FFF	F2000-F3FFF	F4000-F5FFF	F6000-F7FFF	F8000-F9FFF	FA000-FBFFF	FC000-FDFFF	FE000-FFFFF

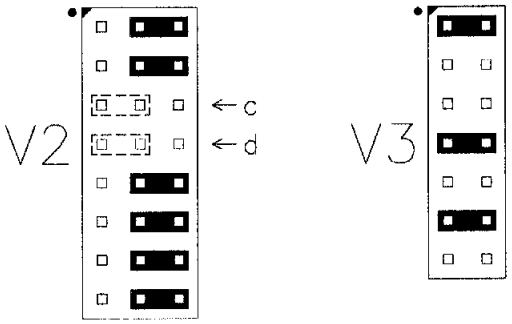
Figure 4-12. 20-bit / 8K Chip Memory Maps

20-Bit Address With 32K Chips

To use 32K chips with 20-bit addressing set jumper blocks V2 and V3 as shown below.

Jumpers V2c-d should be set for the desired board address as shown in Figure 4-13. Figure 4-14 details the resulting address of each memory socket in the selected memory map.

This jumper configuration ignores the state of the MEMEX signal in addressing the board. For systems that will use MEMEX, refer to the MEMEX Options section.



V2c	V2d	Map#	Address Range
X	X	0	00000-3FFFF
X	-	1	40000-7FFFF
-	X	2	80000-BFFFF
-	-	3	C0000-FFFFF

X = Install jumper in location shown
- = Remove jumper

Figure 4-13. 20-bit / 32K Chip Addressing

Map#	Memory Socket 0	1	2	3	4	5	6	7
0	00000-07FFF	08000-0FFFF	10000-17FFF	18000-1FFFF	20000-27FFF	28000-2FFFF	30000-37FFF	38000-3FFFF
1	40000-47FFF	48000-4FFFF	50000-57FFF	58000-5FFFF	60000-67FFF	68000-6FFFF	70000-77FFF	78000-7FFFF
2	80000-87FFF	88000-8FFFF	90000-97FFF	98000-9FFFF	A0000-A7FFF	A8000-AFFFF	B0000-B7FFF	B8000-BFFFF
3	C0000-C7FFF	C8000-CFFFF	D0000-D7FFF	D8000-DFFFF	E0000-E7FFF	E8000-EFFFF	F0000-F7FFF	F8000-FFFFF

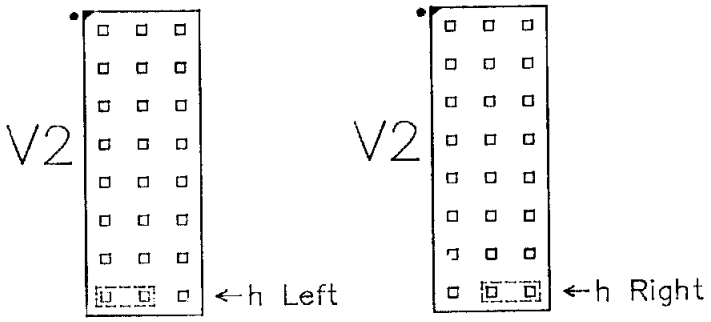
Figure 4-14. 20-bit / 32K Chips Memory Maps

MEMEX OPTIONS

The MEMEX (memory expansion) signal on the STD Bus is normally used to select between two different memory banks or maps. It can be used to expand the available memory (similar to selecting between two banks), or to control a bootstrap PROM. The MEMEX signal is usually controlled by (or jumpered to ground on) the system CPU card.

MEMEX is usually low (default) to select the standard or normal memory map. MEMEX high typically selects a secondary or alternate memory map. Devices that ignore the state of MEMEX will appear in both memory maps.

As shipped the MEMEX jumper (V2h) is set to ignore the MEMEX signal. The VL-7709 board will be addressed whether MEMEX is high or low. It can be jumpered for two other modes as shown in Figure 4-15.



Jumper	Setting	Description
V2h	Left -	Select on MEMEX high.
	Right -	Ignore MEMEX (select on high or low).
	None -	Select on MEMEX low.

Figure 4-15. MEMEX Options

MEMORY SOCKET CONFIGURATION

Once a memory map has been selected, the sockets must be configured for the type of device that will be used in each socket. The sockets are configured in pairs using jumper blocks A-D which are located next to the sockets they control. These jumper blocks also include chip enables and chip power options (discussed below).

Refer to Figure 4-17 for selection of the appropriate jumpers for each memory device type. Note that each pair of sockets is configured together and must use identical chips. RAM and ROM chips can be mixed on the board as long as they are put in different socket pairs. 8K and 32K chips can not be mixed on the board. All sockets should be jumpered for the same size chip.

Jumper Block	Controlled Sockets
A	M0, M1
B	M2, M3
C	M4, M5
D	M6, M7

Figure 4-16. Memory Socket Jumper Blocks

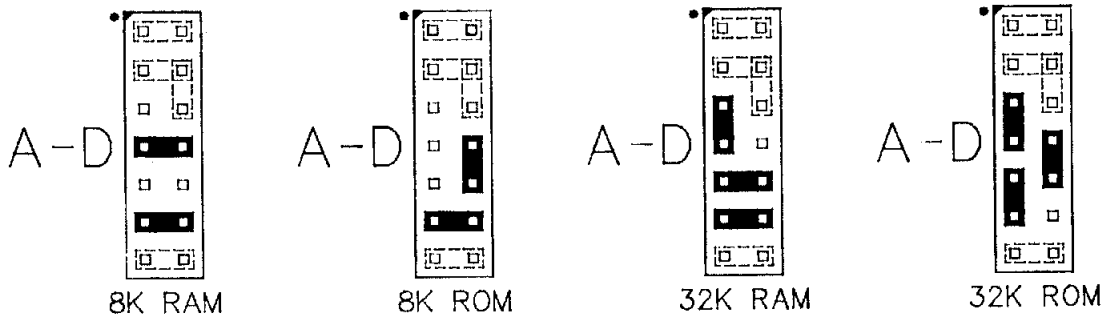


Figure 4-17. Chip Type Jumper Configurations

Chip Power Selection

Jumpers A-D also control the type of power (normal or backup) used for each socket pair. This jumper applies primarily to type "B" boards that include the on-board battery backup option. Boards without the battery backup option must have the power selection jumpers installed, but they may be in either the normal or backup positions.

The sockets may be jumpered for normal power (from the STD Bus system power supply), or backup power (system power with automatic backup from the on-board battery).

Chips which would be an unnecessary power drain on the on-board battery, such as ROMs, or RAMs that do not need to retain data at power-down, should be jumpered for normal power. RAMs that need to retain data at all times should be jumpered for battery backup.

As shipped all sockets are jumpered for backup power. The two power selection options are shown in Figure 4-18.

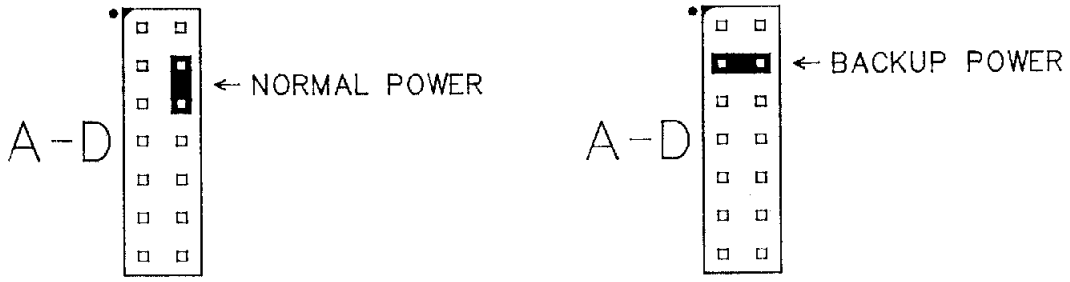


Figure 4-18. Power Selection Jumper

Disabling Unused Sockets

Any unused socket(s) on the board may be disabled, freeing its space in the memory map for memory elsewhere in the system.

Each memory socket is enabled with a jumper at the extreme end of jumper blocks A-D. Each socket is enabled when this jumper is in; it is disabled if the jumper is removed. Figure 4-19 shows the enable jumpers for each socket.

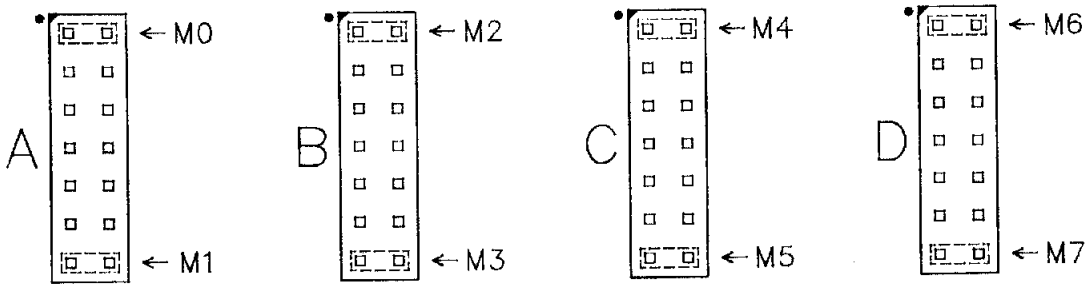


Figure 4-19. Memory Socket Enable Jumpers

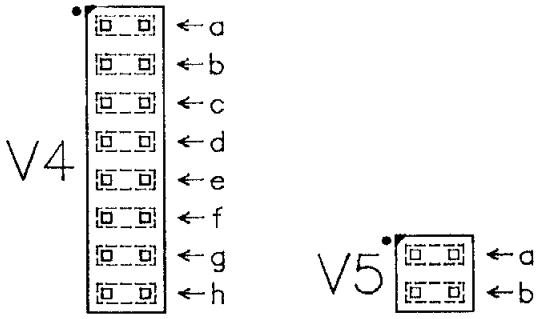
BANK CONTROL PORT ADDRESS

When used in the 16-bit addressing mode, the VL-7709 board provides a Bank Control port to allow selection of multiple memory banks. Banks of memory are selected (enabled) by writing the desired bank number to the Bank Control port. Normally located at I/O address EE, jumper block V4 allows the address of the Bank Control port to be altered for special applications.

Figure 4-20 details the jumper configurations for all of the available I/O addresses (00-FF). Figure 4-21 lists the options for the I/O expansion signal (IOEXP) for the Bank Control port.

Note that for proper operation, the Bank Control port address must be the same for all memory boards in the system.

The Bank Control port is initialized to bank zero when power is applied to the system. This will change only if data is written to the Bank Control port (address EE as shipped). If the Bank Control will not be used it can either be ignored (assuming that nothing in the system will ever write to port EE), or it can be disabled completely by removing all jumpers from V6. If the Bank Control port is disabled, jumper blocks V4 and V5 are ignored and may be left jumpered in any configuration desired.



V4 a	V4 b	V4 c	V4 d	Upper Hex Digit	V4 e	V4 f	V4 g	V4 h	Lower Hex Digit
X	X	X	X	0	X	X	X	X	0
X	X	X	-	1	X	X	X	-	1
X	X	-	X	2	X	X	-	X	2
X	X	-	-	3	X	X	-	-	3
X	-	X	X	4	X	-	X	X	4
X	-	X	-	5	X	-	X	-	5
X	-	-	X	6	X	-	-	X	6
X	-	-	-	7	X	-	-	-	7
-	X	X	X	8	-	X	X	X	8
-	X	X	-	9	-	X	X	-	9
-	X	-	X	A	-	X	-	X	A
-	X	-	-	B	-	X	-	-	B
-	-	X	X	C	-	-	X	X	C
-	-	X	-	D	-	-	X	-	D
-	-	-	X	E	-	-	-	X	E
-	-	-	-	F	-	-	-	-	F

X = Installed jumper

Figure 4-20. Bank Control Port Address

V5 a	V5 b	Description
X	-	Enable when IOEXP high
-	X	Enable when IOEXP low
-	-	Ignore IOEXP

Figure 4-21. Bank Control Port, IOEXP Jumper

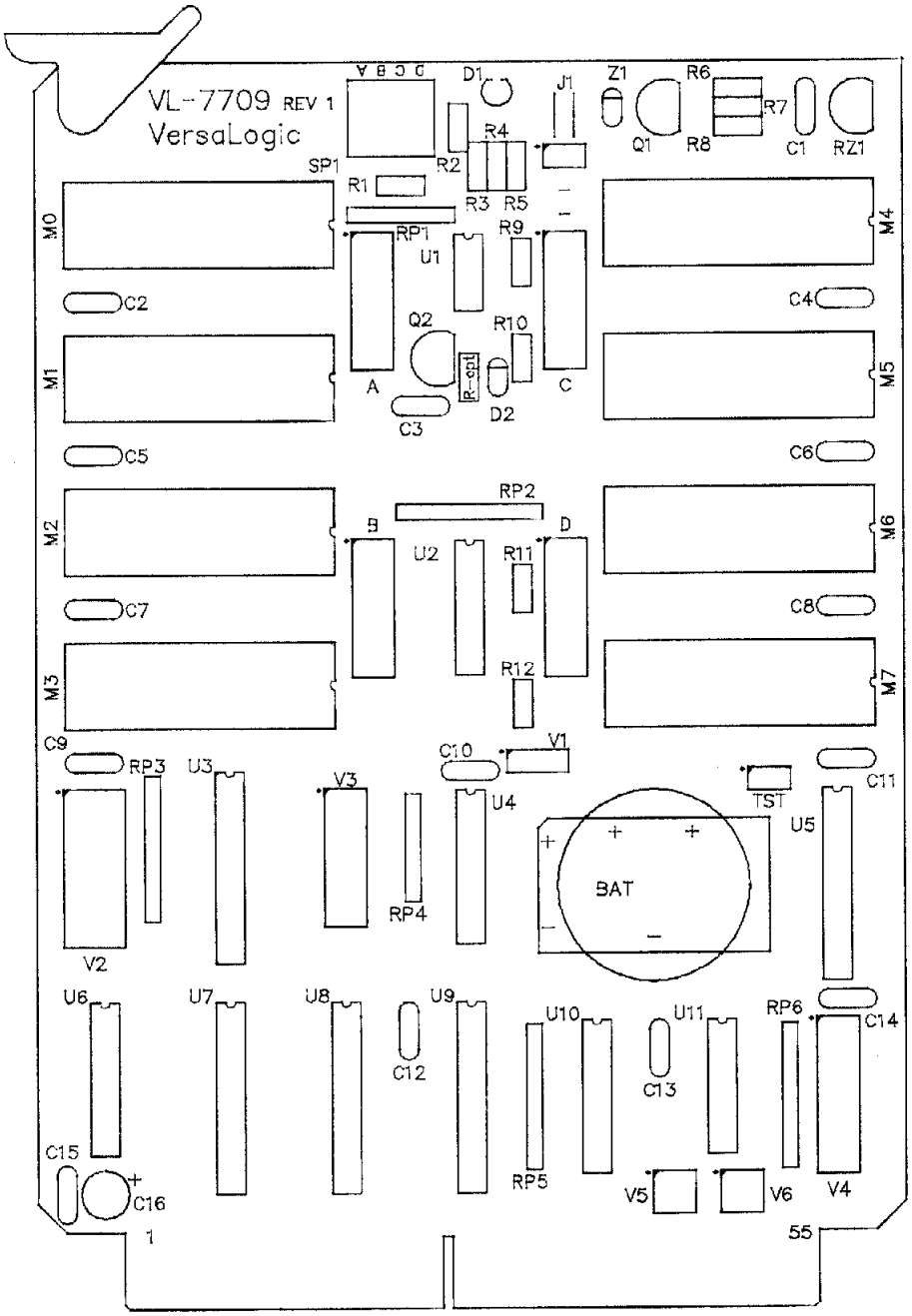
BATTERY BACKUP SOURCE

Normally the backup power for on-board devices is taken from the on-board lithium battery. For this mode of operation jumper V1 should be installed in position b. For special applications with an external backup battery, backup power can be taken from STD Bus pin 5 by moving the V1 jumper to position a.

The V1 jumper is also useful for disconnecting the battery during installation or removal of memory chips. This practice is recommended for the safety of the chips. Removing the jumper from V1 will temporarily disconnect the backup battery from all on-board devices.

Figure 4-22. Battery Backup Source Jumper

VL-7709 REV 1 Parts Placement Diagram 2/86



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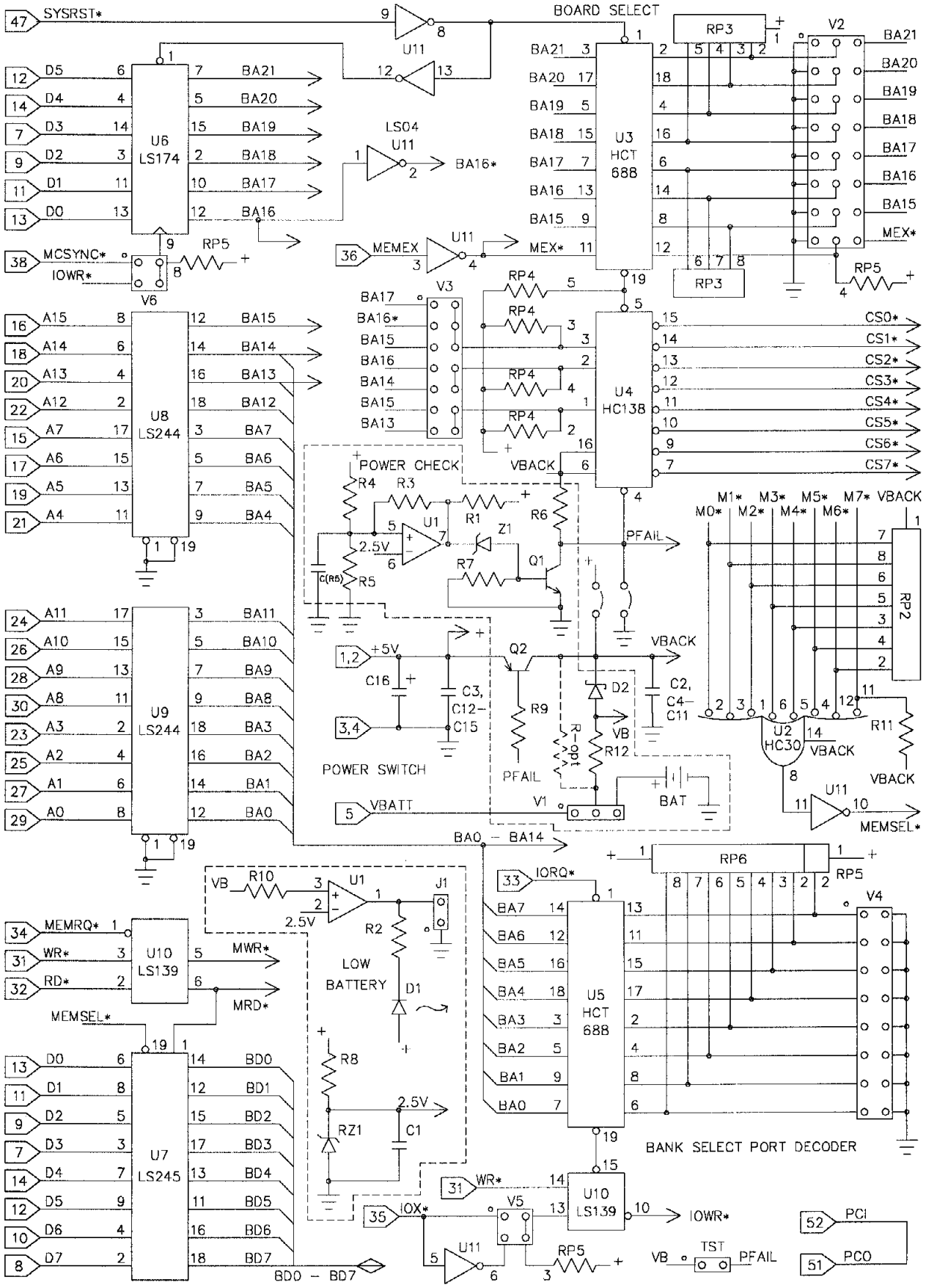
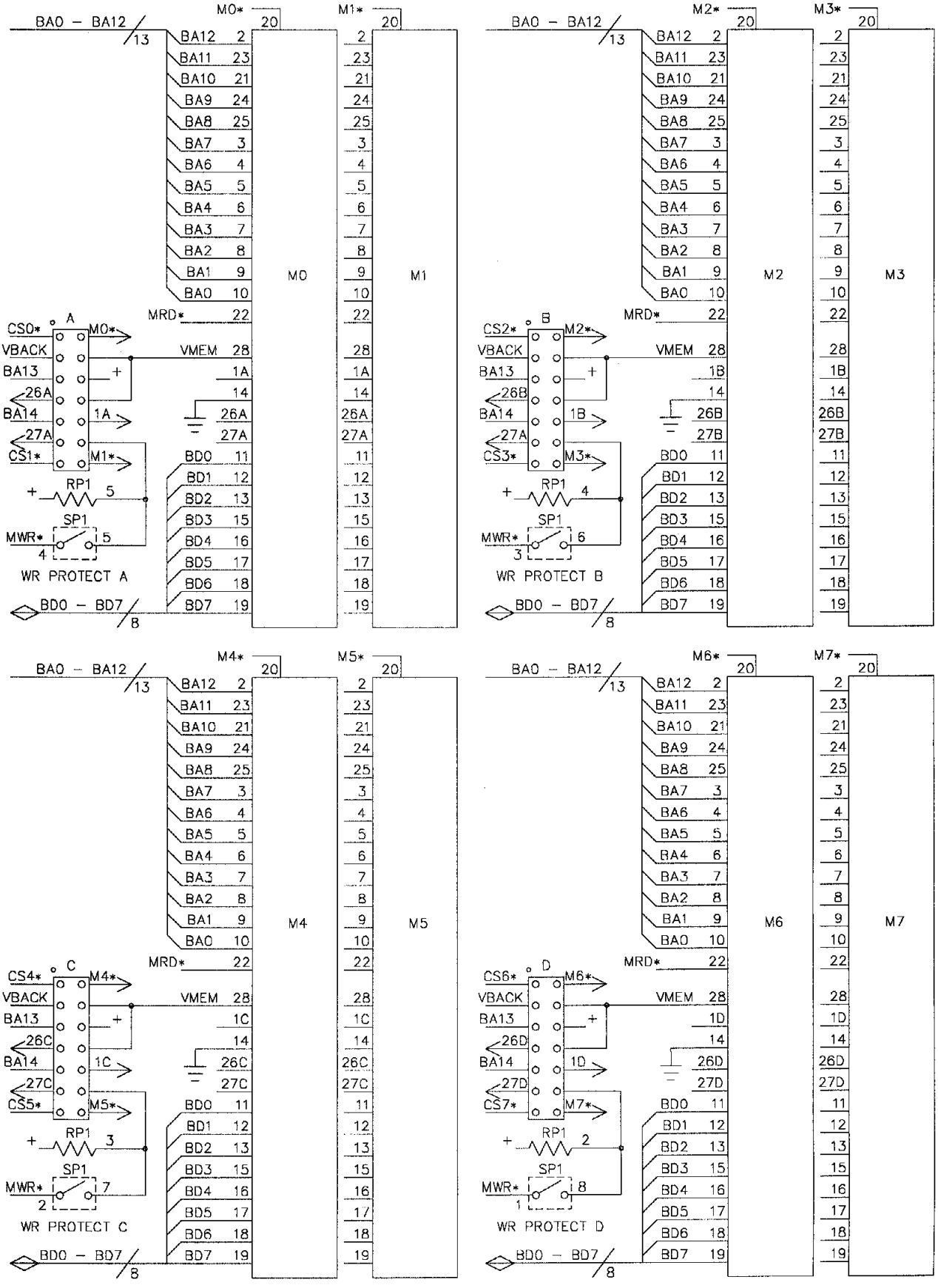


VL-7709 REV 1.01



VL-7709 PARTS LIST
64/256K Memory board (without battery backup).

Capacitors

C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15	.01 uf ceramic disk
C16	22 uf 25V elect. radial

Integrated Circuits

U2	74HC30
U3, U5	74HCT688
U4	74HC138
U6	74LS174
U7	74LS245
U8, U9	74LS244
U10	74LS139
U11	74LS04

Resistors

R11	10K ohm, 5%, 1/4W
RP1, RP4	10K ohm, 5 resistor SIP
RP2, RP3, RP5, RP6	10K ohm, 7 resistor SIP

Miscellaneous

SP1	4 pos. R/A switch

VL-7709B PARTS LIST
64/256K Memory board with on-board battery backup.

Capacitors

C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15	.01 uf ceramic disk
C(R5)	270 pf ceramic disk
C16	22 uf 25V elect. radial

Integrated Circuits

U1	LM2903N
U2	74HC30
U3, U5	74HCT688
U4	74HC138
U6	74LS174
U7	74LS245
U8, U9	74LS244
U10	74LS139
U11	74LS04

Resistors

R1, R9	4K7 ohm, 5%, 1/4W
R2	820 ohm, 5%, 1/4W
R3, R10	374K ohm, 1%, 1/4W
R4, R7	10K ohm, 1%, 1/4W
R5	12.1K ohm, 1%, 1/4W
R6, R8	2K2 ohm, 5%, 1/4W
R11	10K ohm, 5%, 1/4W
R12	470 ohm, 5%, 1/4W
RP1, RP4	10K ohm, 5 resistor SIP
RP2, RP3, RP5, RP6	10K ohm, 7 resistor SIP

Semiconductors

D1	LED MV5077C
D2	1N5817
Q1	PN2222A
Q2	PN2907
RZ1	LM336BZ 2.5V zener
Z1	1N746 3.3V zener

Miscellaneous

J1	2 pin R/A header
BAT	Lithium battery, 3.5V 750 mah
SPI	4 pos. R/A switch

VL-77CT09 PARTS LIST

64/256K Extended Temperature Memory board (without battery backup).

Capacitors

C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15	.01 uf ceramic disk
C16	22 uf 25V elect. radial

Integrated Circuits

U2	74HCT30
U3, U5	74HCT688
U4	74HCT138
U6	74HCT174
U7	74ACT245
U8, U9	74ACT244
U10	74HCT139
U11	74HCT04

Resistors

R11	100K ohm, 5%, 1/4W
RP1, RP4	100K ohm, 5 resistor SIP
RP2, RP3, RP5, RP6	100K ohm, 7 resistor SIP

Miscellaneous

SP1	4 pos. R/A switch

VL-77CT09B PARTS LIST

64/256K Extended Temperature Memory board with on-board battery backup.

Capacitors

C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15	.01 uf ceramic disk
C(R5)	270 pf ceramic disk
C16	22 uf 25V elect. radial

Integrated Circuits

U1	LM2903N
U2	74HCT30
U3, U5	74HCT688
U4	74HCT138
U6	74HCT174
U7	74ACT245
U8, U9	74ACT244
U10	74HCT139
U11	74HCT04

Resistors

R1, R9	4K7 ohm, 5%, 1/4W
R2	820 ohm, 5%, 1/4W
R3, R10	374K ohm, 1%, 1/4W
R4, R7	10K ohm, 1%, 1/4W
R5	12.1K ohm, 1%, 1/4W
R6, R8	2K2 ohm, 5%, 1/4W
R11	100K ohm, 5%, 1/4W
R12	470 ohm, 5%, 1/4W
RP1, RP4	100K ohm, 5 resistor SIP
RP2, RP3, RP5, RP6	100K ohm, 7 resistor SIP

Semiconductors

D1	LED MV5077C
D2	1N5817
Q1	PN2222A
Q2	PN2907
RZ1	LM236H-2.5 zener
Z1	1N746 3.3V zener

Miscellaneous

J1	2 pin R/A header
BAT	Lithium battery, 3.5V 750 mah
SPI	4 pos. R/A switch

STD BUS PINOUT

Connections from the VL-7709 board to the STD BUS are shown below. Pins 1 and 2 are at the top (card ejector) edge of the board. As noted below the odd numbered pins are on the component side of the board while the even numbered pins are on the solder side. Direction of signal flow is referenced to the VL-7709.

COMPONENT SIDE				SOLDER SIDE			
PIN	SIGNAL	FLOW	DESCRIPTION	PIN	SIGNAL	FLOW	DESCRIPTION
1	+5V	In	+5 volt power	2	+5V	In	+5 volt power
3	GND	In	Digital ground	4	GND	In	Digital ground
5	VBB/VBAT	(1)	-5V or bat. backup	6	-5V	-	-5V power
7	D3/A19	In	Data bus	8	D7	In	Data bus
9	D2/A18	In	Data bus	10	D6	In	Data bus
11	D1/A17	In	Data bus	12	D5/A21	In	Data bus
13	DO/A16	In	Data bus	14	D4/A20	In	Data bus
15	A7	In	Address bus	16	A15	In	Address bus
17	A6	In	Address bus	18	A14	In	Address bus
19	A5	In	Address bus	20	A13	In	Address bus
21	A4	In	Address bus	22	A12	In	Address bus
23	A3	In	Address bus	24	A11	In	Address bus
25	A2	In	Address bus	26	A10	In	Address bus
27	A1	In	Address bus	28	A9	In	Address bus
29	AO	In	Address bus	30	A8	In	Address bus
31	WR*	In	Write strobe	32	RD*	In	Read strobe
33	IORQ*	In	I/O addr. select	34	MEMRQ*	In	Memory addr. select
35	IOEXP*	In	I/O expansion	36	MEMEX*	In	Memory expansion
37	REFRESH*	-	Refresh timing	38	MCSYNC*	In	Machine cycle sync.
39	STATUS1*	-	CPU status	40	STATUSO*	-	CPU status
41	BUSAK*	-	Bus acknowledge	42	BUSRQ*	-	Bus request
43	INTAK*	-	Interrupt acknowl.	44	INTRQ*	-	Interrupt request
45	WAITRQ*	-	Wait request	46	NMIRQ*	-	Non-maskable interrupt
47	SYSRESET*	In	System reset	48	PBRESET*	-	Push button reset
49	CLOCK*	-	CPU clock	50	CNTRL*	-	AUX timing
51	PCO	Out	Priority chain out	52	PCI	In	Priority chain in
53	AUXGND	-	±12 volt ground	54	AUXGND	-	±12 volt ground
55	AUX+V	-	+12 volt input	56	AUX-V	-	-12 volt input

Notes:
1) Jumper option. Normally not connected.

DECIMAL / HEX / ASCII CONVERSION CHART

The chart below is useful for both ASCII and decimal/hex conversion. The "^" symbol denotes control characters. "^A" represents control A, etc.

Dec.	Hex	ASCII	Dec.	Hex	ASCII	Dec.	Hex	ASCII	Dec.	Hex	ASCII
0	00	NUL	32	20		64	40	@	96	60	`
1	01	^A SOH	33	21	!	65	41	A	97	61	a
2	02	^B STX	34	22	"	66	42	B	98	62	b
3	03	^C ETX	35	23	#	67	43	C	99	63	c
4	04	^D EOT	36	24	$	68	44	D	100	64	d
5	05	^E ENQ	37	25	%	69	45	E	101	65	e
6	06	^F ACK	38	26	&	70	46	F	102	66	f
7	07	^G BEL	39	27	'	71	47	G	103	67	g
8	08	^H BS	40	28	(	72	48	H	104	68	h
9	09	^I HT	41	29	)	73	49	I	105	69	i
10	0A	^J LF	42	2A	*	74	4A	J	106	6A	j
11	0B	^K VT	43	2B	+	75	4B	K	107	6B	k
12	0C	^L FF	44	2C	,	76	4C	L	108	6C	l
13	0D	^M CR	45	2D	-	77	4D	M	109	6D	m
14	0E	^N SO	46	2E	.	78	4E	N	110	6E	n
15	0F	^O SI	47	2F	/	79	4F	O	111	6F	o
16	10	^P DLE	48	30	0	80	50	P	112	70	p
17	11	^Q DC1	49	31	1	81	51	Q	113	71	q
18	12	^R DC2	50	32	2	82	52	R	114	72	r
19	13	^S DC3	51	33	3	83	53	S	115	73	s
20	14	^T DC4	52	34	4	84	54	T	116	74	t
21	15	^U NAK	53	35	5	85	55	U	117	75	u
22	16	^V SYN	54	36	6	86	56	V	118	76	v
23	17	^W ETB	55	37	7	87	57	W	119	77	w
24	18	^X CAN	56	38	8	88	58	X	120	78	x
25	19	^Y EM	57	39	9	89	59	Y	121	79	y
26	1A	^Z SUB	58	3A	:	90	5A	Z	122	7A	z
27	1B	ESC	59	3B	;	91	5B	[	123	7B	{
28	1C	FS	60	3C	<	92	5C	\	124	7C	|
29	1D	GS	61	3D	=	93	5D	]	125	7D	}
30	1E	RS	62	3E	>	94	5E	^	126	7E	~
31	1F	US	63	3F	?	95	5F	_	127	7F	DEL