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IPD06N03LA

OptiMOS[®] 2 Power-Transistor

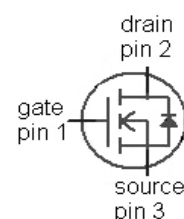
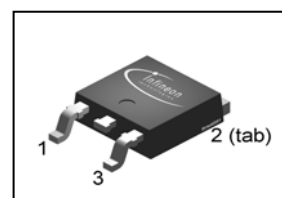
Features

- Ideal for high-frequency dc/dc converters
- N-channel
- Logic level
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance
- 175 °C operating temperature
- dv/dt rated

Product Summary

V_{DS}	25	V
$R_{DS(on),max}$	5.7	mΩ
I_D	50	A

P-TO252-3-11



Type	Package	Ordering Code	Marking
IPD06N03LA	P-TO252-3-11	Q67042-S4149	06N03LA

Maximum ratings, at $T_J=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_C=25\text{ °C}^{(1)}$	50	A
		$T_C=100\text{ °C}$	50	
		$T_C=25\text{ °C}^{(2)}$	350	
Pulsed drain current	$I_{D,pulse}$	$T_C=25\text{ °C}^{(2)}$	350	
Avalanche energy, single pulse	E_{AS}	$I_D=50\text{ A}$, $R_{GS}=25\text{ Ω}$	225	mJ
Reverse diode dv/dt	dv/dt	$I_D=50\text{ A}$, $V_{DS}=20\text{ V}$, $di/dt=200\text{ A/μs}$, $T_{j,max}=175\text{ °C}$	6	kV/μs
Gate source voltage ⁽³⁾	V_{GS}		±20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	83	W
Operating and storage temperature	T_j , T_{stg}		-55 ... 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	



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Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - case	R_{thJC}		-	-	1,8	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	75	
		6 cm ² cooling area ⁴⁾	-	-	50	

Electrical characteristics, at $T_j=25\text{ }^{\circ}\text{C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$	25	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=40\text{ }\mu\text{A}$	1,2	1,6	2	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=25\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ }^{\circ}\text{C}$	-	0,1	1	μA
		$V_{DS}=25\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ }^{\circ}\text{C}$	-	10	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	10	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5\text{ V}, I_D=30\text{ A}$	-	7,5	8,4	m Ω
		$V_{GS}=10\text{ V}, I_D=30\text{ A}$	-	4,8	5,7	
Gate resistance	R_G		-	1	-	Ω
Transconductance	g_{fs}	$ V_{DS} >2 I_D R_{DS(on)max}, I_D=30\text{ A}$	27	54	-	S

¹⁾ Current is limited by bondwire; with an $R_{thJC}=1.8\text{ K/W}$ the chip is able to carry 94 A.

²⁾ See figure 3

³⁾ $T_{j,max}=150\text{ }^{\circ}\text{C}$ and duty cycle $D<0.25$ for $V_{GS}<-5\text{ V}$

⁴⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.



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Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=15\text{ V}, f=1\text{ MHz}$	-	1995	2653	pF
Output capacitance	C_{oss}		-	848	1128	
Reverse transfer capacitance	C_{rss}		-	124	186	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=15\text{ V}, V_{GS}=10\text{ V}, I_D=25\text{ A}, R_G=2.7\ \Omega$	-	11	17	ns
Rise time	t_r		-	17	26	
Turn-off delay time	$t_{d(off)}$		-	30	45	
Fall time	t_f		-	7	11	

Gate Charge Characteristics⁵⁾

Gate to source charge	Q_{gs}	$V_{DD}=15\text{ V}, I_D=25\text{ A}, V_{GS}=0\text{ to }5\text{ V}$	-	7	9	nC
Gate charge at threshold	$Q_{g(th)}$		-	3,2	4,2	
Gate to drain charge	Q_{gd}		-	4,8	7,1	
Switching charge	Q_{sw}		-	8	12	
Gate charge total	Q_g		-	16	22	
Gate plateau voltage	$V_{plateau}$		-	3,3	-	V
Gate charge total, sync. FET	$Q_{g(sync)}$	$V_{DS}=0.1\text{ V}, V_{GS}=0\text{ to }5\text{ V}$	-	14	19	nC
Output charge	Q_{oss}	$V_{DD}=15\text{ V}, V_{GS}=0\text{ V}$	-	18	24	

Reverse Diode

Diode continuous forward current	I_S	$T_C=25\text{ °C}$	-	-	50	A
Diode pulse current	$I_{S,pulse}$		-	-	350	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=50\text{ A}, T_J=25\text{ °C}$	-	0,92	1,2	V
Reverse recovery charge	Q_{rr}	$V_R=15\text{ V}, I_F=I_S, di_F/dt=400\text{ A}/\mu\text{s}$	-	-	10	nC

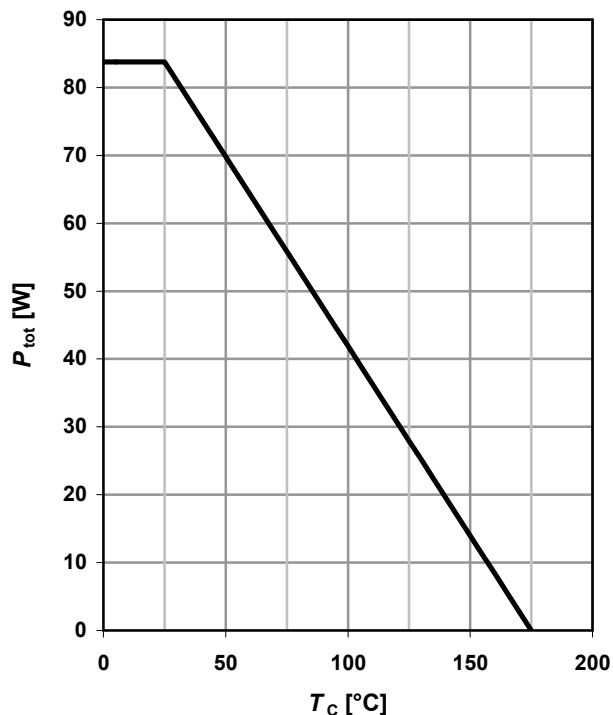
⁵⁾ See figure 16 for gate charge parameter definition



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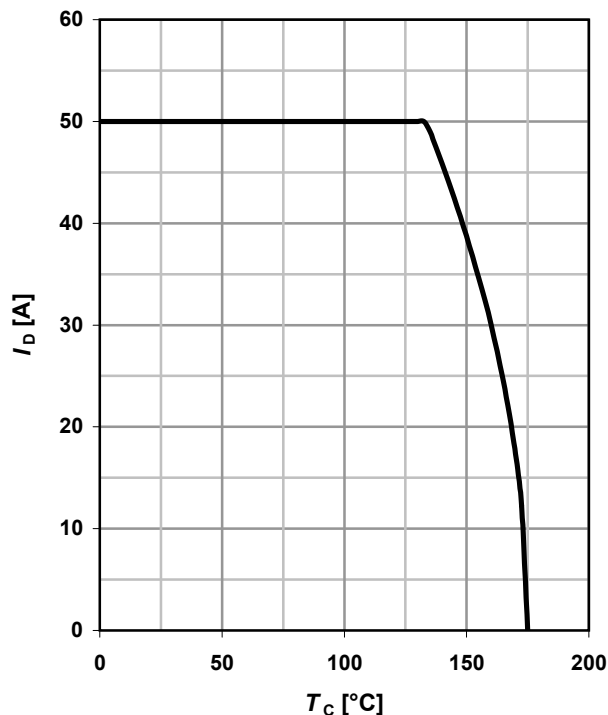
1 Power dissipation

$$P_{\text{tot}} = f(T_C)$$



2 Drain current

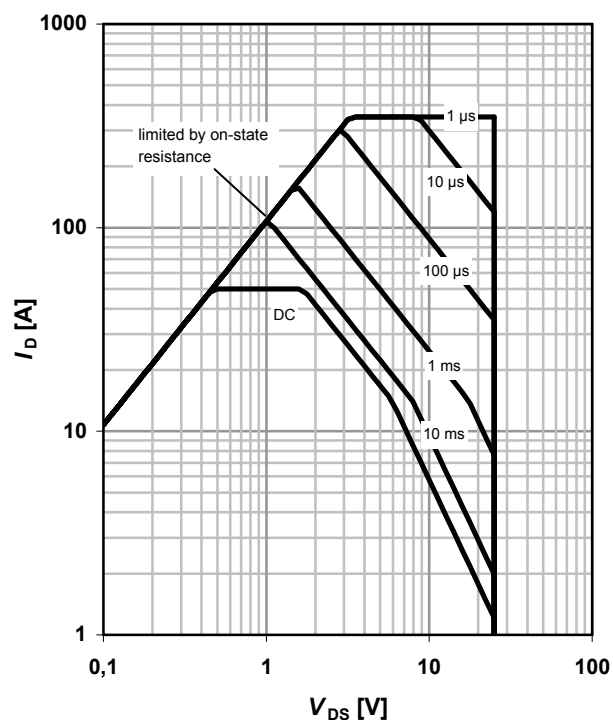
$$I_D = f(T_C); V_{GS} \geq 10 \text{ V}$$



3 Safe operation area

$$I_D = f(V_{DS}); T_C = 25^\circ\text{C}; D = 0$$

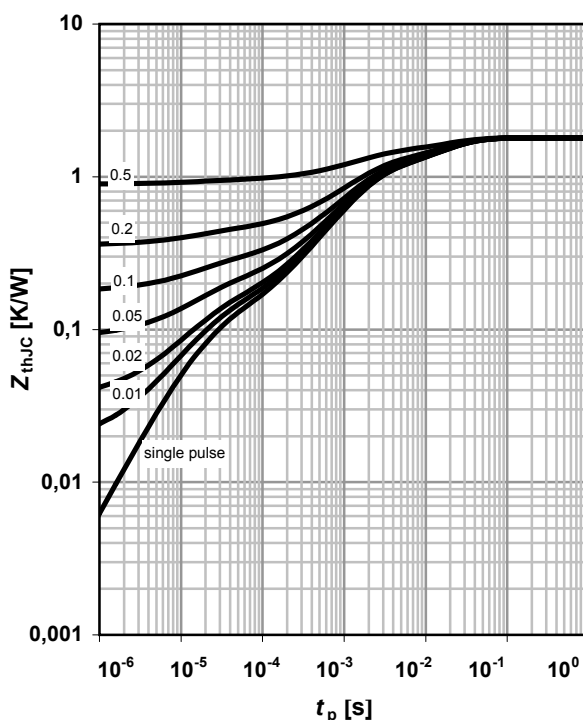
parameter: t_p



4 Max. transient thermal impedance

$$Z_{\text{thJC}} = f(t_p)$$

parameter: $D = t_p/T$



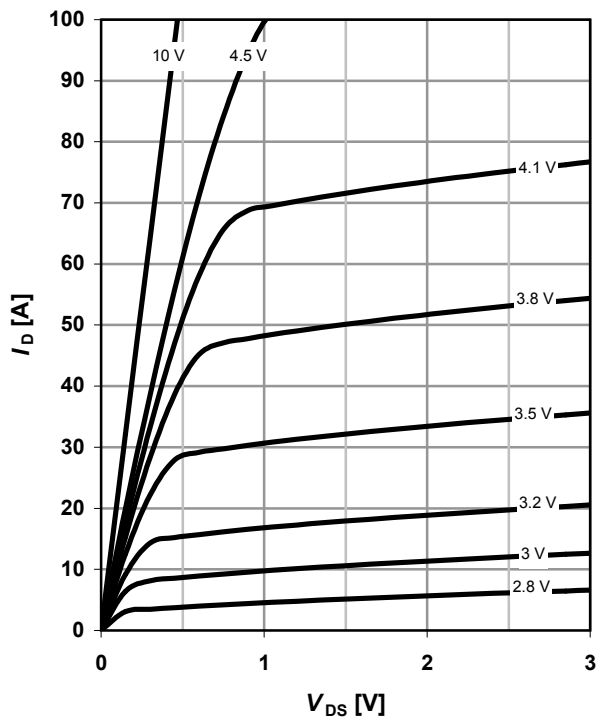


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5 Typ. output characteristics

$$I_D = f(V_{DS}); T_j = 25^\circ\text{C}$$

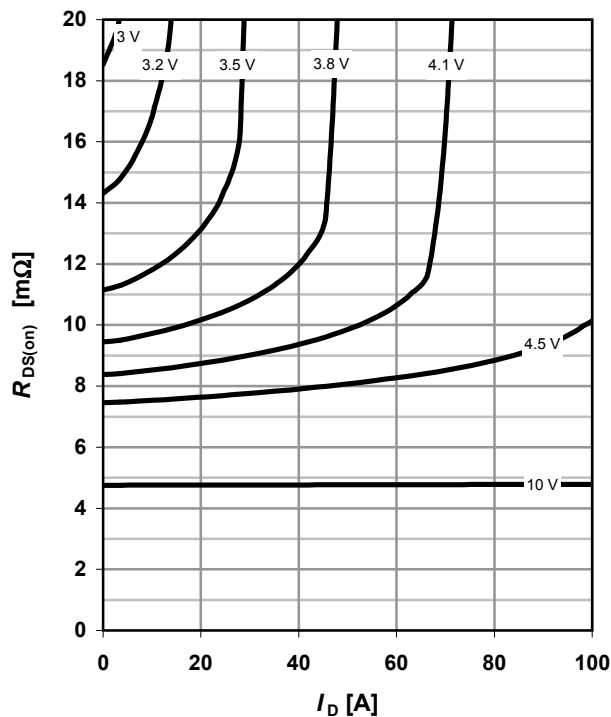
parameter: V_{GS}



6 Typ. drain-source on resistance

$$R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$$

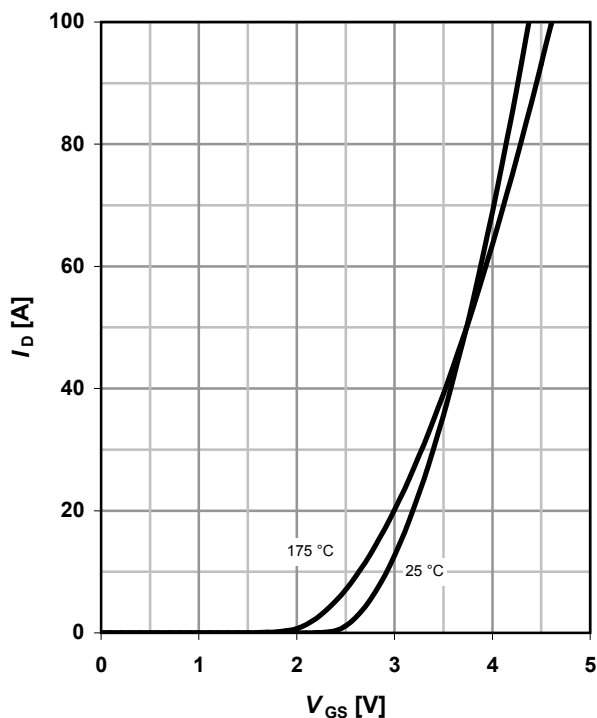
parameter: V_{GS}



7 Typ. transfer characteristics

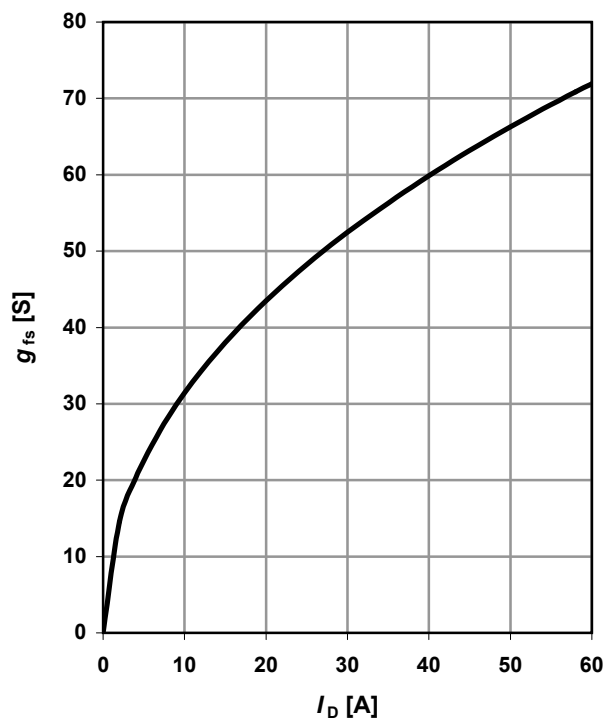
$$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$$

parameter: T_j



8 Typ. forward transconductance

$$g_{fs} = f(I_D); T_j = 25^\circ\text{C}$$

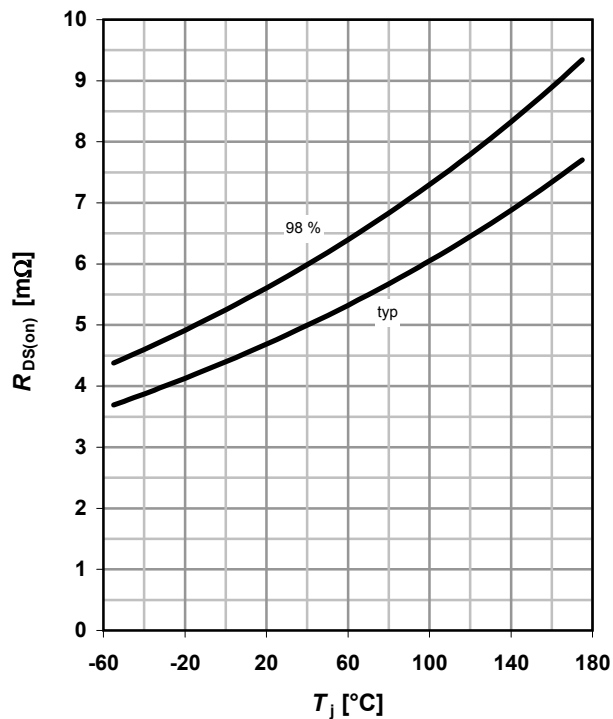




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9 Drain-source on-state resistance

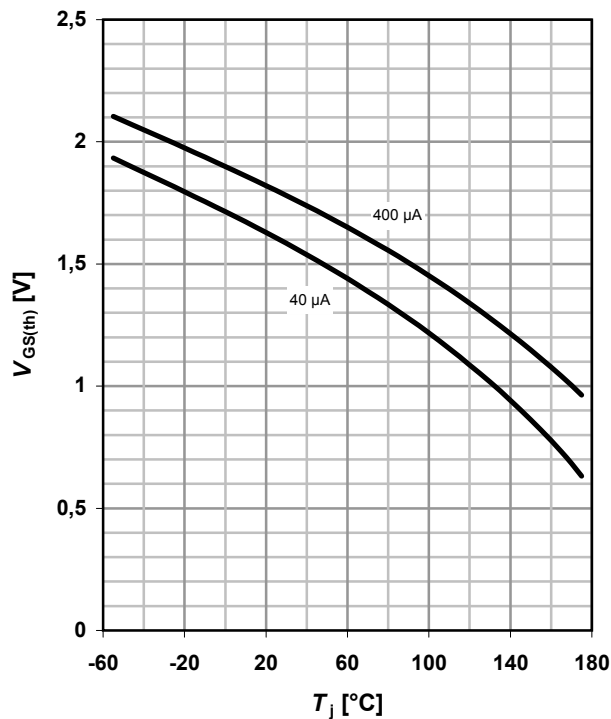
$$R_{DS(on)} = f(T_j); I_D = 30 \text{ A}; V_{GS} = 10 \text{ V}$$



10 Typ. gate threshold voltage

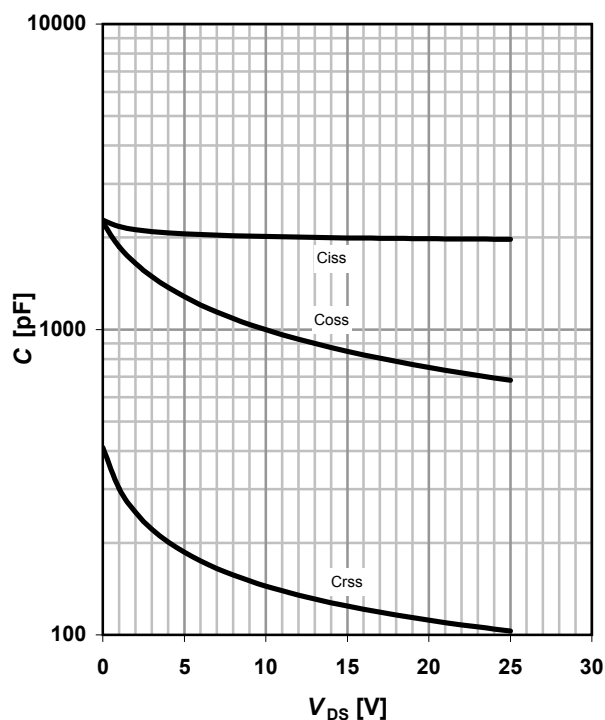
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: I_D



11 Typ. Capacitances

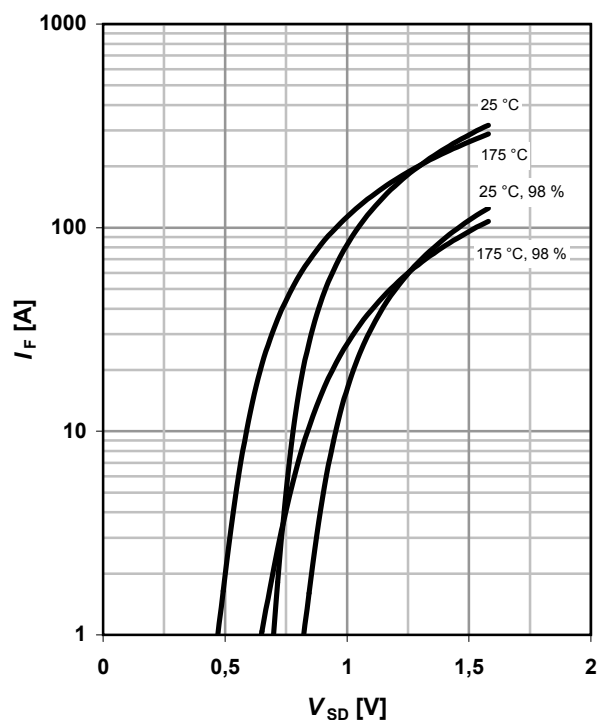
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$



12 Forward characteristics of reverse diode

$$I_F = f(V_{SD})$$

parameter: T_j



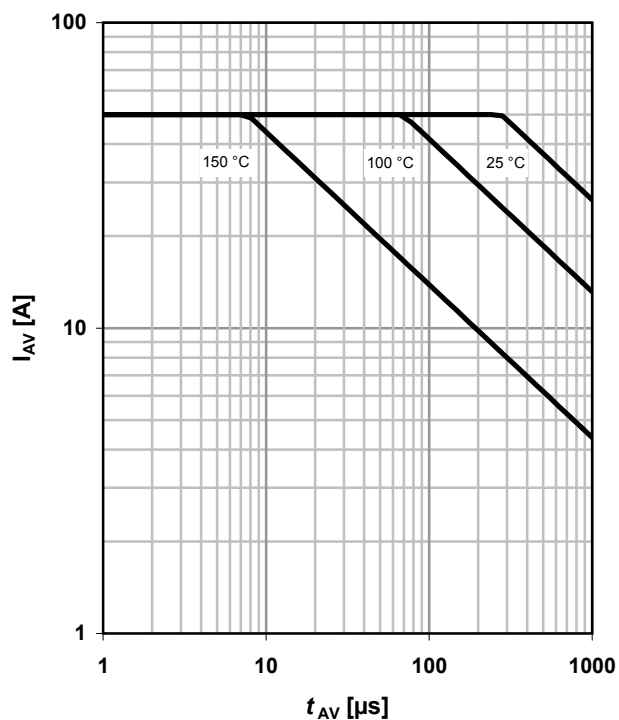


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13 Avalanche characteristics

$$I_{AS}=f(t_{AV}); R_{GS}=25\ \Omega$$

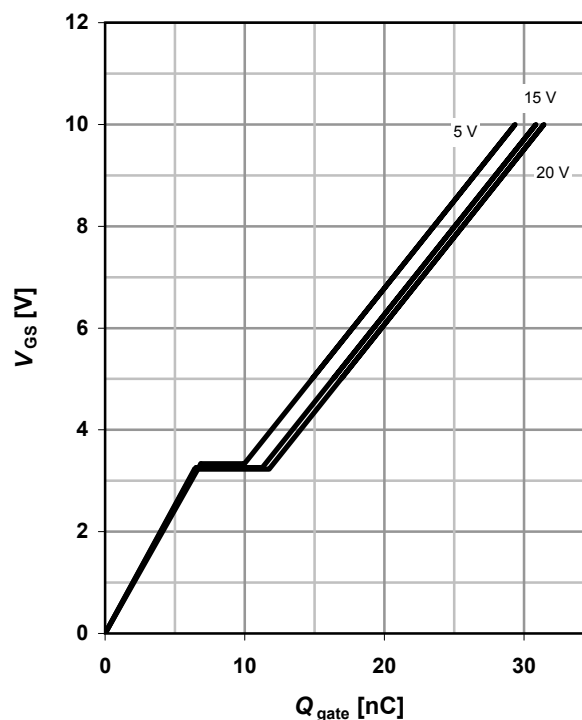
parameter: $T_{j(\text{start})}$



14 Typ. gate charge

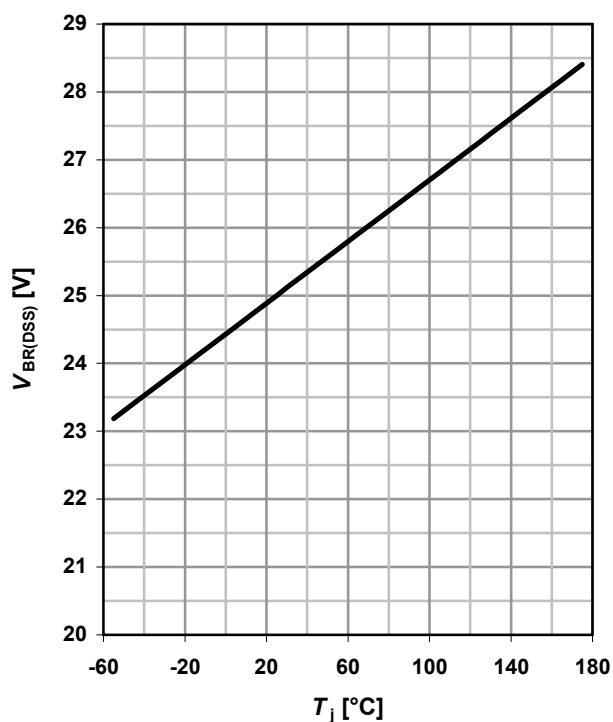
$$V_{GS}=f(Q_{\text{gate}}); I_D=25\ \text{A pulsed}$$

parameter: V_{DD}

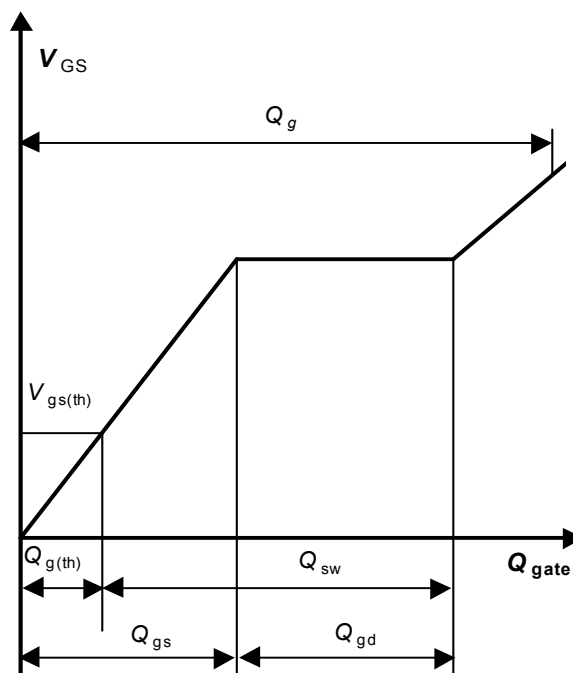


15 Drain-source breakdown voltage

$$V_{BR(DSS)}=f(T_j); I_D=1\ \text{mA}$$



16 Gate charge waveforms

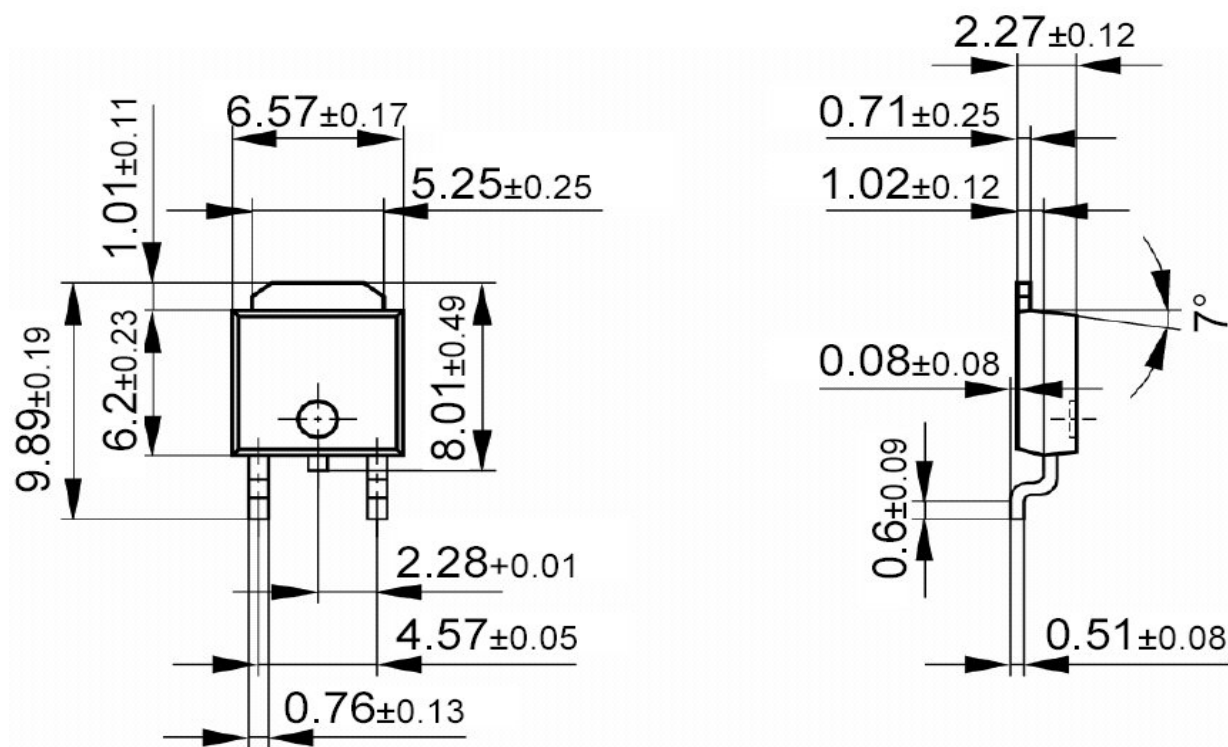




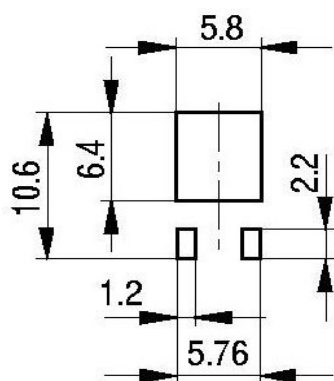
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Package Outline

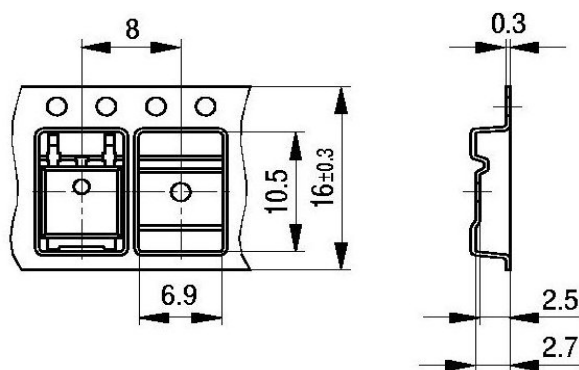
P-TO252-3-1: Outline



Footprint:



Packaging:





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