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STLVDS3486BDR

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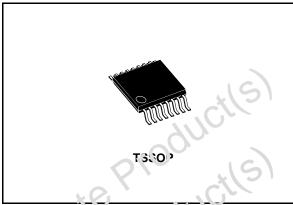
High speed differential line drivers

Feature summary

- meets or exceeds the requirements of ansi TIA/EIA-644 standard
- Operates with a single 3.3V supply
- Designed for signaling rate up to 400Mbps
- Differential input thresholds ±100mV max
- Typical propagation delay time of 2.5ns
- Power dissipation 60mW typical per receiver at 200MHz
- Low voltage TTL (LVTTL) logic output levels
- Pin compatible with the MC3486 and SN65LVD3486
- Open circuit fail safe
- ESD protection:7KV receiver pins3KV all pins vs gnd

Description

The STLVDS3486, is a differential line receiver that implements the electrical characteristics of low voltage differential signaling (LVC3). This signaling technique lowers the output voltage levels of 57 differential standard levels (such as TIA/EIA-122B) to reduce the power, increase the switching speeds and allow operations with a 2.37 supply rail. This differential receiver provides a valid logical of court state with a 3.37 supply rail.



It also provides a valid logical petput state with a ±100m% differential input voltage within the input coroner, mode voltage varige. The input common and a voltage allows 1V of ground potential difference between two LVDS nodes.

The intended application of this device and signaline technique is both point-to-point and reclard op data transmission over controlled impedance media approximately 100Ω . The transmission media may be printed circuit board traces, backplanes or cables. The ultimate rate and distance of data transfer depend upon the attenuation characteristics of the media and noise coupling to the environment.

The STLVDS3486 version is characterized for operation from -40°C to 85°C.

Order code

Part number	Temperature Range	Package	Comments
STLVDS3486BTR	-40 to 85 °C	TSSOP16 (Tape & Reel)	2500 parts per reel

April 2006 Rev. 4 1/15



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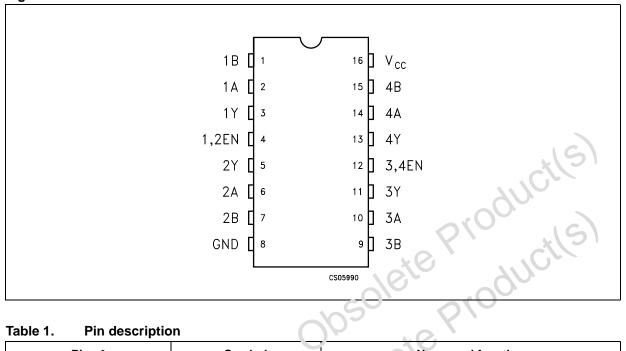




STLVDS3486 Pin configuration

Pin configuration 1

Figure 1. Pin connections



Pin description Table 1.

Pin n°	Symbol	Name and function	
2, 6, 10, 14	1/\ to 4A	Receiver inputs	
1, 7, 9, 15	12 to 4B	Negated receiver inputs	
3, 5, 11, 13	1Y to 4Y	Receiver outputs	
4	1EN, 2EN	Receivers 1 and 2 enable	
12	3EN, 4EN	Receivers 3 and 4 enable	
1030	GND	Ground	
16	V _{CC}	Supply voltage	

Table 2. Truth table

Differential input	Enables	Output
A, B	EN	Y
V _{ID} ≥ 100mV	Н	Н
-100mV < V _{ID} < 100mV	Н	?
V _{ID} ≤ -100mV	Н	L
X	L	Z
OPEN	Н	Н

L=Low level, H=High Level, X=Don't care, Z= High Impedance

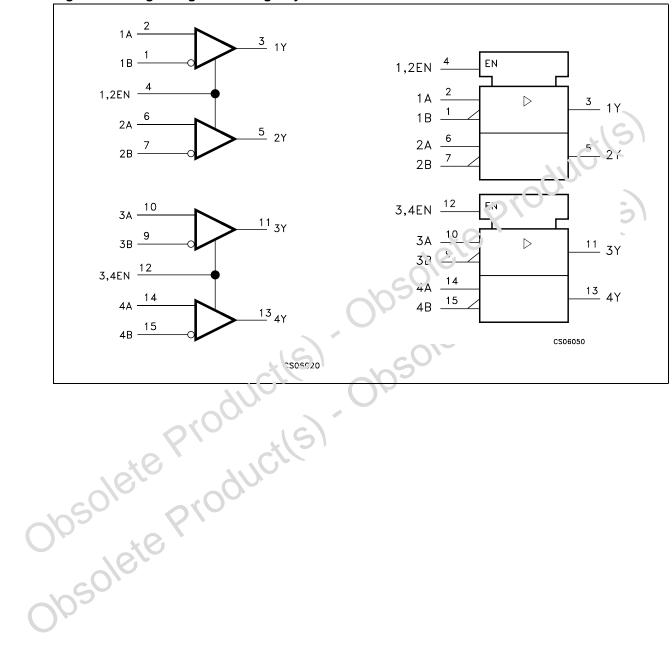




Logic diagram STLVDS3486

2 Logic diagram

Figure 2. Logic diagram and logic symbol





STLVDS3486 Maximum ratings

3 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit	
V _{CC}	Supply voltage (Note 1)	-0.5 to 4.6	V	
V _I	Input voltage	-0.5 to (V _{CC} + 0.5)	V	
V _I	Input voltage (A or B inputs)	-0.5 to 4.6	V	
ESD	Human hady model	Pins receivers	7	KV
E9D	Human body model All pins vs gnd		3	I IV
T _{stg}	Storage temperature range	-65 to +150	℃	

Note: Absolute Maximum Ratings are those values beyond which damage to the device may

occur. Functional operation under these condition is not implica-

Note: 1 All voltages except differential I/O bus voltage, are with respect to the network ground

terminal.

Table 4. Recommended operating conditions

	Symbol Parameter		Min.	Тур.	Max.	Unit
	V_{CC}	Supply voltage	3.0	3.3	3.6	V
	V _{IH}	HIGH Level input voltage (enable)	2.0			V
	V _{IL}	LOW Level input voltage (ยายhle)	0		0.8	V
	V _{ID}	Magnitude of diffe:e.atia Imput voltage	0.1		0.6	V
	1/	Common n.odo input voltage	0.5 V _{ID}		2.4-0.5 V _{ID}	V
	V _{IC}	Comment in Sice input voltage			V _{CC} - 0.8	
	T _J Overating temperature range				85	°C
0	osole osole	ate Produc				
Ö	pso.					





Electrical characteristics

STLVDS3486

4 Electrical characteristics

Table 5. Electrical characteristics

(Over recommended operating conditions unless otherwise noted. All typical values are at T_A = 25°C, and V_{CC} = 3.3V).

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Un
V _{ITH+}	Positive Going Differential Input Voltage Threshold				100	m\
V _{ITH} -	Negative Going Differential Input Voltage Threshold		-100			m'
V _{OH}	High Level Output Voltage	$I_{OH} = -8mA$ $I_{OH} = -4mA$	2.4 2.8		1/2	
V _{OL}	Low Level Output Voltage	I _{OH} = 8mA	2.0	ZD'	0.4	V
I _{CC}	Supply Current	Enabled, No Load	0 Y C	10	18	m.
		Disabled		0.25	0.5	m.
I	Input Current (A or B inputs)	$V_1 = 0V$	-2	-10	-20	μ
I _{I(OFF)}	Power off Input Current (A or B inputs)	$V_1 = 2.4V$ $V_{CC} = 0, V_1 = 3.6V$	-1.2	-3 10	20	μ
I _{IH}	High Level Input Current (EN, G, G or Inputs)	$V_{li} = 2V$			10	μ
I _{IL}	Low Level Input Current (EN, G, C or Inputs)	V _{IL} = 0.8V			10	μ
I _{OZ}	High Impedance Output Current	$V_O = 0$ or V_{CC}			± 10	μ
50	Low Level Input Current (EN, G, C or Inputs) High Impedance Output Current					





Electrical characteristics

Table 6. Switching characteristics

(Over recommended operating conditions unless otherwise noted. All typical values are at $T_A = 25$ °C, and $V_{CC} = 3.3$ V).

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{PLH}	Propagation Delay Time, Low to High Output		1.5	2.5	3.3	ns
t _{PHL}	Propagation Delay Time, High to Low Output		1.5	2.5	3.3	ns
t _r	Differential Output Signal Rise Time			0.4		ns
t _f	Differential Output Signal Fall Time	C _L = 10pF, Fig. 1		0.4	. 1 0	าร
t _{sk(O)}	Channel to Channel Output Skew (note1)			0.1	03	ns
t _{sk(P)}	Pulse Skew (t _{PHL} - t _{PLH}) (note2)		. (7.2	0.4	ns
t _{sk(PP)}	Part to Part Skew (note3)	•	011		1	ns
t _{PZH}	Propagation Delay Time, High Impedance to High Level Output	3/8		3	12	ns
t _{PZL}	Propagation Delay Time, High Impedance to Low Level Output	Fig. 2	01	5	12	ns
t _{PHZ}	Propagation Delay Time, High Level to High Impedance Output	19.2		5	12	ns
t _{PLZ}	Propagation Delay Time, Low Level to High Impedance Output	ol coles		5	12	ns

Note:

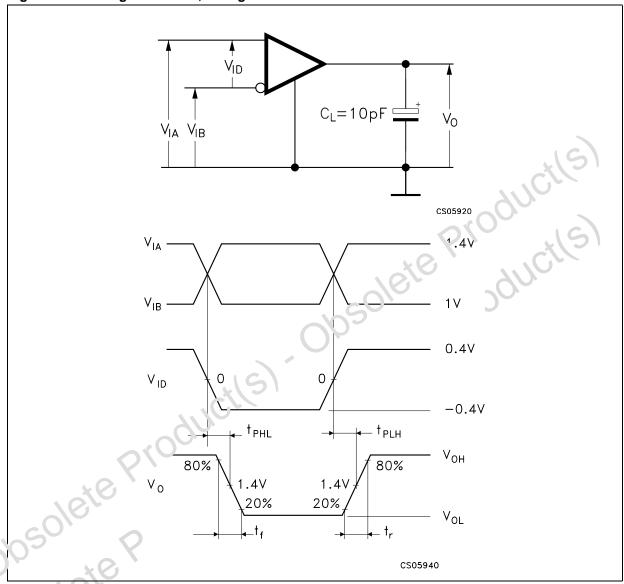
- $t_{sk(O)}$ is the maximum delay time difference between the propagation delay of one channel and that of the outers on the same chip with any event on the inputs.
- $t_{sk(P)}$ is the magnitude difference in differential propagation delay time between the positive going eage and the negative going edge of the same channel.
- and the negative and the negative and the negative specification applies to device operating temperature range. $f_{sk}(P_F)$ is the differential channel-to-channel skew of any event between devices. This specification applies to devices at the same V_{CC}, and within 5°C of each other within the



Test circuit STLVDS3486

5 Test circuit

Figure 3. Timing test circuit, timing and waveforms



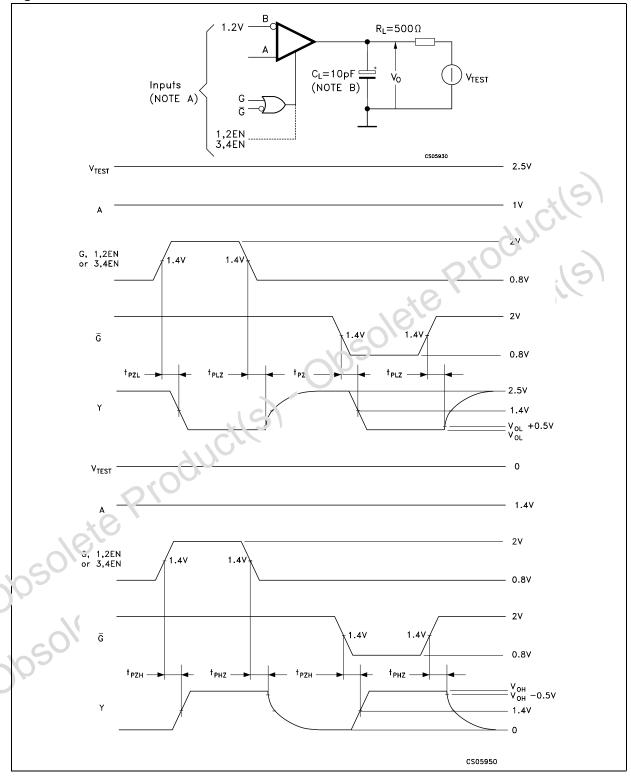
Note A: All input pulse are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 50Mpps, pulse width = 10 ± 0.2ns.

Note B: C_L includes instrumentation and fixture capacitance within 6mm of the D.U.T.



STLVDS3486 Test circuit

Figure 4. Enable and disable time test circuit and waveform



Note A: All input pulse are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 50Mpps, pulse width = 500 \pm 10ns. Note B: C_L includes instrumentation and fixture capacitance within 6mm of the D.U.T.

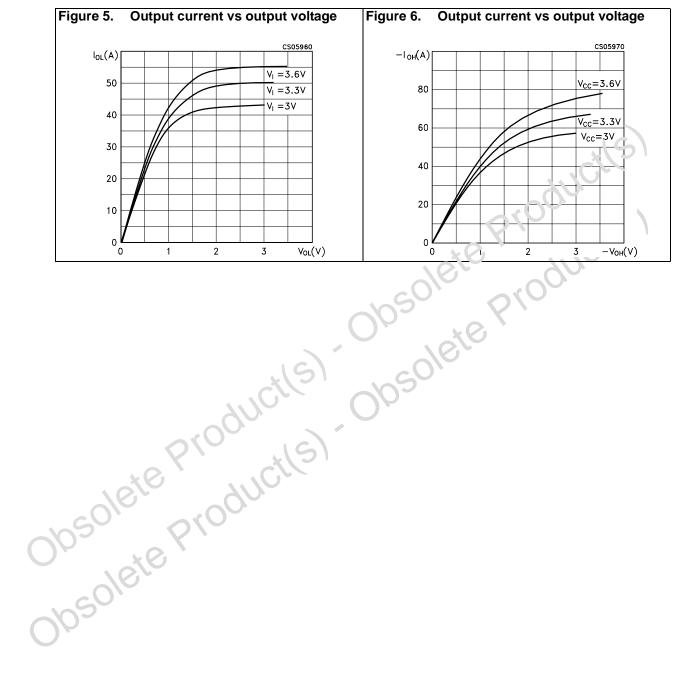


Typical performance characteristics

STLVDS3486

6 Typical performance characteristics

(unless otherwise specified at $T_{.l} = 25^{\circ}C$)





Package mechanical data

7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

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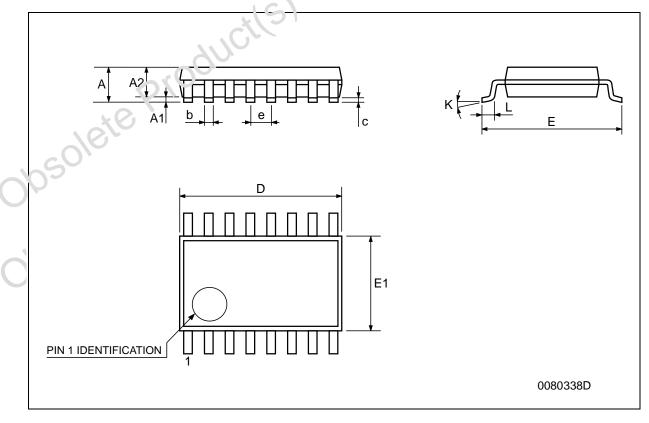


Package mechanical data

STLVDS3486

TSSOP16 MECHANICAL DATA

DIM.		mm.		inch			
DIWI.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.	
А			1.2			0.047	
A1	0.05		0.15	0.002	0.004	0.006	
A2	0.8	1	1.05	0.031	0.039	0.041	
b	0.19		0.30	0.007		0.012	
С	0.09		0.20	0.004		0.0079	
D	4.9	5	5.1	0.193	0.197	0.201	
E	6.2	6.4	6.6	0.244	0.252	0.260	
E1	4.3	4.4	4.48	0.109	0.173	0.176	
е		0.65 BSC		0/0	0.0256 BSC		
K	0°		C° O	0°		8°	
L	0.45	0.60	0.75	0.018	0.024	0.030	

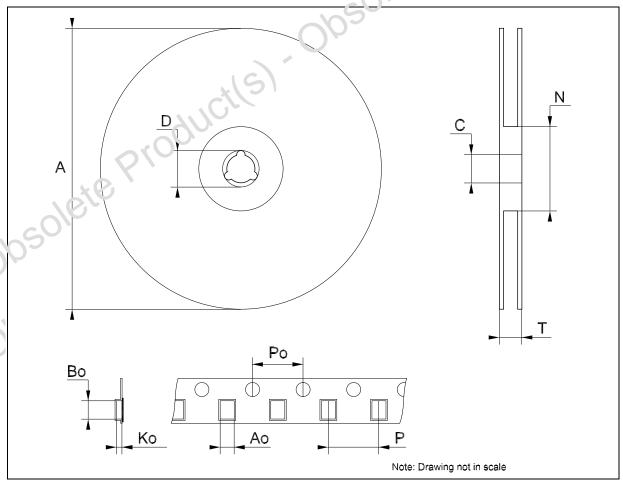




Package mechanical data

Tape & Reel TSSOP16 MECHANICAL DATA

DIM.	mm.			inch			
DIWI.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.	
А			330			12.992	
С	12.8		13.2	0.504		0.519	
D	20.2			0.795			
N	60			2.362			
Т			22.4			C 865	
Ao	6.7		6.9	0.264		0.272	
Во	5.3		5.5	0.209	<u> </u>	0.217	
Ko	1.6		1.8	0.063	210	0.071	
Po	3.9		4.1	0.153		0.161	
Р	7.9		8.1	(1.311		0.319	





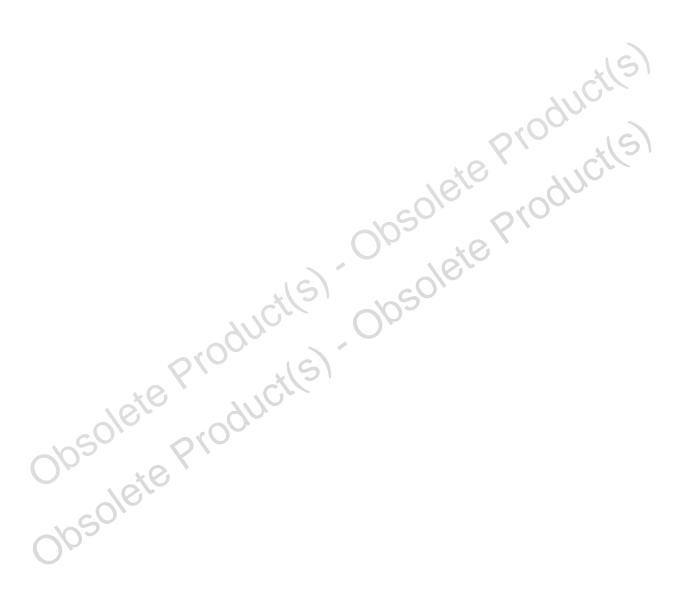


Revision history STLVDS3486

8 Revision history

Table 7. Revision history

Date	Revision	Changes
06-Apr-2006	4	Order codes has been updated and new template.





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STLVDS3486

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