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STP12NM50 - STP12NM50FP STB12NM50 - STB12NM50-1

N-channel 550V @ t_{jmax} - 0.30Ω - 12A TO-220/FP/D²/I²PAK
MDmesh™ Power MOSFET

General features

Type	V _{DSS} (@T _{jmax})	R _{DS(on)}	I _D
STB12NM50	550V	<0.35Ω	12A
STB12NM50-1	550V	<0.35Ω	12A
STP12NM50	550V	<0.35Ω	12A
STP12NM50FP	550V	<0.35Ω	12A

- High dv/dt and avalanche capabilities
- Low input capacitance and gate charge
- 100% avalanche tested
- Low gate input resistance
- Tight process control and high manufacturing yields

Description

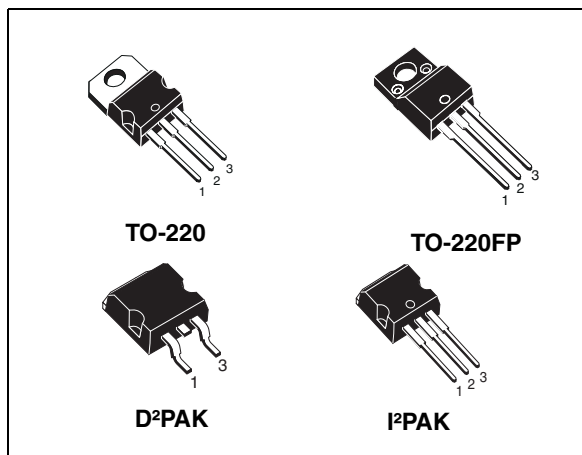
The MDmesh™ is a new revolutionary MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competition's products.

Applications

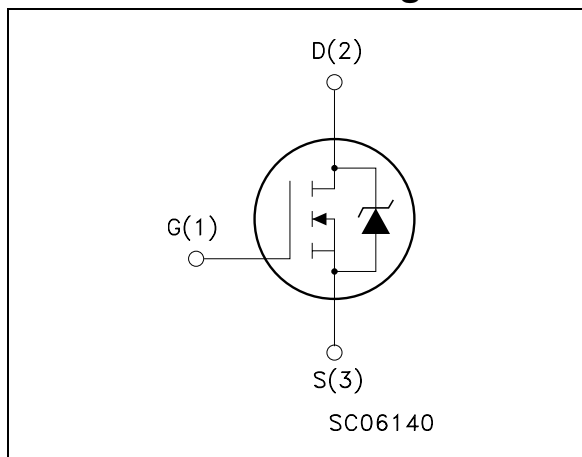
- Switching application

Order codes

Part number	Marking	Package	Packaging
STB12NM50T4	B12NM50	D ² PAK	Tape & reel
STB12NM50-1	B12NM50	I ² PAK	Tube
STP12NM50	P12NM50	TO-220	Tube
STP12NM50FP	P12NM50FP	TO-220FP	Tube



Internal schematic diagram



Contents

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3	Test circuit	9
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STP12NM50-STP12NM50FP-STB12NM50-STB12NM50-1

Electrical ratings

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220- /D ² PAK/I ² PAK	TO-220FP	
V _{GS}	Gate-source voltage	± 30		V
I _D	Drain current (continuous) at T _C = 25°C	12	12 ⁽¹⁾	A
I _D	Drain current (continuous) at T _C =100°C	7.5	7.5 ⁽¹⁾	A
I _{DM} ⁽²⁾	Drain current (pulsed)	48	48 ⁽¹⁾	A
P _{TOT}	Total dissipation at T _C = 25°C	160	35	W
	Derating Factor	1.28	0.28	W/°C
V _{ISO}	Insulation withstand voltage (DC)	--	2500	V
dv/dt ⁽³⁾	Peak diode recovery voltage slope	15		V/ns
T _J T _{stg}	Operating junction temperature Storage temperature	-65 to 150		°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. I_{SD} ≤2A, di/dt ≤400A/μs, V_{DD} =80%V_{(BR)DSS}

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		TO-220/D ² PAK/ I ² PAK	TO-220FP	
R _{thj-case}	Thermal resistance junction-case Max	0.78	3.57	°C/W
R _{thj-a}	Thermal resistance junction-ambient Max	62.5		°C/W
T _I	Maximum lead temperature for soldering purpose	300		°C

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by T _j Max)	6	A
E _{AS}	Single pulse avalanche energy (starting T _j =25°C, I _d =I _{ar} , V _{dd} =50V)	400	mJ

Electrical characteristics

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2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 250 μA, V _{GS} = 0	500			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = Max rating, V _{DS} = Max rating @ 125°C			1 10	μA μA
I _{GSS}	Gate body leakage current (V _{DS} = 0)	V _{GS} = ±30V			± 100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 50μA	3	4	5	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10V, I _D = 6A		0.30	0.35	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g _{fs} ⁽¹⁾	Forward transconductance	V _{DS} = 15V, I _D = 6A		5.5		S
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		1000 250 20		pF pF pF
C _{oss eq} ⁽²⁾	Equivalent output capacitance	V _{GS} = 0, V _{DS} = 0V to 400V		90		pF
t _{d(on)} t _r	Turn-on Delay Time Rise Time	V _{DD} = 250V, I _D = 6A, R _G = 4.7Ω V _{GS} = 10V (see Figure 14)		20 10		ns ns
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	V _{DD} = 400V, I _D = 12A V _{GS} = 10V (see Figure 15)		28 8 18	39	nC nC nC
R _g	Gate input resistance	f = 1MHz Gate DC Bias = 0 test signal level = 20mV open drain		1.6		Ω

1. Pulsed: pulse duration = 300μs, duty cycle 1.5%

2. C_{oss eq} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

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Electrical characteristics

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				11	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				48	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=12A$, $V_{GS}=0$			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=12A$, $di/dt = 100A/\mu s$, $V_{DD}=100V$, $T_J=25^\circ C$ (see Figure 16)		270 2.23 16.5		ns μC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=12A$, $di/dt = 100A/\mu s$, $V_{DD}=100V$, $T_J=150^\circ C$ (see Figure 16)		340 3 18		ns μC A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

Electrical characteristics

STP12NM50-STP12NM50FP-STB12NM50-STB12NM50-1

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

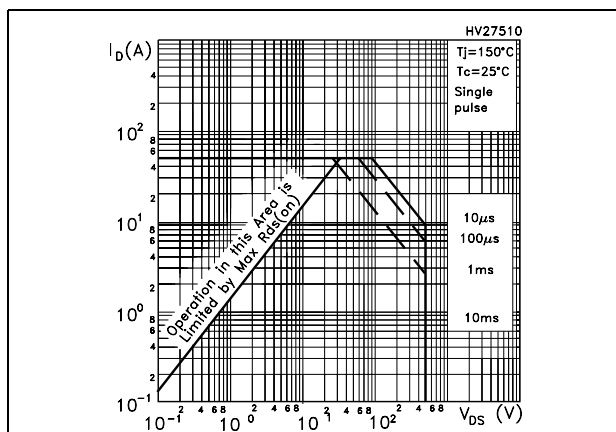


Figure 2. Thermal impedance

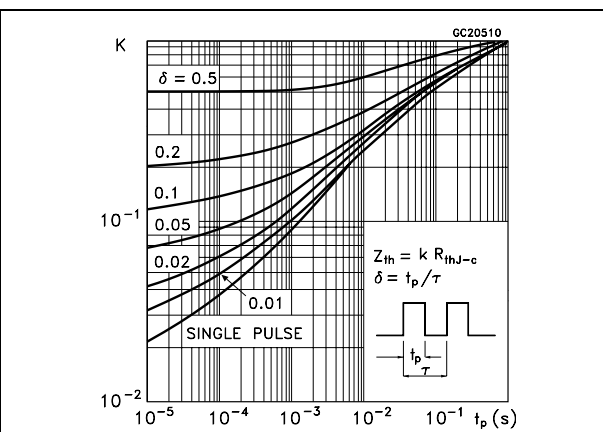


Figure 3. Safe operating area for TO-220FP

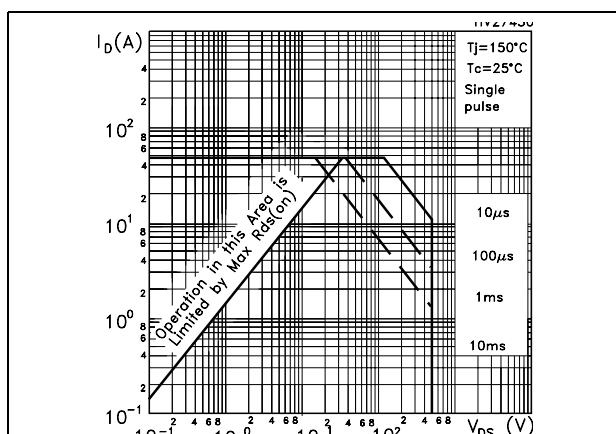


Figure 4. Thermal impedance for TO-220FP

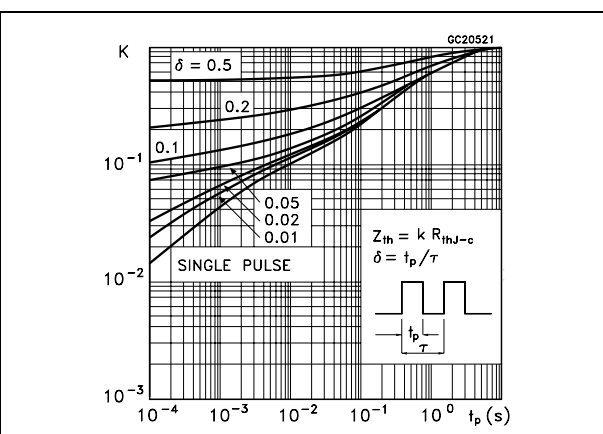


Figure 5. Output characteristics

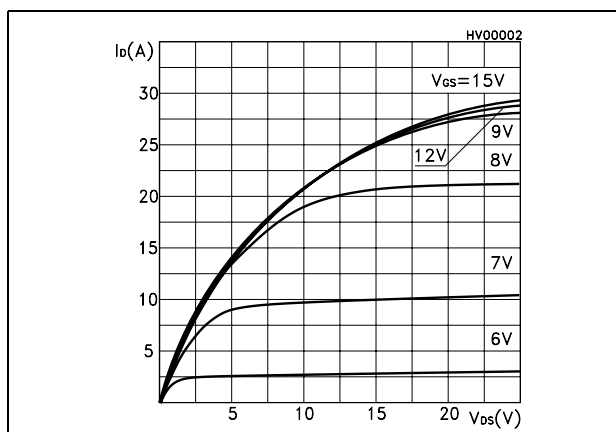
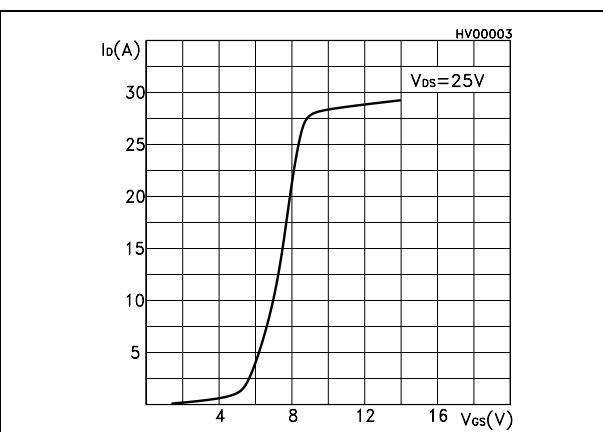


Figure 6. Transfer characteristics



STP12NM50-STP12NM50FP-STB12NM50-STB12NM50-1

Electrical characteristics

Figure 7. Transconductance

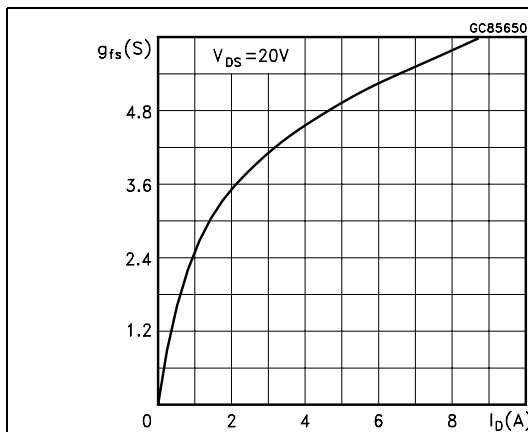


Figure 8. Static drain-source on resistance

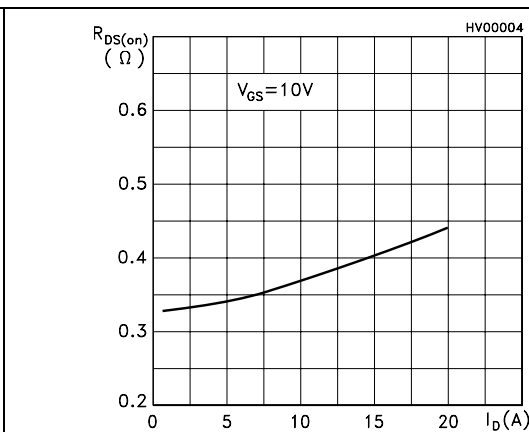


Figure 9. Gate charge vs gate-source voltage **Figure 10. Capacitance variations**

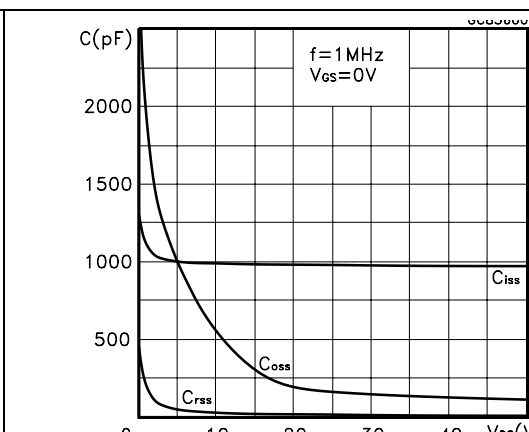
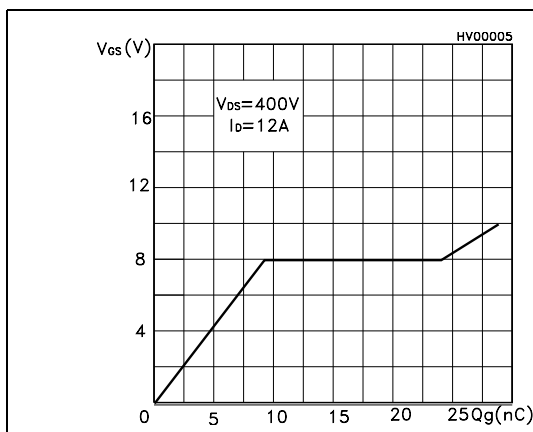


Figure 11. Normalized gate threshold voltage vs temperature

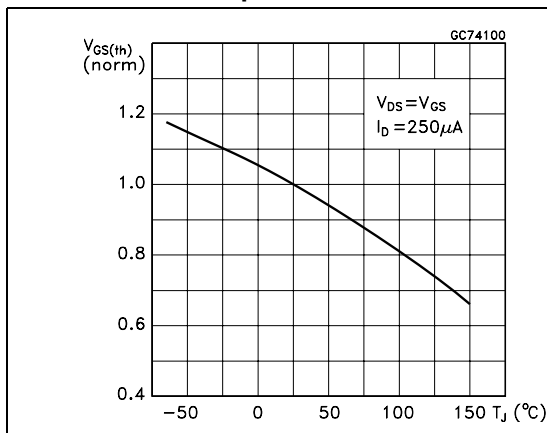
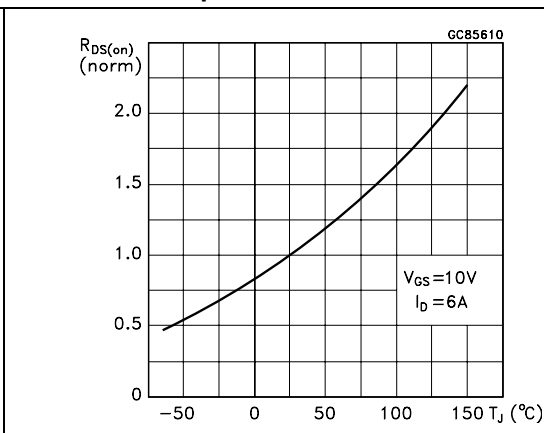


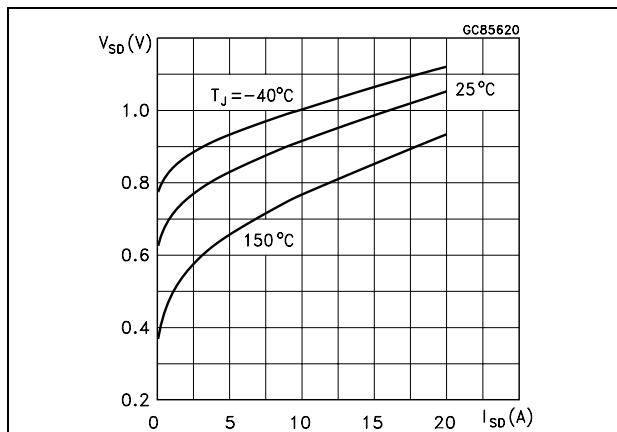
Figure 12. Normalized on resistance vs temperature



Electrical characteristics

STP12NM50-STP12NM50FP-STB12NM50-STB12NM50-1

Figure 13. Source-drain diode forward characteristics



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Test circuit

3 Test circuit

Figure 14. Switching times test circuit for resistive load

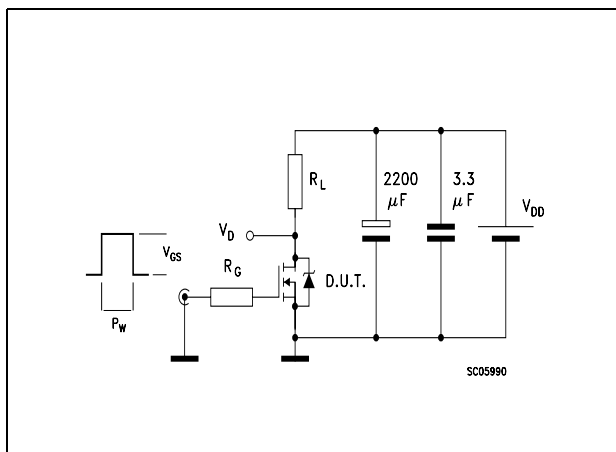


Figure 15. Gate charge test circuit

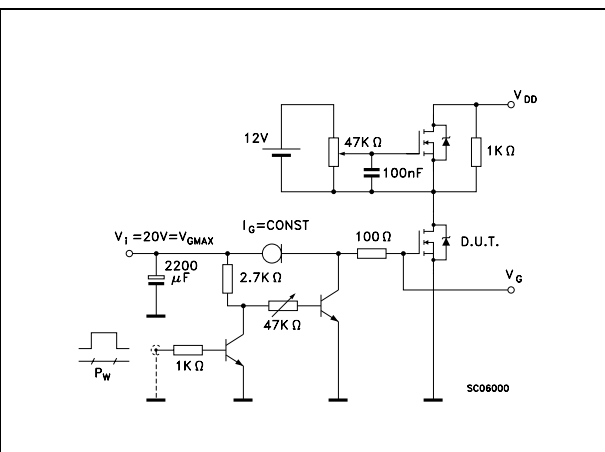


Figure 16. Test circuit for inductive load switching and diode recovery times

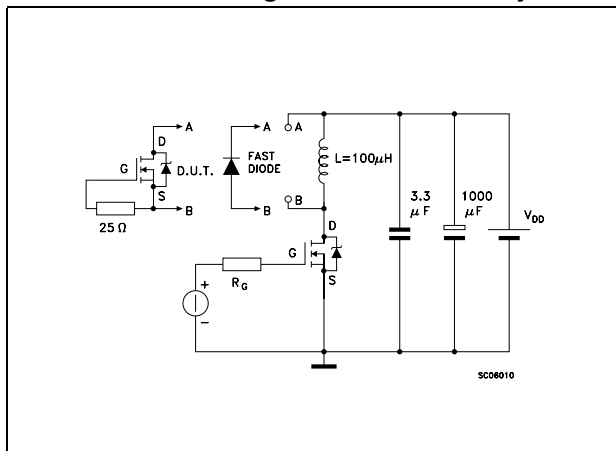


Figure 17. Unclamped Inductive load test circuit

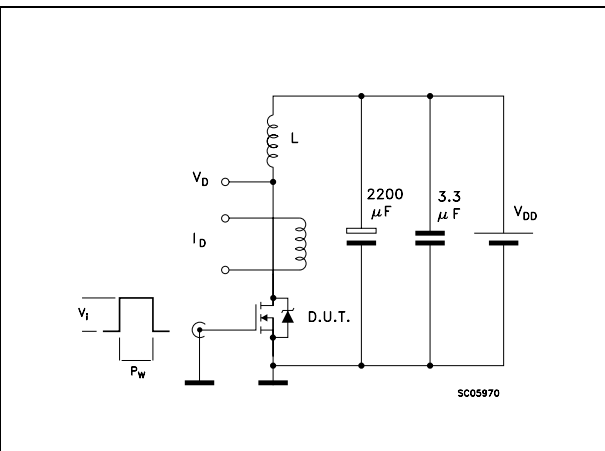


Figure 18. Unclamped inductive waveform

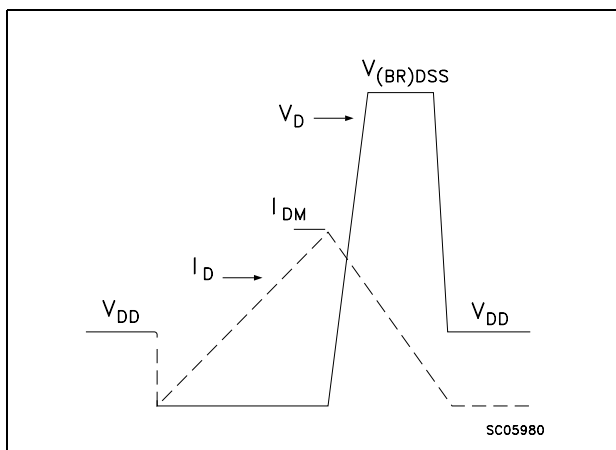
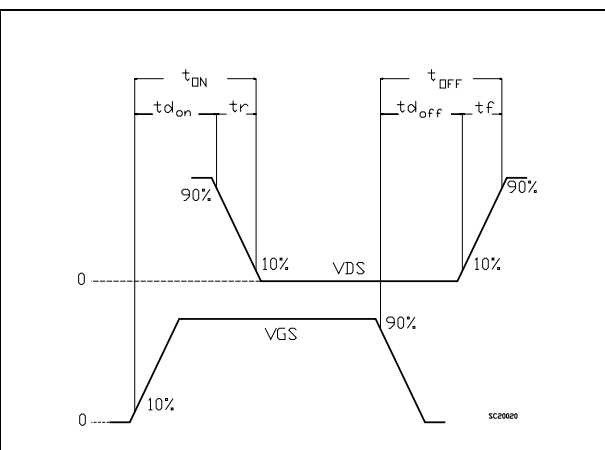


Figure 19. Switching time waveform



Package mechanical data**STP12NM50-STP12NM50FP-STB12NM50-STB12NM50-1**

4 Package mechanical data

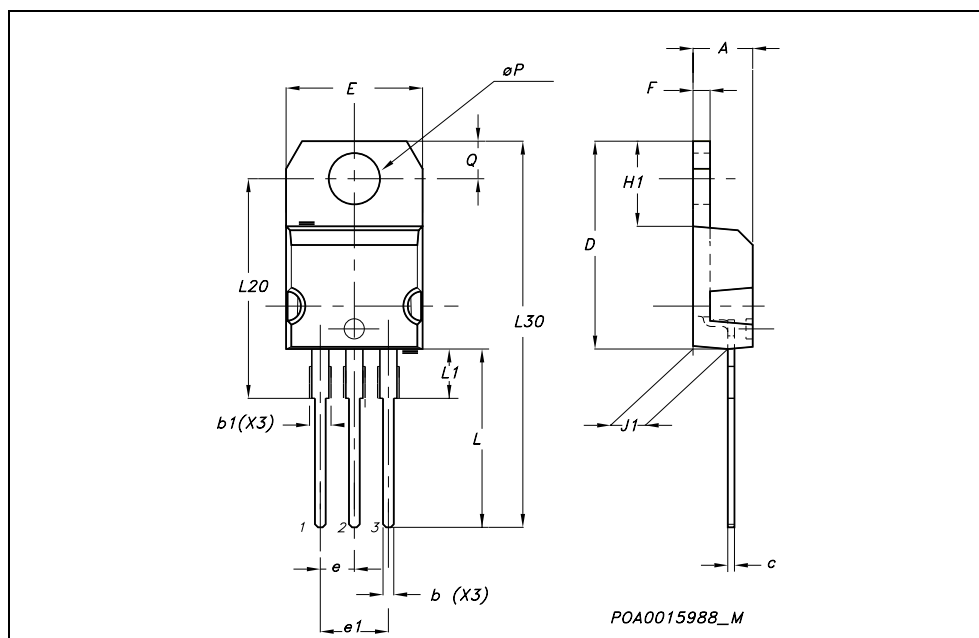
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

STP12NM50-STP12NM50FP-STB12NM50-STB12NM50-1

Package mechanical data

TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116

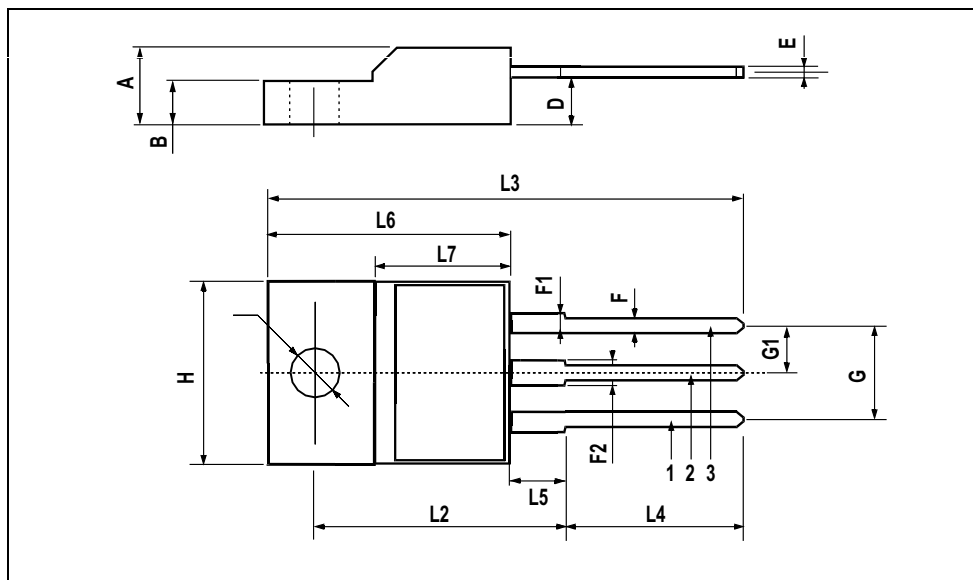


Package mechanical data

STP12NM50-STP12NM50FP-STB12NM50-STB12NM50-1

TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126

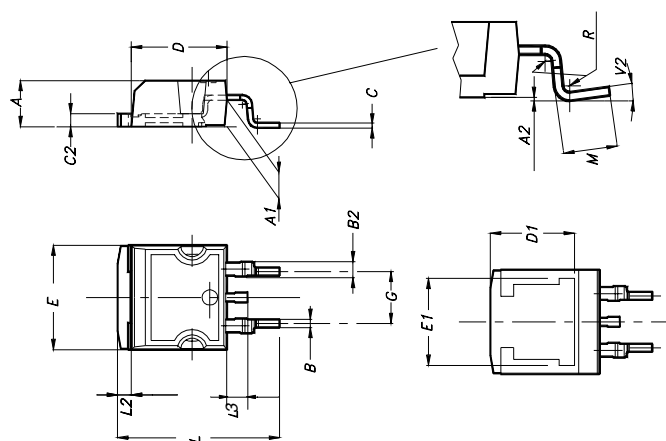


STP12NM50-STP12NM50FP-STB12NM50-STB12NM50-1

Package mechanical data

D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			

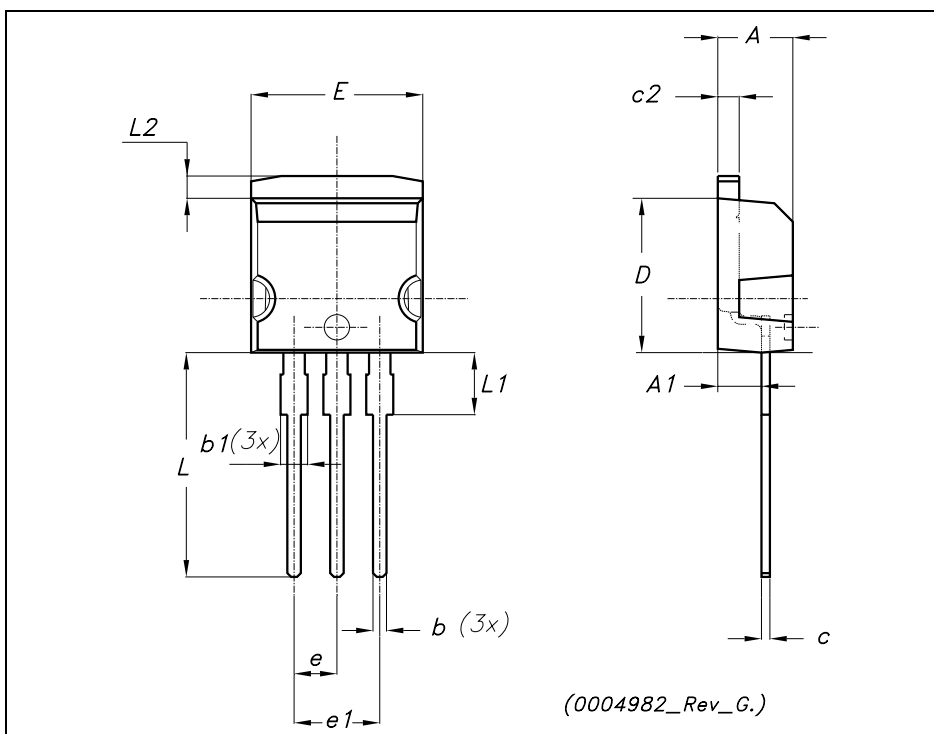


Package mechanical data

STP12NM50-STP12NM50FP-STB12NM50-STB12NM50-1

TO-262 (I²PAK) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
A1	2.40		2.72	0.094		0.107
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.49		0.70	0.019		0.027
c2	1.23		1.32	0.048		0.052
D	8.95		9.35	0.352		0.368
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
E	10		10.40	0.393		0.410
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L2	1.27		1.40	0.050		0.055

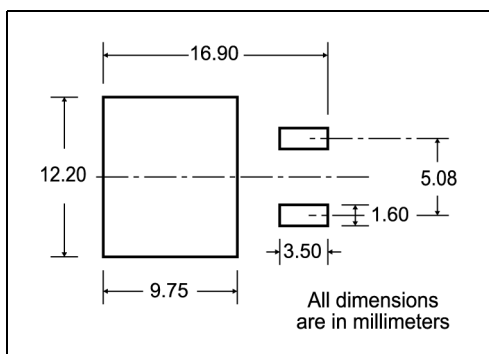


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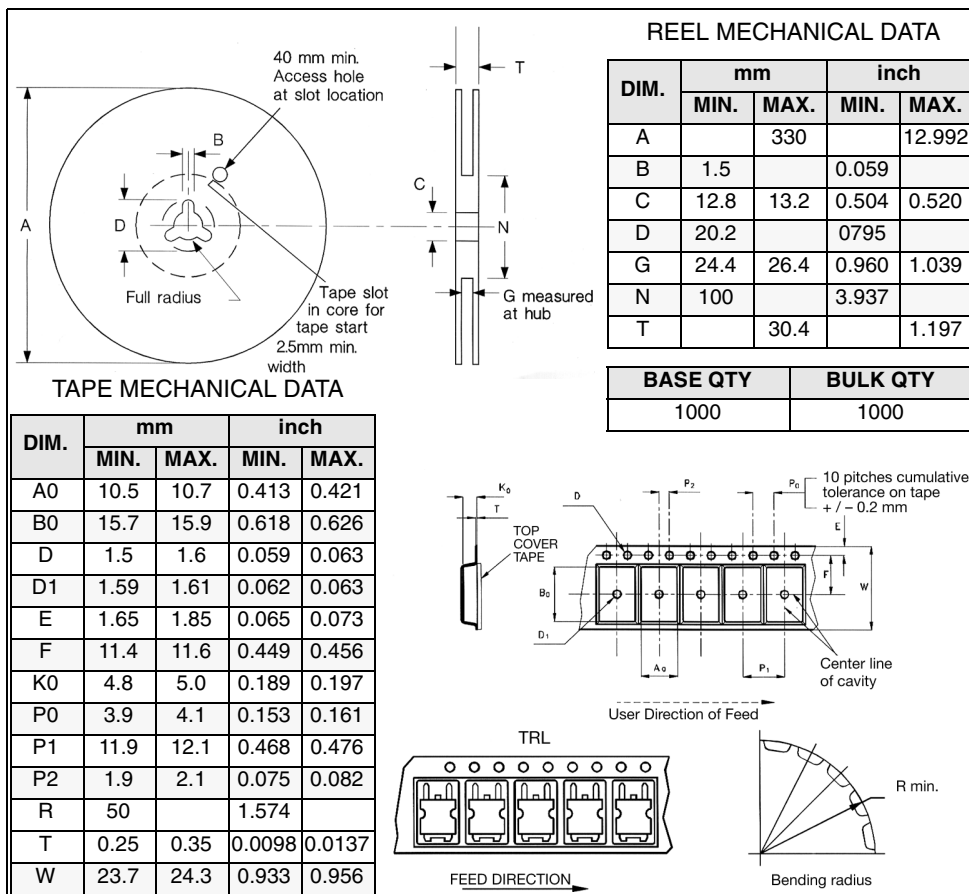
Packaging mechanical data

5 Packaging mechanical data

D²PAK FOOTPRINT



TAPE AND REEL SHIPMENT



* on sales type

6 Revision history

Table 7. Revision history

Date	Revision	Changes
14-Mar-2004	8	Preliminary version
15-Feb-2006	9	New voltage value on first page at t_{jmax} .
05-Apr-2006	10	Inserted ecopack indication
27-Jul-2006	11	New template, no content change

STP12NM50-STP12NM50FP-STB12NM50-STB12NM50-1

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