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ON Semiconductor
NTGS3446T1

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NTGS3446

Power MOSFET 20 V, 5.1 A Single N-Channel, TSOP6

ON Semiconductor®

http://onsemi.com

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
20 V	36 mΩ @ 4.5 V	5.1 A

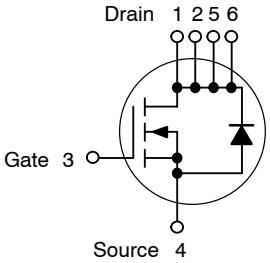
Features

- Ultra Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Diode Exhibits High Speed, Soft Recovery
- Avalanche Energy Specified
- I_{DSS} Specified at Elevated Temperature
- Pb−Free Package is Available

Applications

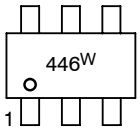
- Power Management in portable and battery−powered products, i.e. computers, printers, PCMCIA cards, cellular and cordless
- Lithium Ion Battery Applications
- Notebook PC

N−Channel



MARKING DIAGRAM

TSOP−6
CASE 318G
STYLE 1



446 = Device Code
W = Work Week

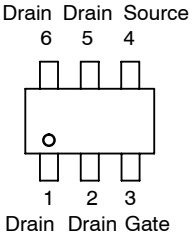
MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	20	V
Gate−to−Source Voltage	V_{GS}	±12	V
Thermal Resistance Junction−to−Ambient (Note 1) Total Power Dissipation @ T_A = 25°C Drain Current − Continuous @ T_A = 25°C − Pulsed Drain Current (t_p < 10 μs)	 $R_{\theta JA}$ P_d I_D I_{DM}	 244 0.5 2.5 10	 °C/W W A A
Thermal Resistance Junction−to−Ambient (Note 2) Total Power Dissipation @ T_A = 25°C Drain Current − Continuous @ T_A = 25°C − Pulsed Drain Current (t_p < 10 μs)	 $R_{\theta JA}$ P_d I_D I_{DM}	 128 1.0 3.6 14	 °C/W W A A
Thermal Resistance Junction−to−Ambient (Note 3) Total Power Dissipation @ T_A = 25°C Drain Current − Continuous @ T_A = 25°C − Pulsed Drain Current (t_p < 10 μs)	 $R_{\theta JA}$ P_d I_D I_{DM}	 62.5 2.0 5.1 20	 °C/W W A A
Source Current (Body Diode)	I_S	5.1	A
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C
Maximum Lead Temperature for Soldering Purposes for 10 seconds	T_L	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Minimum FR−4 or G−10PCB, operating to steady state.
2. Mounted onto a 2" square FR−4 board (1" sq. 2 oz. cu. 0.06" thick single−sided), operating to steady state.
3. Mounted onto a 2" square FR−4 board (1" sq. 2 oz. cu. 0.06" thick single−sided), t < 5.0 seconds.

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping†
NTGS3446T1	TSOP−6	3000/Tape & Reel
NTGS3446T1G	TSOP−6 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTGS3446

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain−to−Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc) Temperature Coefficient (Positive)	$V_{(BR)DSS}$	20 –	– 22	– –	Vdc mV/°C
Zero Gate Voltage Collector Current (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc, T_J = 85°C)	I_{DSS}	 – –	 – –	 1.0 25	µAdc
Gate−Body Leakage Current (V_{GS} = ±12 Vdc, V_{DS} = 0)	$I_{GSS(f)}$ $I_{GSS(r)}$	– –	– –	100 −100	nAdc
ON CHARACTERISTICS (Note 4)					
Gate Threshold Voltage I_D = 0.25 mA, V_{DS} = V_{GS} Temperature Coefficient (Negative)	$V_{GS(th)}$	0.6 –	0.85 −2.5	1.2 –	Vdc mV/°C
Static Drain−to−Source On−Resistance (V_{GS} = 4.5 Vdc, I_D = 5.1 Adc) (V_{GS} = 2.5 Vdc, I_D = 4.4 Adc)	$R_{DS(on)}$	 – –	 36 44	 45 55	mΩ
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 5.1 Adc)	g_{FS}	–	12	–	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 10 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	–	510	750	pF
Output Capacitance		C_{oss}	–	200	350	
Transfer Capacitance		C_{rss}	–	60	100	
SWITCHING CHARACTERISTICS (Note 5)					
Turn−On Delay Time	(V_{DD} = 10 Vdc, I_D = 1.0 Adc, V_{GS} = 4.5 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	–	9.0	16	ns
Rise Time		t_r	–	12	20	
Turn−Off Delay Time		$t_{d(off)}$	–	35	60	
Fall Time		t_f	–	20	35	
Gate Charge	(V_{DS} = 10 Vdc, I_D = 5.1 Adc, V_{GS} = 4.5 Vdc)	Q_T	–	8.0	15	nC
		Q_{gs}	–	2.0	–	
		Q_{gd}	–	2.0	–	
SOURCE−DRAIN DIODE CHARACTERISTICS					
Forward On−Voltage (Note 4)	(I_S = 1.7 Adc, V_{GS} = 0 Vdc) (I_S = 1.7 Adc, V_{GS} = 0 Vdc, T_J = 85°C)	V_{SD}	 – –	 0.74 0.66	 1.1 –	Vdc
Reverse Recovery Time	(I_S = 1.7 Adc, V_{GS} = 0 Vdc, di_S/dt = 100 A/µs)	t_{rr}	–	20	–	ns
		t_a	–	11	–	
		t_b	–	9.0	–	
Reverse Recovery Stored Charge		Q_{RR}	–	0.01	–	µC

4. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperature.

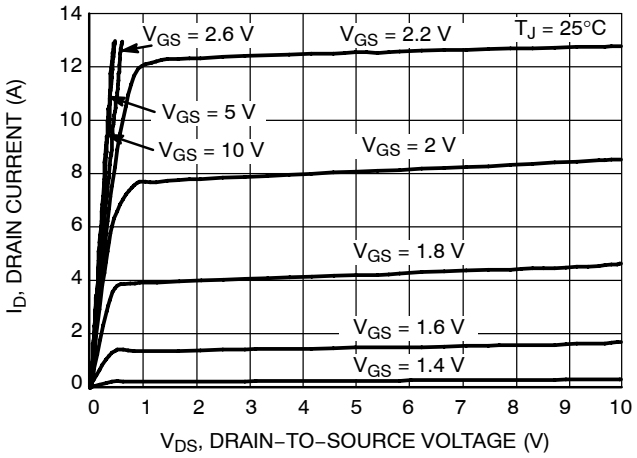


Figure 1. On−Region Characteristics

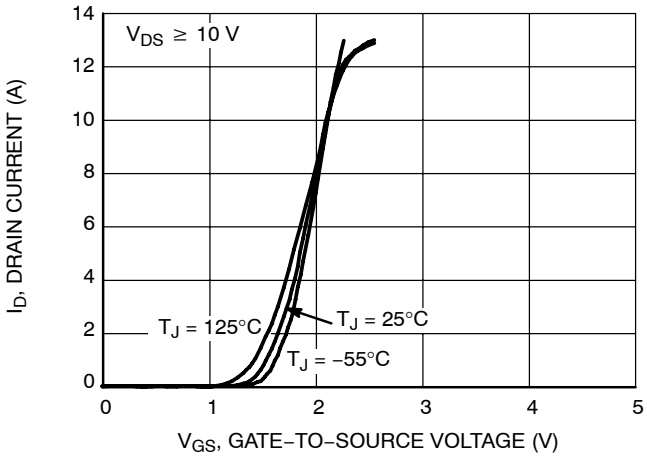


Figure 2. Transfer Characteristics

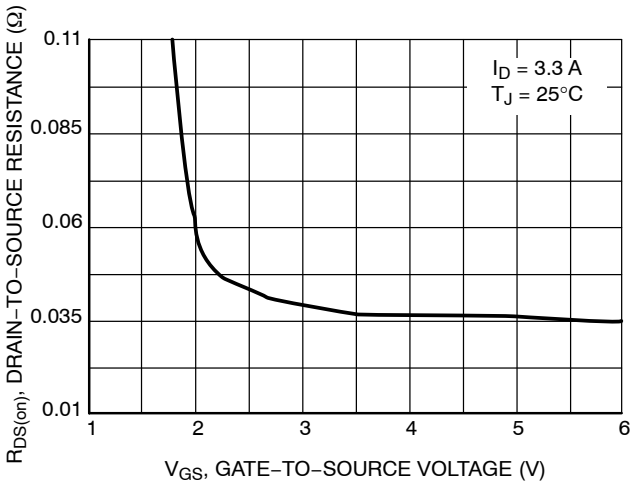


Figure 3. On−Resistance versus Gate−To−Source Voltage

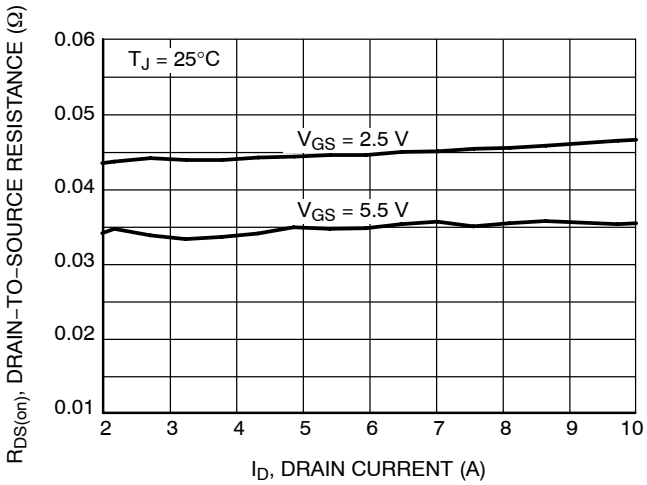


Figure 4. On−Resistance versus Drain Current and Gate Voltage

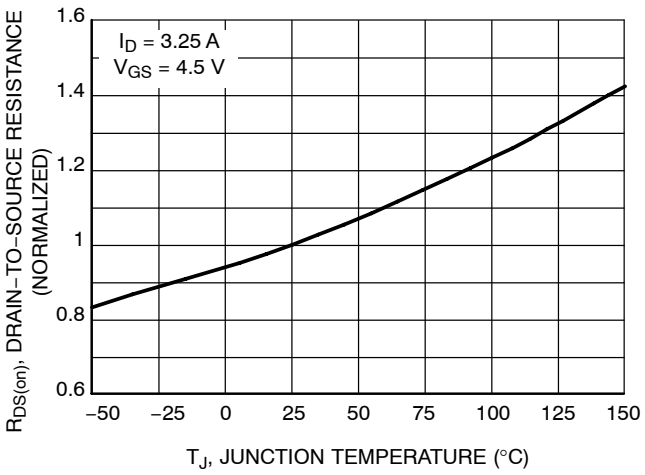


Figure 5. On−Resistance Variation with Temperature

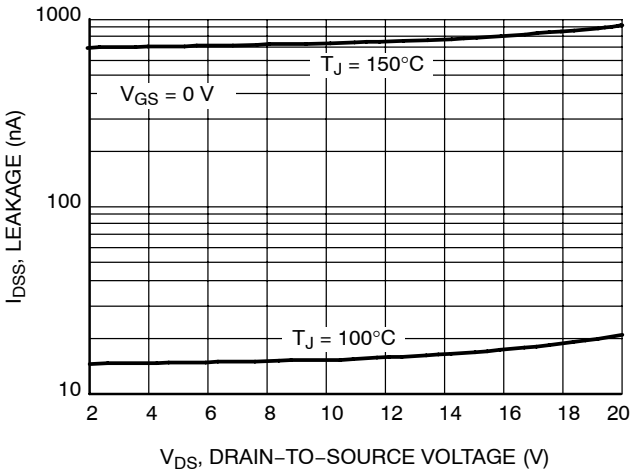


Figure 6. Drain−to−Source Leakage Current versus Voltage

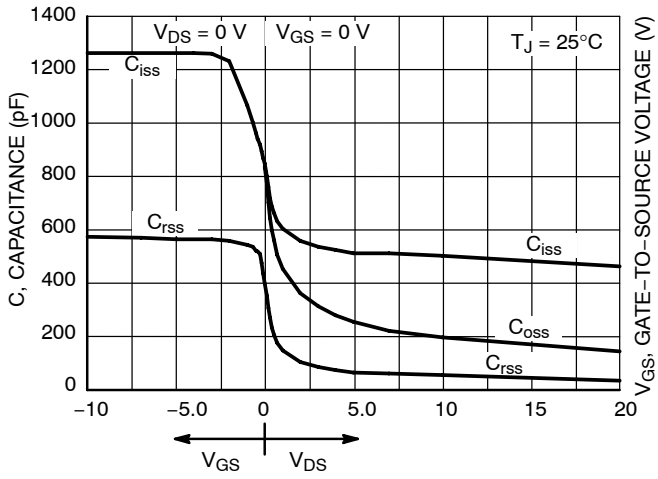


Figure 7. Capacitance Variation

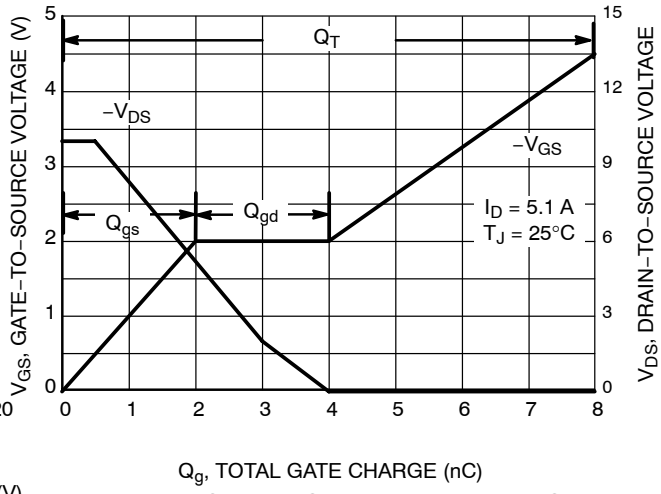


Figure 8. Gate−to−Source and Drain−to−Source Voltage versus Total Charge

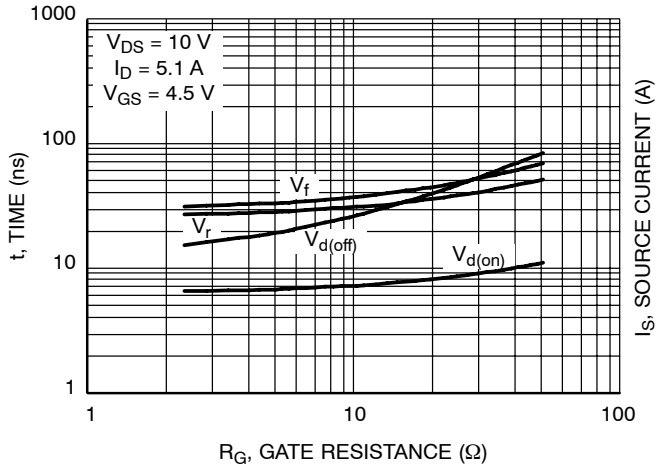


Figure 9. Resistive Switching Time Variation versus Gate Resistance

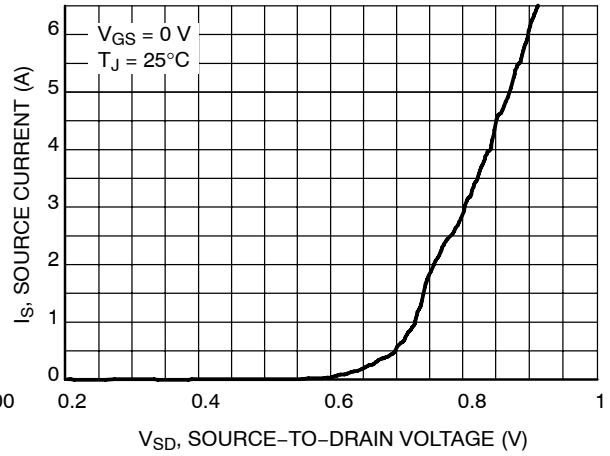
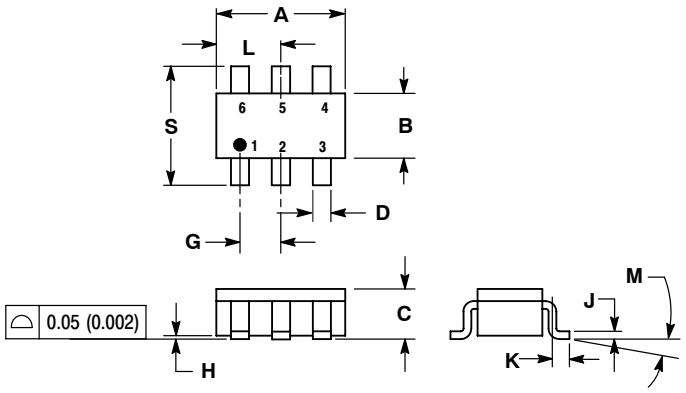


Figure 10. Diode Forward Voltage versus Current

NTGS3446

PACKAGE DIMENSIONS

TSOP−6
CASE 318G−02
ISSUE N

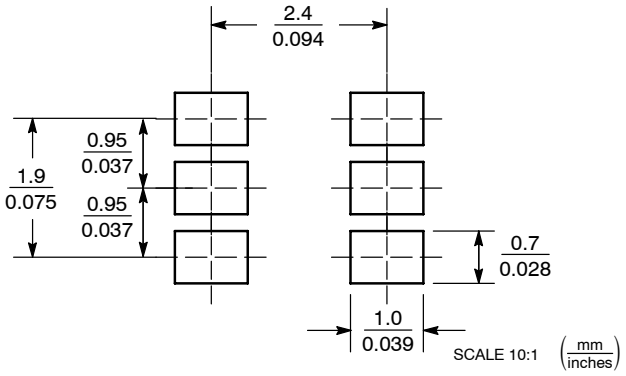


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0 °	10 °	0 °	10 °
S	2.50	3.00	0.0985	0.1181

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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